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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc55a-04-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### 3.1 **Clocking Scheme/Instruction** Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

#### 3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



#### FIGURE 3-2: **CLOCK/INSTRUCTION CYCLE**

#### EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

# PIC16C5X



## FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME



## FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): SLOW VDD RISE TIME



#### 8.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

#### 8.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

#### EXAMPLE 8-1: CHANGING PRESCALER (TIMER0→WDT)

CLRWDT	;Clear WDT
CLRF TMR0	;Clear TMR0 & Prescaler
MOVLW B'00xx1111'	;Last 3 instructions in
	this example
OPTION	;are required only if
	;desired
CLRWDT	;PS<2:0> are 000 or
	;001
MOVLW B'00xx1xxx'	;Set Prescaler to
OPTION	;desired WDT rate

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

# EXAMPLE 8-2: CHANGING PRESCALER (WDT $\rightarrow$ TIMER0)

CLRWDT		;Clear WDT and
		;prescaler
MOVLW	B'xxxx0xxx'	;Select TMR0, new
		;prescale value and
		;clock source

OPTION

#### 11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

### 11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multiproject software development tool.

#### 11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft<sup>®</sup> Windows environment were chosen to best make these features available to you, the end user.

### 11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

#### 12.1 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)

PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial				
Param No.	Symbol	bol Characteristic/Device		Тур†	Max	Units	Conditions
D001	Vdd	Supply Voltage PIC16C5X-RC PIC16C5X-XT PIC16C5X-10 PIC16C5X-HS	3.0 3.0 4.5 4.5		6.25 6.25 5.5 5.5	V V V V	
D002	Vdr	PIC16C5X-LP RAM Data Retention Voltage <sup>(1)</sup>	2.5	 1.5*	6.25 —	V V	Device in SLEEP Mode
D003	Vpor	VDD Start Voltage to ensure Power-on Reset		Vss	_	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current <sup>(2)</sup> PIC16C5X-RC <sup>(3)</sup> PIC16C5X-XT PIC16C5X-10 PIC16C5X-HS PIC16C5X-HS PIC16C5X-LP		1.8 1.8 4.8 9.0 15	3.3 3.3 10 10 20 32	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = $32$ kHz, VDD = $3.0V$ , WDT disabled
D020	IPD	Power-down Current <sup>(2)</sup>		4.0 0.6	12 9	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled

\* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .

#### 12.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage PIC16C5X-RCI PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI	3.0 3.0 4.5 4.5		6.25 6.25 5.5 5.5 6.25	V V V V		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	2.5	1.5*		V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current <sup>(2)</sup> PIC16C5X-RCI <sup>(3)</sup> PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI PIC16C5X-LPI		1.8 1.8 4.8 9.0 15	3.3 3.3 10 10 20 40	mA mA mA mA μA	Fosc = 4 MHz, VDD = $5.5V$ Fosc = 4 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = $32$ kHz, VDD = $3.0V$ , WDT disabled	
D020	IPD	Power-down Current <sup>(2)</sup>	_	4.0 0.6	14 12	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled	

\* These parameters are characterized but not tested.

- † Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
  - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
    - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
    - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
  - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

#### TABLE 14-2: INPUT CAPACITANCE FOR PIC16C54/56

Pin	Typical Capacitance (pF)				
FIII	18L PDIP	18L SOIC			
RA port	5.0	4.3			
RB port	5.0	4.3			
MCLR	17.0	17.0			
OSC1	4.0	3.5			
OSC2/CLKOUT	4.3	3.5			
TOCKI	3.2	2.8			

All capacitance values are typical at  $25^{\circ}$ C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

TABLE 14-3:	INPUT CAPACITANCE FOR
	PIC16C55/57

	Typical Capacitance (pF)				
Pin	28L PDIP (600 mil)	28L SOIC			
RA port	5.2	4.8			
RB port	5.6	4.7			
RC port	5.0	4.1			
MCLR	17.0	17.0			
OSC1	6.6	3.5			
OSC2/CLKOUT	4.6	3.5			
TOCKI	4.5	3.5			

All capacitance values are typical at  $25^{\circ}$ C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

### 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$				
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)			$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units Conditions					
	IPD	Power-down Current <sup>(2)</sup>						
D006		PIC16LC5X	—	2.5	12	μΑ	VDD = 2.5V, WDT enabled, Commercial	
			—	0.25	4.0	μΑ	VDD = 2.5V, WDT disabled, Commercial	
			$- \begin{array}{c c c c c c c c c c c c c c c c c c c $					
D006A		PIC16C5X	_	4.0	12	μΑ	VDD = 3.0V, WDT enabled, Commercial	
			—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial	
			—	5.0	14	μΑ	VDD = 3.0V, WDT enabled, Industrial	
				0.3	5.0	μA	$v \Box U = 3.0v, v U T uisabled, industrial$	

Legend: Rows with standard voltage device data only are shaded for improved readability.

\* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k $\Omega$ .



TABLE 16-2:INPUT CAPACITANCE FOR<br/>PIC16C54A/C58A

Pin	Typical Capacitance (pF)				
FIII	18L PDIP	18L SOIC			
RA port	5.0	4.3			
RB port	5.0	4.3			
MCLR	17.0	17.0			
OSC1	4.0	3.5			
OSC2/CLKOUT	4.3	3.5			
TOCKI	3.2	2.8			

All capacitance values are typical at 25°C. A part-to-part variation of  $\pm 25\%$  (three standard deviations) should be taken into account.

#### FIGURE 16-23: PORTA, B AND C IOL vs. VOL, VDD = 5V



### **19.3 Timing Parameter Symbology and Load Conditions**

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. Tp	pS	
Т		
F	Frequency	T Time
Lowe	ercase letters (pp) and their meanings:	
рр		
2	to	mc MCLR
ck	CLKOUT	osc oscillator
су	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer
Uppe	ercase letters and their meanings:	
S		
F	Fall	P Period
Н	High	R Rise
Ι	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

#### FIGURE 19-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS -PIC16C54C/C55A/C56A/C57C/C58B-40











#### 18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.050			1.27	
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-051

### 28-Lead Ceramic Dual In-line with Window (JW) - 600 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.195	.210	.225	4.95	5.33	5.72
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.038	.060	0.38	0.95	1.52
Shoulder to Shoulder Width	Е	.595	.600	.625	15.11	15.24	15.88
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	В	.016	.020	.023	0.41	0.51	0.58
Overall Row Spacing §	eB	.610	.660	.710	15.49	16.76	18.03
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37

Sontolling Parameter
Significant Characteristic
JEDEC Equivalent: MO-103
Drawing No. C04-013

#### Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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ISBN: 9781620769355

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