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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lc55a-04i-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16lc55a-04i-p</a>

## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

# PIC16C5X

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NOTES:

## 6.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a **GOTO** instruction, bits 8:0 of the PC are provided by the **GOTO** instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 6-7, Figure 6-8 and Figure 6-9).

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number must be supplied as well. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

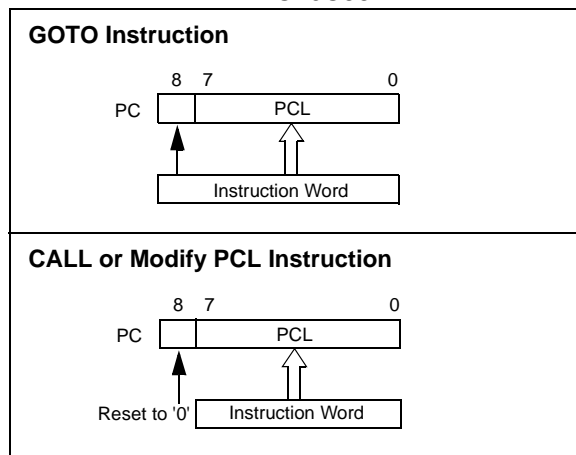
For a **CALL** instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 6-7 and Figure 6-8).

Instructions where the PCL is the destination, or modify PCL instructions, include **MOVWF PCL**, **ADDWF PCL**, and **BSF PCL, 5**.

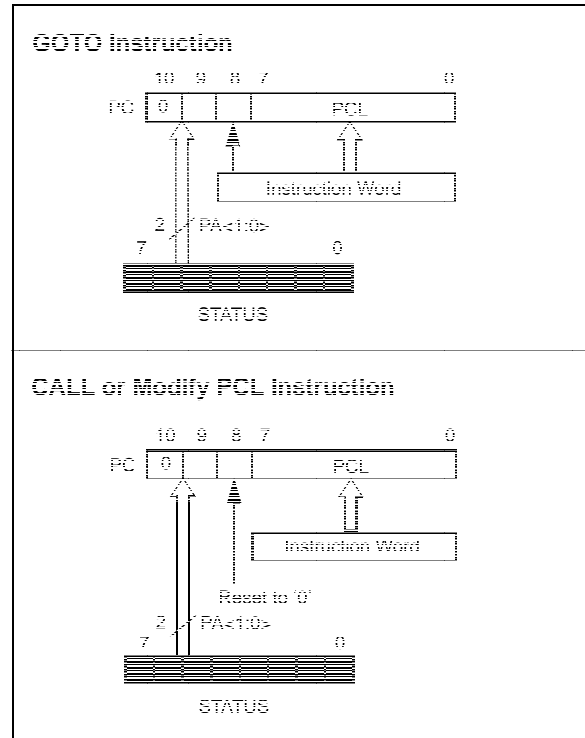
For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number again must be supplied. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

**Note:** Because PC<8> is cleared in the **CALL** instruction, or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

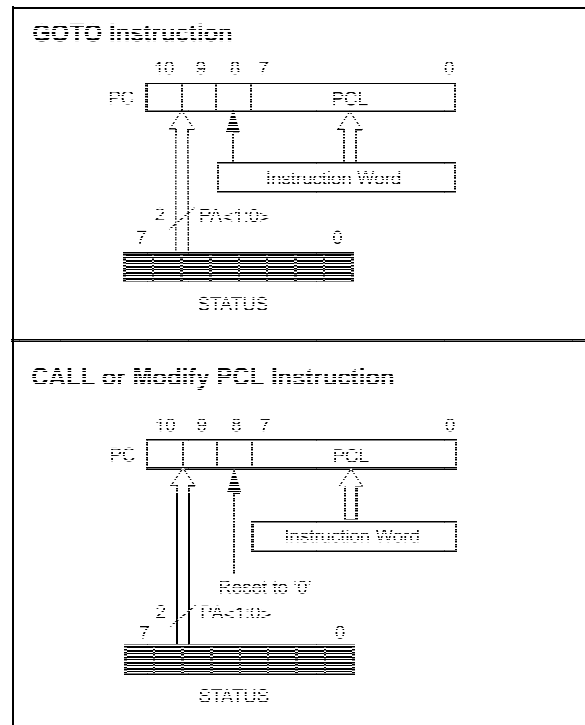
**FIGURE 6-7: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C54, PIC16CR54, PIC16C55**



**FIGURE 6-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C56/PIC16CR56**



**FIGURE 6-9: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C57/PIC16CR57, AND PIC16C58/PIC16CR58**



## 8.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1,x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

### 8.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

#### EXAMPLE 8-1: CHANGING PRESCALER (TIMER0→WDT)

```
CLRWDT          ;Clear WDT
CLRF    TMR0     ;Clear TMR0 & Prescaler
MOVLW  B'00xx1111' ;Last 3 instructions in
                    this example
OPTION          ;are required only if
                ;desired
CLRWDT          ;PS<2:0> are 000 or
                ;001
MOVLW  B'00xx1xxx' ;Set Prescaler to
OPTION          ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

#### EXAMPLE 8-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT          ;Clear WDT and
                ;prescaler
MOVLW  B'xxxx0xxx' ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

## 9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

### 9.3.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the  $\overline{TO}$  bit (STATUS<4>) is set, the  $\overline{PD}$  bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the  $\overline{MCLR}/VPP$  pin low.

For lowest current consumption while powered down, the  $T0CKI$  input should be at  $VDD$  or  $VSS$  and the  $\overline{MCLR}/VPP$  pin must be at a logic high level ( $\overline{MCLR} = V_{IH}$ ).

### 9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external RESET input on  $\overline{MCLR}/VPP$  pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The  $\overline{TO}$  and  $\overline{PD}$  bits can be used to determine the cause of device RESET. The  $\overline{TO}$  bit is cleared if a WDT time-out occurred (and caused wake-up). The  $\overline{PD}$  bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

## 9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

**Note:** Microchip does not recommend code protecting windowed devices.

## 9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

**Note:** Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

## GOTO Unconditional Branch

Syntax: [ *label* ] GOTO *k*

Operands:  $0 \leq k \leq 511$

Operation:  $k \rightarrow PC<8:0>;$   
 $STATUS<6:5> \rightarrow PC<10:9>$

Status Affected: None

Encoding: 

101k	kkkk	kkkk
------	------	------

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction.

Words: 1

Cycles: 2

Example: GOTO THERE

After Instruction  
 PC = address (THERE)

## INCF Increment f

Syntax: [ *label* ] INCF *f,d*

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

Operation:  $(f) + 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding: 

0010	10df	ffff
------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: INCF CNT, 1

Before Instruction  
 CNT = 0xFF  
 Z = 0

After Instruction  
 CNT = 0x00  
 Z = 1

## INCFSZ Increment f, Skip if 0

Syntax: [ *label* ] INCFSZ *f,d*

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

Operation:  $(f) + 1 \rightarrow (\text{dest}), \text{skip if result} = 0$

Status Affected: None

Encoding: 

0011	11df	ffff
------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example: HERE INCFSZ CNT, 1  
 GOTO LOOP  
 CONTINUE •  
 •  
 •

Before Instruction  
 PC = address (HERE)

After Instruction  
 CNT = CNT + 1;  
 if CNT = 0,  
 PC = address (CONTINUE);  
 if CNT  $\neq$  0,  
 PC = address (HERE + 1)

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## RLF Rotate Left f through Carry

Syntax: [label] RLF f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

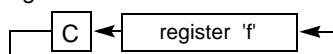
Operation: See description below

Status Affected: C

Encoding: 

0011	01df	ffff
------	------	------

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1,0

Before Instruction

REG1 = 1110 0110

C = 0

After Instruction

REG1 = 1110 0110

W = 1100 1100

C = 1

## RRF Rotate Right f through Carry

Syntax: [label] RRF f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

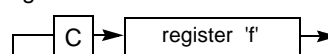
Operation: See description below

Status Affected: C

Encoding: 

0011	00df	ffff
------	------	------

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example: RRF REG1,0

Before Instruction

REG1 = 1110 0110

C = 0

After Instruction

REG1 = 1110 0110

W = 0111 0011

C = 0

## SLEEP Enter SLEEP Mode

Syntax: [label] SLEEP

Operands: None

Operation: 00h → WDT;  
 0 → WDT prescaler; if assigned  
 1 →  $\overline{TO}$ ;  
 0 →  $\overline{PD}$

Status Affected:  $\overline{TO}$ ,  $\overline{PD}$

Encoding: 

0000	0000	0011
------	------	------

Description: Time-out status bit ( $\overline{TO}$ ) is set. The power-down status bit ( $\overline{PD}$ ) is cleared. The WDT and its prescaler are cleared.  
 The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: SLEEP



## 11.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELQ® Demonstration Board

### 11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

### 11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

### 11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

12.6 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T		T
F	Frequency	Time

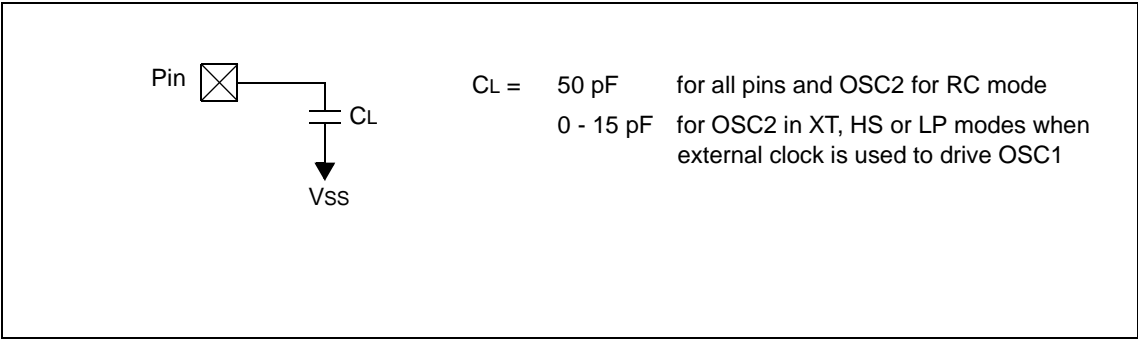
Lowercase letters (pp) and their meanings:

pp		mc	MCLR
2	to	osc	oscillator
ck	CLKOUT	os	OSC1
cy	cycle time	t0	T0CKI
drt	device reset timer	wdt	watchdog timer
io	I/O port		

Uppercase letters and their meanings:

S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

FIGURE 12-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54/55/56/57



## 13.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

### Absolute Maximum Ratings<sup>(†)</sup>

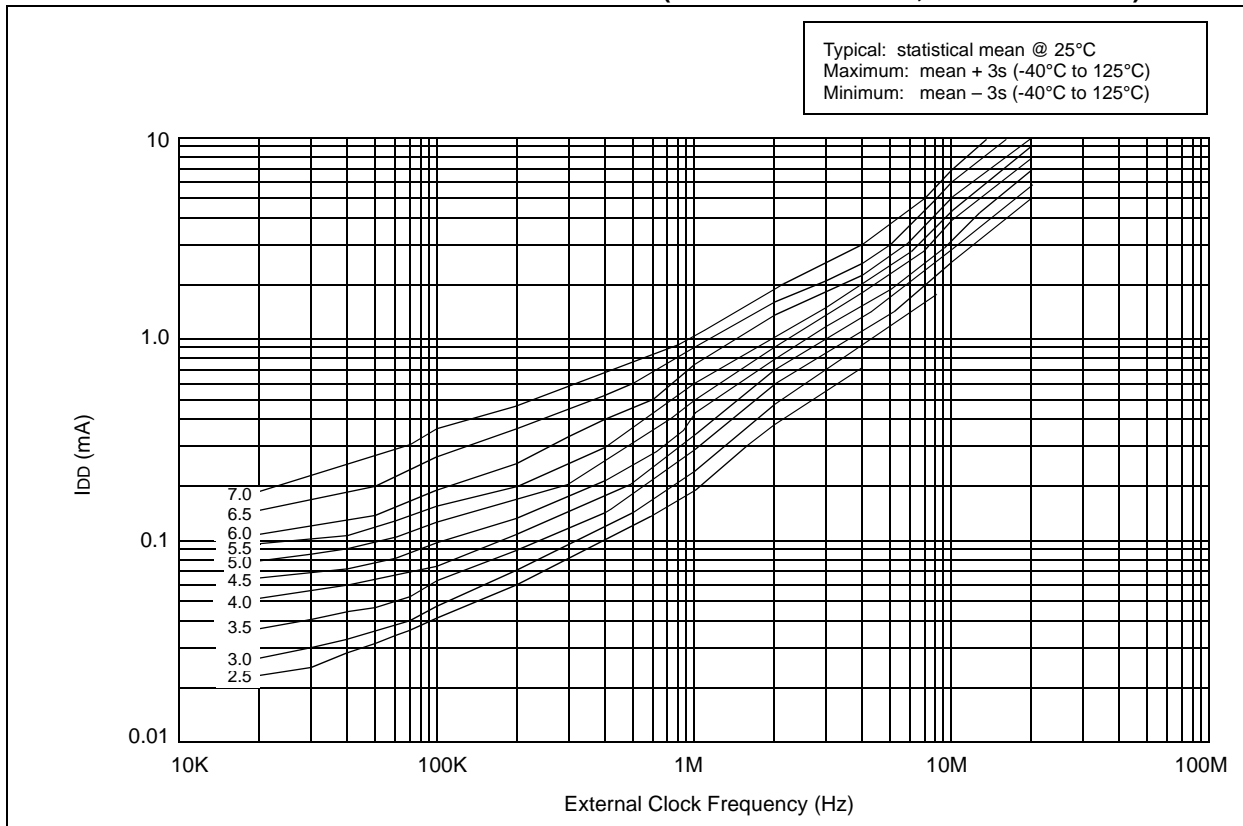
Ambient Temperature under bias .....	–55°C to +125°C
Storage Temperature .....	–65°C to +150°C
Voltage on VDD with respect to VSS .....	0 to +7.5V
Voltage on MCLR with respect to VSS <sup>(1)</sup> .....	0 to +14V
Voltage on all other pins with respect to VSS .....	–0.6V to (VDD + 0.6V)
Total power dissipation <sup>(2)</sup> .....	800 mW
Max. current out of VSS pin .....	150 mA
Max. current into VDD pin .....	50 mA
Max. current into an input pin (TOCKI only) .....	±500 µA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD) .....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD) .....	±20 mA
Max. output current sunk by any I/O pin .....	25 mA
Max. output current sourced by any I/O pin .....	20 mA
Max. output current sourced by a single I/O port (PORTA or B) .....	40 mA
Max. output current sunk by a single I/O port (PORTA or B) .....	50 mA

**Note 1:** Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a low level to the MCLR pin rather than pulling this pin directly to VSS.

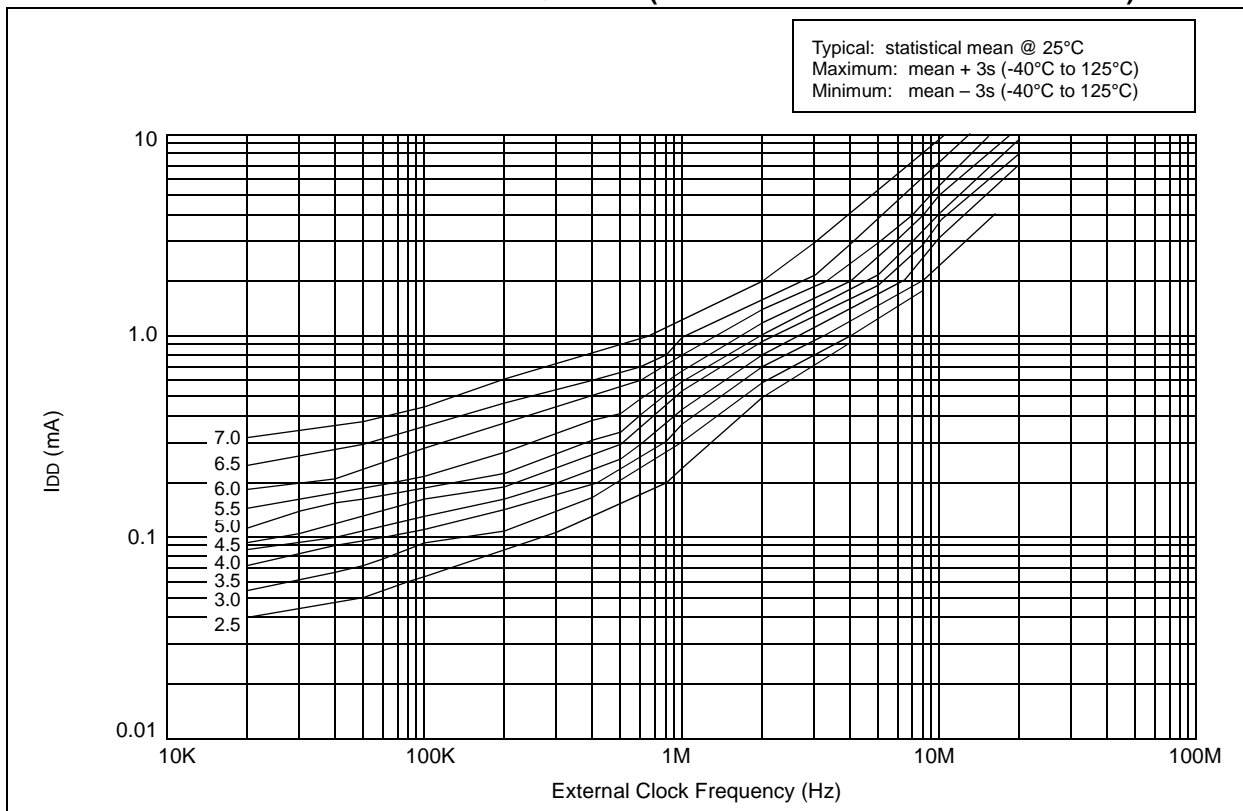
**2:** Power Dissipation is calculated as follows:  $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**FIGURE 14-13: MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK, -40°C TO +85°C)**



**FIGURE 14-14: MAXIMUM  $I_{DD}$  vs. FREQUENCY (EXTERNAL CLOCK -55°C TO +125°C)**



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**TABLE 14-2: INPUT CAPACITANCE FOR  
PIC16C54/56**

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

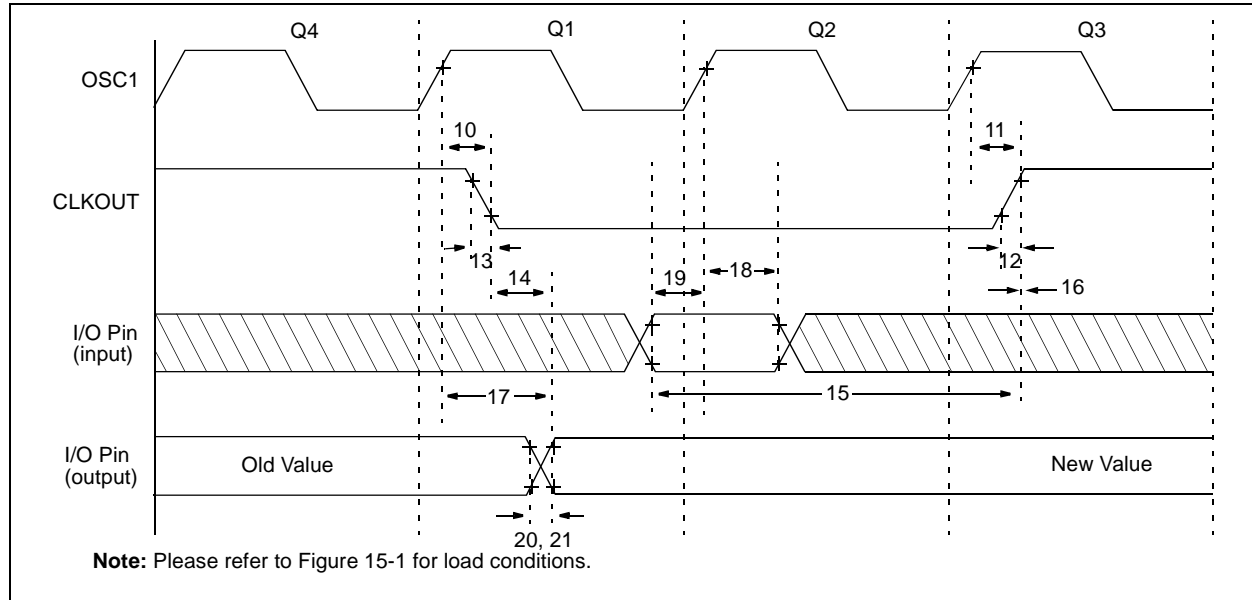
All capacitance values are typical at 25°C. A part-to-part variation of  $\pm 25\%$  (three standard deviations) should be taken into account.

**TABLE 14-3: INPUT CAPACITANCE FOR  
PIC16C55/57**

Pin	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
T0CKI	4.5	3.5

All capacitance values are typical at 25°C. A part-to-part variation of  $\pm 25\%$  (three standard deviations) should be taken into account.

**FIGURE 15-3: CLKOUT AND I/O TIMING - PIC16C54A**



**TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A**

<b>Standard Operating Conditions (unless otherwise specified)</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial - PIC16LV54A-02I $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended						
<b>AC Characteristics</b>						
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ <sup>(1)</sup>	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ <sup>(1)</sup>	—	15	30**	ns
12	TckR	CLKOUT rise time <sup>(1)</sup>	—	5.0	15**	ns
13	TckF	CLKOUT fall time <sup>(1)</sup>	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid <sup>(1)</sup>	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ <sup>(1)</sup>	$0.25 \text{ TCY} + 30^*$	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ <sup>(1)</sup>	$0^*$	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid <sup>(2)</sup>	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time <sup>(2)</sup>	—	10	25**	ns
21	TioF	Port output fall time <sup>(2)</sup>	—	10	25**	ns

\* These parameters are characterized but not tested.

\*\* These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Please refer to Figure 15-1 for load conditions.

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FIGURE 16-5: TYPICAL I<sub>PD</sub> vs. V<sub>DD</sub>, WATCHDOG DISABLED (25°C)

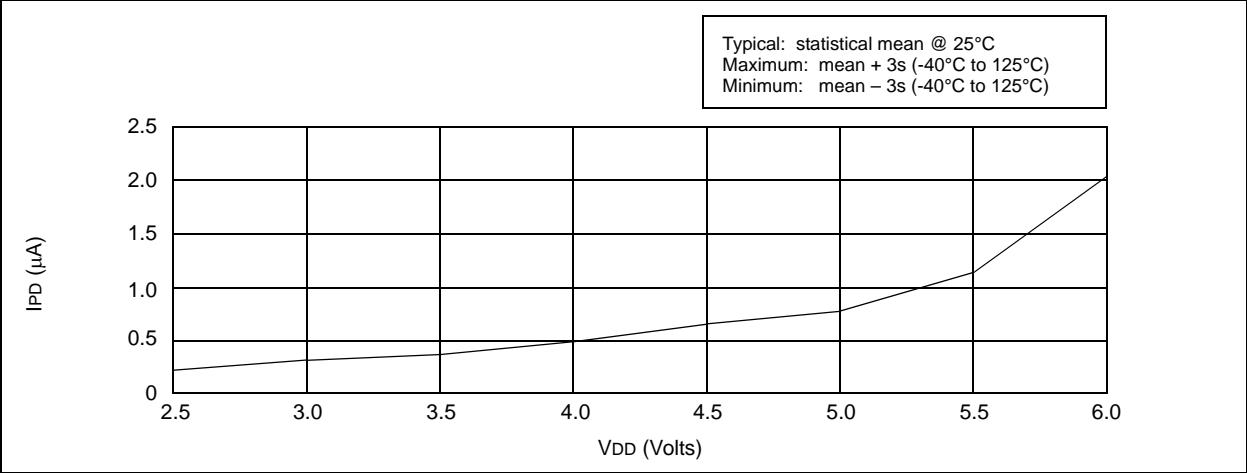
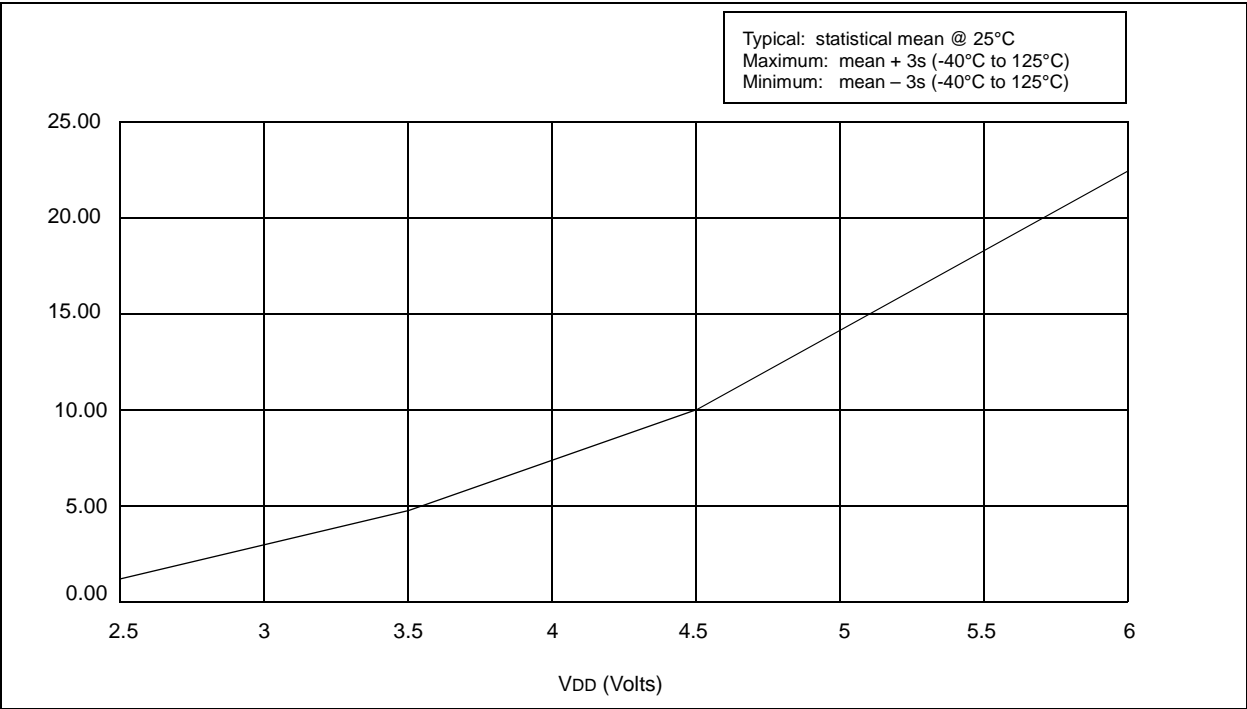
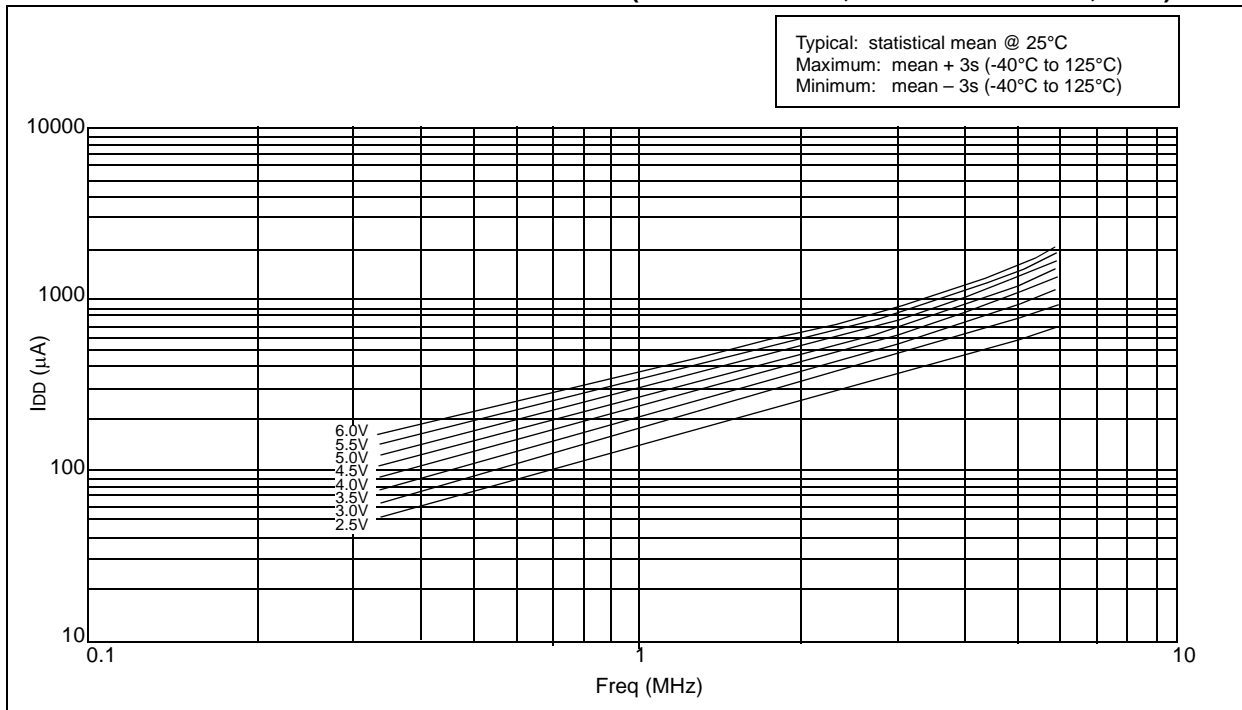


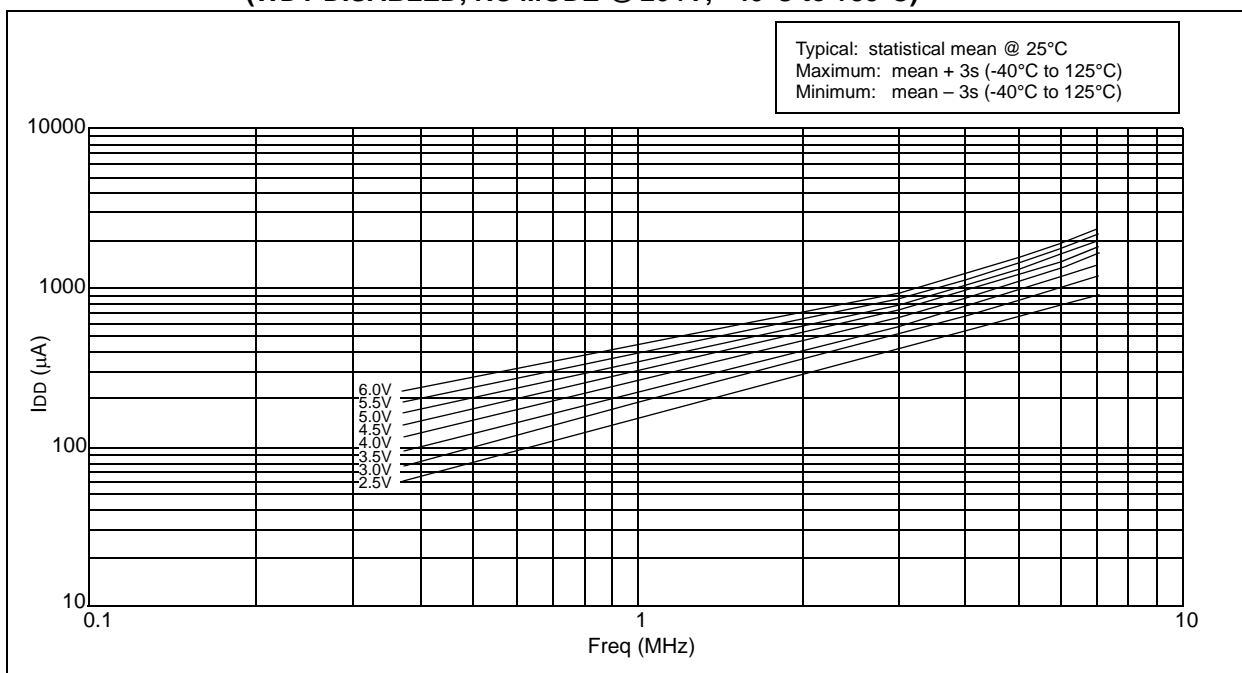
FIGURE 16-6: TYPICAL I<sub>PD</sub> vs. V<sub>DD</sub>, WATCHDOG ENABLED (25°C)



**FIGURE 16-10: TYPICAL  $I_{DD}$  vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)**

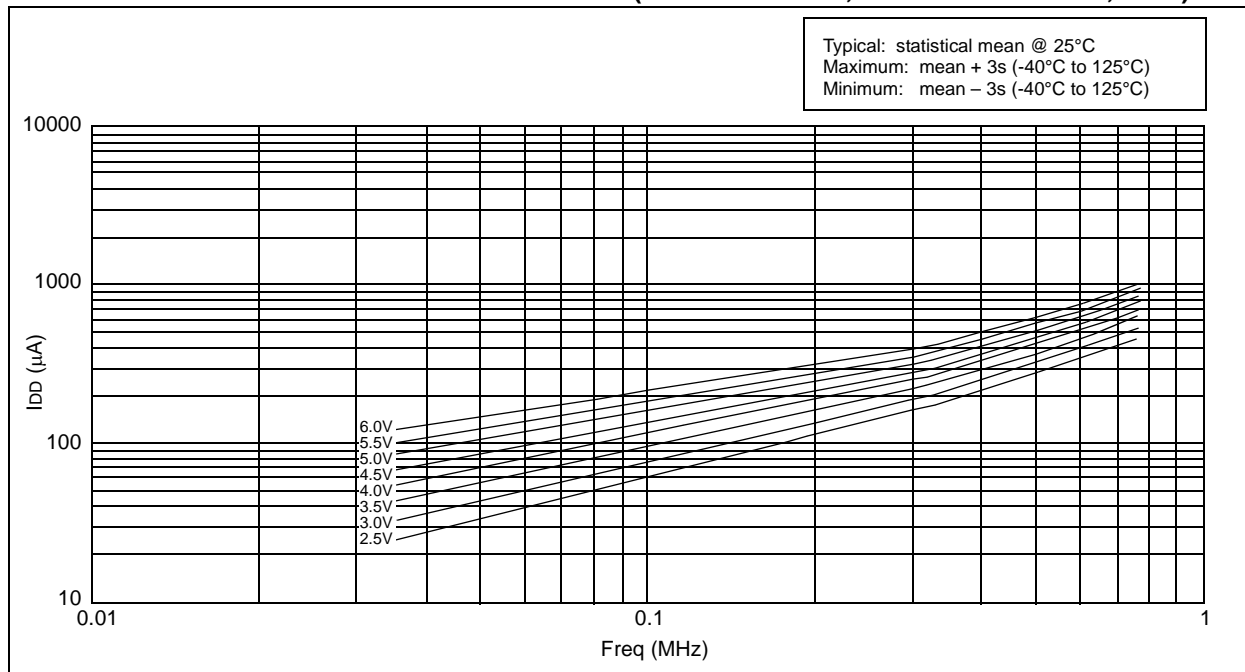


**FIGURE 16-11: MAXIMUM  $I_{DD}$  vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, -40°C to +85°C)**

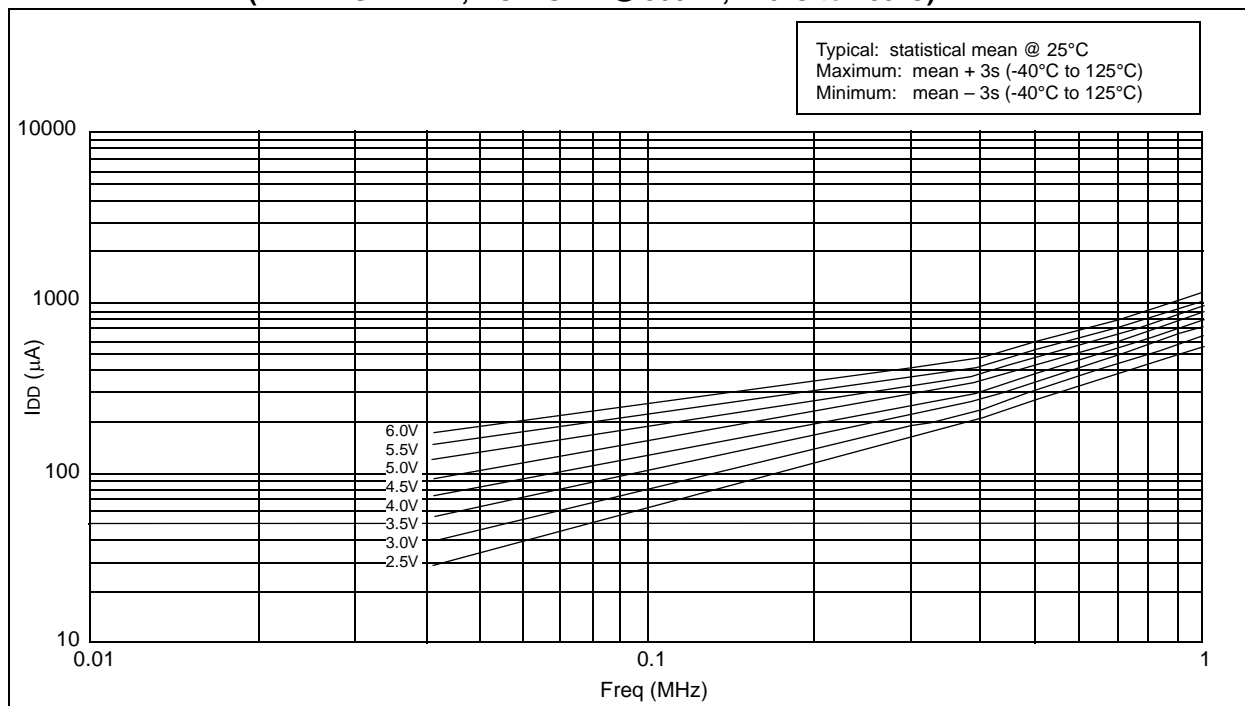




**FIGURE 16-14: TYPICAL  $I_{DD}$  vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)**



**FIGURE 16-15: MAXIMUM  $I_{DD}$  vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, -40°C to +85°C)**



# PIC16C5X

## 17.3 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature				
			0°C ≤ TA ≤ +70°C for commercial				
			-40°C ≤ TA ≤ +85°C for industrial				
			-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	VIL	<b>Input Low Voltage</b> I/O Ports I/O Ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VSS VSS VSS VSS VSS VSS	— — — — — —	0.8 V 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V V	4.5V < VDD ≤ 5.5V Otherwise  RC mode only <sup>(3)</sup> XT, HS and LP modes
D040	VIH	<b>Input High Voltage</b> I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.25 VDD+0.8 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD	— — — — — —	VDD VDD VDD VDD VDD VDD	V V V V V V	4.5V < VDD ≤ 5.5V Otherwise  RC mode only <sup>(3)</sup> XT, HS and LP modes
D050	VHYS	<b>Hysteresis of Schmitt Trigger inputs</b>	0.15 VDD*	—	—	V	
D060	IIL	<b>Input Leakage Current<sup>(1,2)</sup></b> I/O ports  MCLR MCLR T0CKI OSC1	-1.0  -5.0  -3.0 -3.0	0.5  — 0.5 0.5 0.5	+1.0  +5.0 +3.0 +3.0 —	μA  μA μA μA μA	<b>For VDD ≤ 5.5V:</b> VSS ≤ VPIN ≤ VDD, pin at hi-impedance VPIN = VSS +0.25V VPIN = VDD VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
D080	VOL	<b>Output Low Voltage</b> I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC mode only
D090	VOH	<b>Output High Voltage<sup>(2)</sup></b> I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7	— —	— —	V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC mode only

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPIN pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

FIGURE 18-6: TYPICAL  $I_{PD}$  vs.  $V_{DD}$ , WATCHDOG ENABLED (25°C)

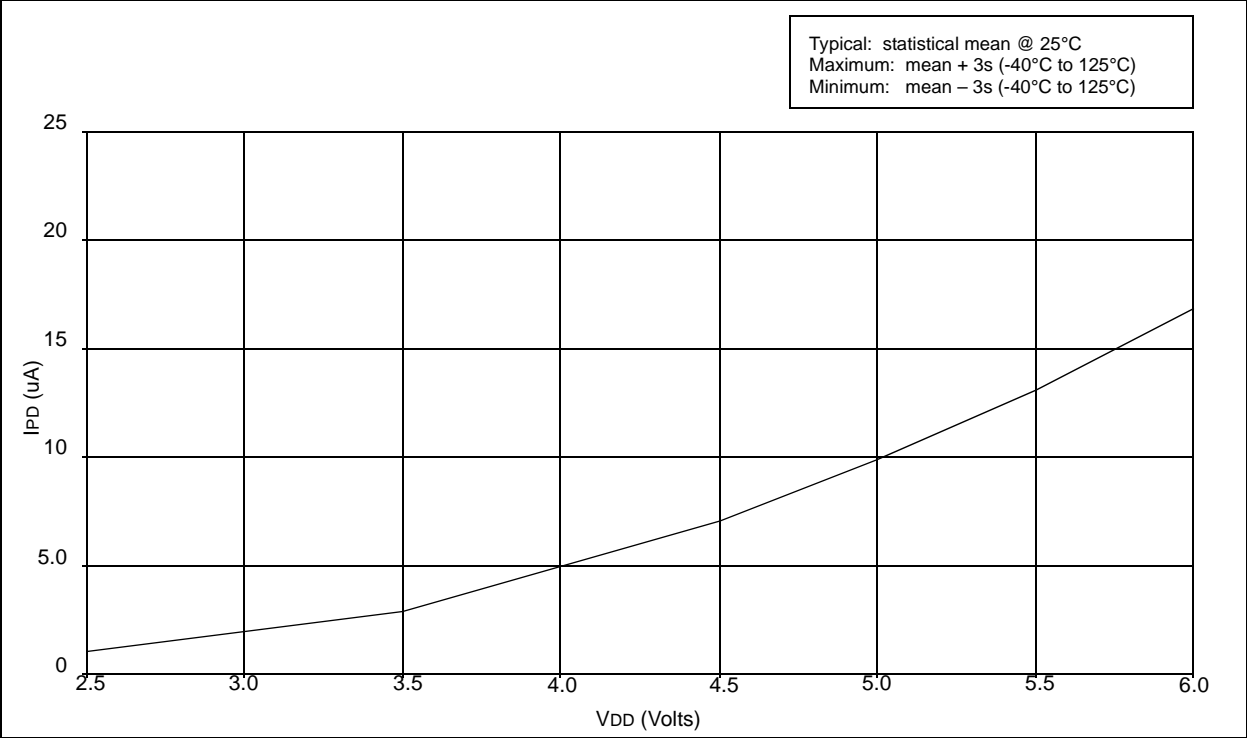


FIGURE 18-7: TYPICAL  $I_{PD}$  vs.  $V_{DD}$ , WATCHDOG ENABLED (-40°C, 85°C)

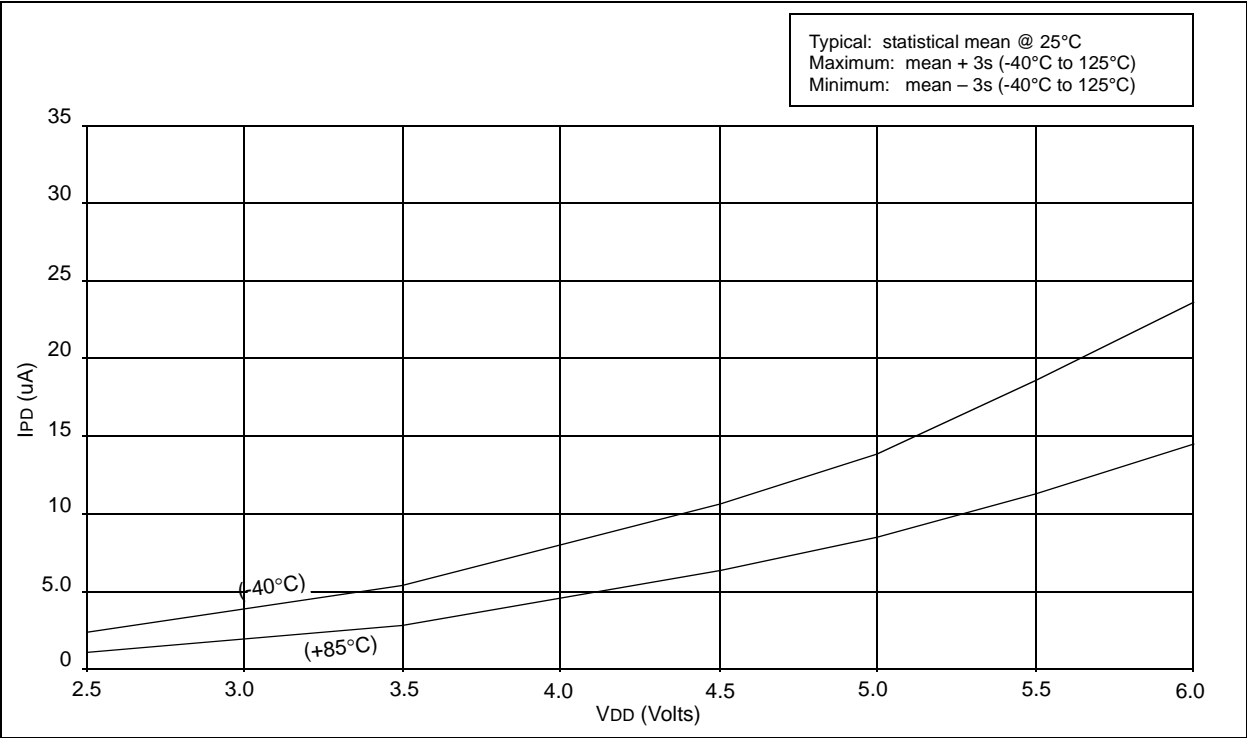


FIGURE 20-2: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)

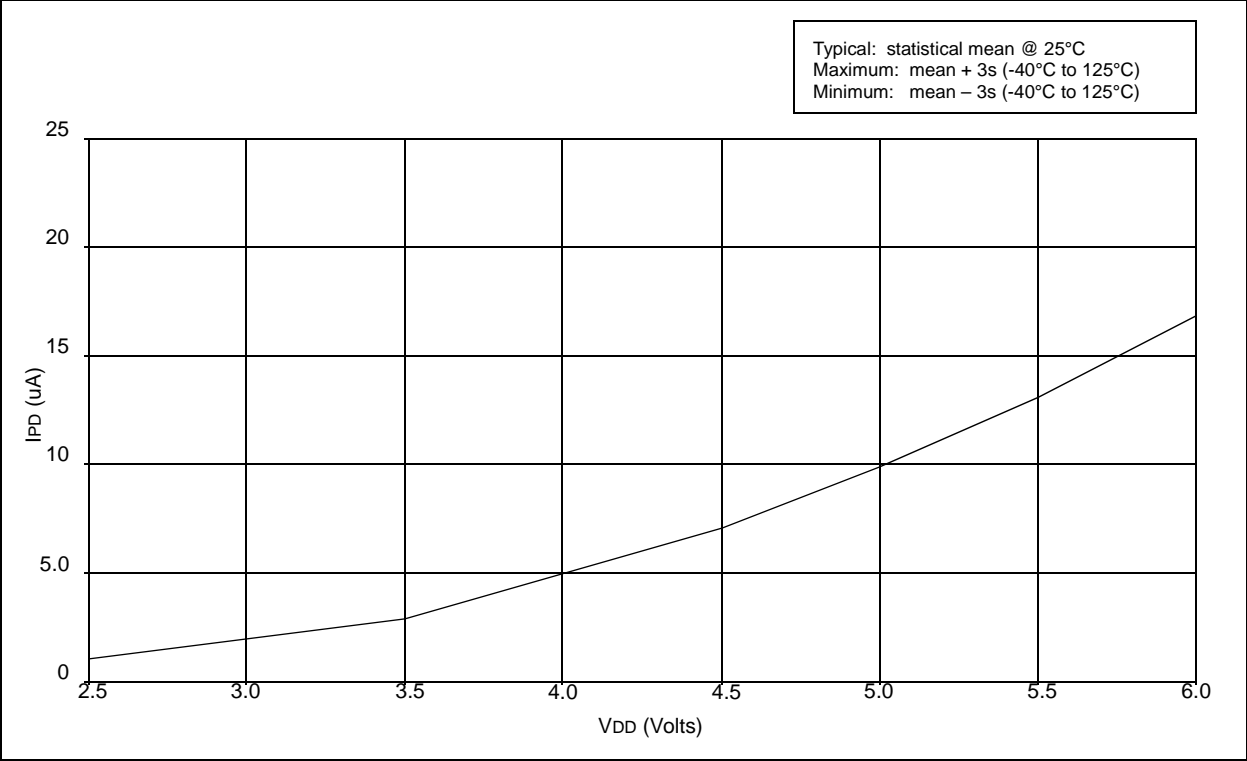
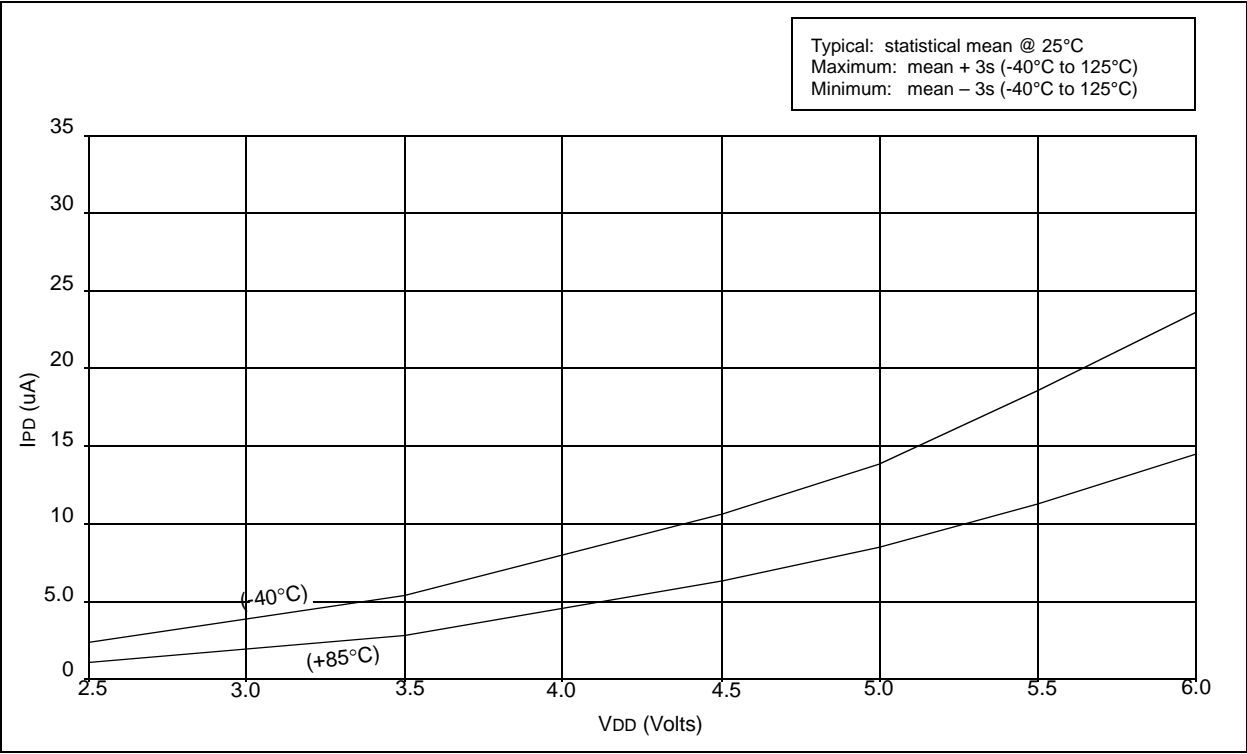
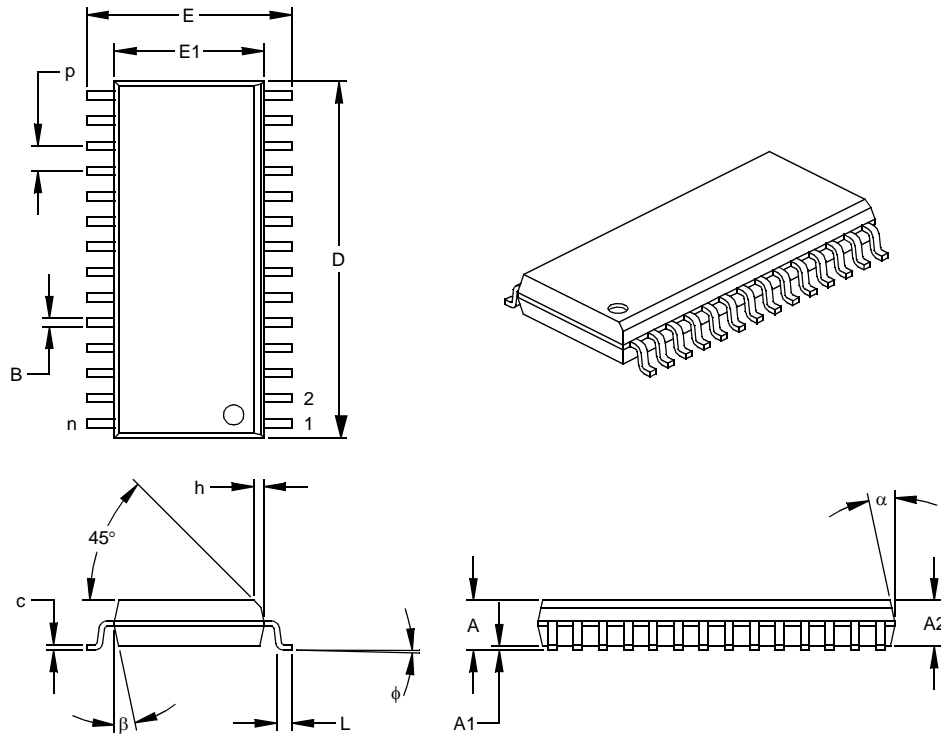


FIGURE 20-3: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (-40°C, 85°C)



## 28-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-052