What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc55a-04i-so

PIC16C5X

8-Bit EPROM/ROM-Based CMOS Microcontrollers

1.0   GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low cost, high performance, 8-bit fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches which take two cycles. The PIC16C5X delivers performance in an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external RESET circuitry. There are four oscillator configurations to choose from, including the power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and Code Protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1   Applications

The PIC16C5X series fits perfectly in applications ranging from high speed automotive and appliance motor control to low power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low cost, low power, high performance ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, co-processor applications).

NOTES:

PIC16C5X

TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	SOIC	SSOP			
RA0	6	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	7	6	I/O	TTL	
RA2	8	8	7	I/O	TTL	
RA3	9	9	8	I/O	TTL	
RB0	10	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	11	10	I/O	TTL	
RB2	12	12	11	I/O	TTL	
RB3	13	13	12	I/O	TTL	
RB4	14	14	13	I/O	TTL	
RB5	15	15	15	I/O	TTL	
RB6	16	16	16	I/O	TTL	
RB7	17	17	17	I/O	TTL	
RC0	18	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	19	I/O	TTL	
RC2	20	20	20	I/O	TTL	
RC3	21	21	21	I/O	TTL	
RC4	22	22	22	I/O	TTL	
RC5	23	23	23	I/O	TTL	
RC6	24	24	24	I/O	TTL	
RC7	25	25	25	I/O	TTL	
T0CKI	1	1	2	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
$\overline{\text{MCLR}}$	28	28	28	I	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
OSC1/CLKIN	27	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	2	2	3,4	P	—	Positive supply for logic and I/O pins.
Vss	4	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	3,5	—	—	—	Unused, do not connect.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

Preliminary

NOTES:

5.0   RESET

PIC16C5X devices may be RESET in one of the following ways:

- Power-On Reset (POR)
- $\overline{MCLR}$ Reset (normal operation)
- $\overline{MCLR}$ Wake-up Reset (from SLEEP)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from SLEEP)

Table 5-1 shows these RESET conditions for the PCL and STATUS registers.

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-On Reset (POR), $\overline{MCLR}$ or WDT Reset. A $\overline{MCLR}$ or WDT wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

The $\overline{TO}$ and $\overline{PD}$ bits (STATUS <4:3>) are set or cleared depending on the different RESET conditions (Table 5-1). These bits may be used to determine the nature of the RESET.

Table 5-3 lists a full description of RESET states of all registers. Figure 5-1 shows a simplified block diagram of the On-chip Reset circuit.

TABLE 5-1:   STATUS BITS AND THEIR SIGNIFICANCE

Condition	$\overline{TO}$	$\overline{PD}$
Power-On Reset	1	1
$\overline{MCLR}$ Reset (normal operation)	u	u
$\overline{MCLR}$ Wake-up (from SLEEP)	1	0
WDT Reset (normal operation)	0	1
WDT Wake-up (from SLEEP)	0	0

Legend: u = unchanged, x = unknown, — = unimplemented read as '0'.

TABLE 5-2:   SUMMARY OF REGISTERS ASSOCIATED WITH RESET

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on $\overline{MCLR}$ and WDT Reset
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, q = see Table 5-1 for possible values.

PIC16C5X

IORLW	Inclusive OR literal with W
Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. (k) $\rightarrow$ (W)
Status Affected:	Z

Encoding:

1101	kkkk	kkkk

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `IORLW   0x35`

    Before Instruction
       W   =   0x9A
    After Instruction
       W   =   0xBF
       Z   =   0

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W).OR. (f) $\rightarrow$ (dest)
Status Affected:	Z

Encoding:

0001	00df	ffff

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: `IORWF       RESULT, 0`

    Before Instruction
       RESULT   =   0x13
       W   =   0x91
    After Instruction
       RESULT   =   0x13
       W   =   0x93
       Z   =   0

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) $\rightarrow$ (dest)
Status Affected:	Z

Encoding:

0010	00df	ffff

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example: `MOVF    FSR,   0`

    After Instruction
       W   =   value in FSR register

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k $\rightarrow$ (W)
Status Affected:	None

Encoding:

1100	kkkk	kkkk

Description: The eight bit literal 'k' is loaded into the W register.

Words: 1

Cycles: 1

Example: `MOVLW   0x5A`

    After Instruction
       W   =   0x5A

PIC16C5X

12.3   DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D001	VDD	**Supply Voltage** PIC16C5X-RCE PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-LPE	3.25 3.25 4.5 4.5 2.5	— — — — —	6.0 6.0 5.5 5.5 6.0	V V V V V	
D002	VDR	**RAM Data Retention Voltage**[1]	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current**[2] PIC16C5X-RCE[3] PIC16C5X-XTE PIC16C5X-10E PIC16C5X-HSE PIC16C5X-HSE PIC16C5X-LPE	— — — — — —	1.8 1.8 4.8 4.8 9.0 19	3.3 3.3 10 10 20 55	mA mA mA mA mA μA	FOSC = 4 MHz, VDD = 5.5V FOSC = 4 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V FOSC = 32 kHz, VDD = 3.25V, WDT disabled
D020	IPD	**Power-down Current**[2]	— —	5.0 0.8	22 18	μA μA	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

*   These parameters are characterized but not tested.

†   Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial)
PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)			**Standard Operating Conditions** (unless otherwise specified) Operating Temperature $\quad$ 0°C $\leq$ TA $\leq$ +70°C for commercial $\quad$ −40°C $\leq$ TA $\leq$ +85°C for industrial				
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			**Standard Operating Conditions** (unless otherwise specified) Operating Temperature $\quad$ 0°C $\leq$ TA $\leq$ +70°C for commercial $\quad$ −40°C $\leq$ TA $\leq$ +85°C for industrial				
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IPD	**Power-down Current**[2]					
D006		PIC16LCR54A-Commercial	—	1.0	6.0	μA	VDD = 2.5V, WDT disabled
			—	2.0	8.0*	μA	VDD = 4.0V, WDT disabled
			—	3.0	15	μA	VDD = 6.0V, WDT disabled
			—	5.0	25	μA	VDD = 6.0V, WDT enabled
D006A		PIC16CR54A-Commercial	—	1.0	6.0	μA	VDD = 2.5V, WDT disabled
			—	2.0	8.0*	μA	VDD = 4.0V, WDT disabled
			—	3.0	15	μA	VDD = 6.0V, WDT disabled
			—	5.0	25	μA	VDD = 6.0V, WDT enabled
D007		PIC16LCR54A-Industrial	—	1.0	8.0	μA	VDD = 2.5V, WDT disabled
			—	2.0	10*	μA	VDD = 4.0V, WDT disabled
			—	3.0	20*	μA	VDD = 4.0V, WDT enabled
			—	3.0	18	μA	VDD = 6.0V, WDT disabled
			—	5.0	45	μA	VDD = 6.0V, WDT enabled
D007A		PIC16CR54A-Industrial	—	1.0	8.0	μA	VDD = 2.5V, WDT disabled
			—	2.0	10*	μA	VDD = 4.0V, WDT disabled
			—	3.0	20*	μA	VDD = 4.0V, WDT enabled
			—	3.0	18	μA	VDD = 6.0V, WDT disabled
			—	5.0	45	μA	VDD = 6.0V, WDT enabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

* $\quad$ These parameters are characterized but not tested.

† $\quad$ Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

$\quad$ a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

$\quad$ b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1	TOSC	External CLKIN Period[(1)]	250	—	—	ns	XT OSC mode
			250	—	—	ns	HS OSC mode (04)
			100	—	—	ns	HS OSC mode (10)
			50	—	—	ns	HS OSC mode (20)
			5.0	—	—	μs	LP OSC mode
		Oscillator Period[(1)]	250	—	—	ns	RC OSC mode
			250	—	10,000	ns	XT OSC mode
			250	—	250	ns	HS OSC mode (04)
			100	—	250	ns	HS OSC mode (10)
			50	—	250	ns	HS OSC mode (20)
			5.0	—	200	μs	LP OSC mode
2	Tcy	Instruction Cycle Time[(2)]	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

PIC16C5X

15.3 DC Characteristics: PIC16LV54A-02 (Commercial)
PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)							Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-20°C \leq T_A \leq +85°C$ for industrial
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	V_{DD}	**Supply Voltage** RC and XT modes	2.0	—	3.8	V	
D002	V_{DR}	**RAM Data Retention Voltage**[1]	—	1.5*	—	V	Device in SLEEP mode
D003	V_{POR}	**V_{DD} Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	S_{VDD}	**V_{DD} Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	I_{DD}	**Supply Current**[2] RC[3] and XT modes LP mode, Commercial LP mode, Industrial	— — —	0.5 11 14	— 27 35	mA µA µA	F_{OSC} = 2.0 MHz, V_{DD} = 3.0V F_{OSC} = 32 kHz, V_{DD} = 2.5V WDT disabled F_{OSC} = 32 kHz, V_{DD} = 2.5V WDT disabled
D020	I_{PD}	**Power-down Current**[2,4] Commercial Commercial Industrial Industrial	— — — —	2.5 0.25 3.5 0.3	12 4.0 14 5.0	µA µA µA µA	V_{DD} = 2.5V, WDT enabled V_{DD} = 2.5V, WDT disabled V_{DD} = 2.5V, WDT enabled V_{DD} = 2.5V, WDT disabled

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

  a) The test conditions for all I_{DD} measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

  b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through R_{EXT}. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

4: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

Preliminary

PIC16C5X

15.5   Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

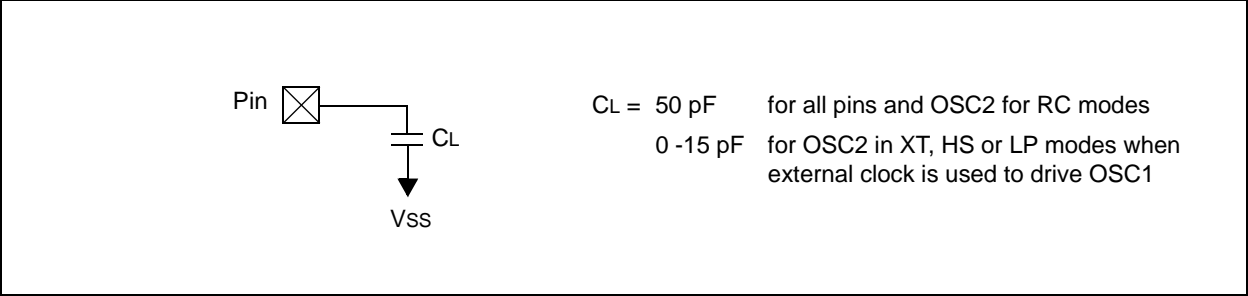| T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 15-1:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54A

$C_L = 50$ pF   for all pins and OSC2 for RC modes

$0 - 15$ pF   for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

Preliminary

15.6 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16C54A
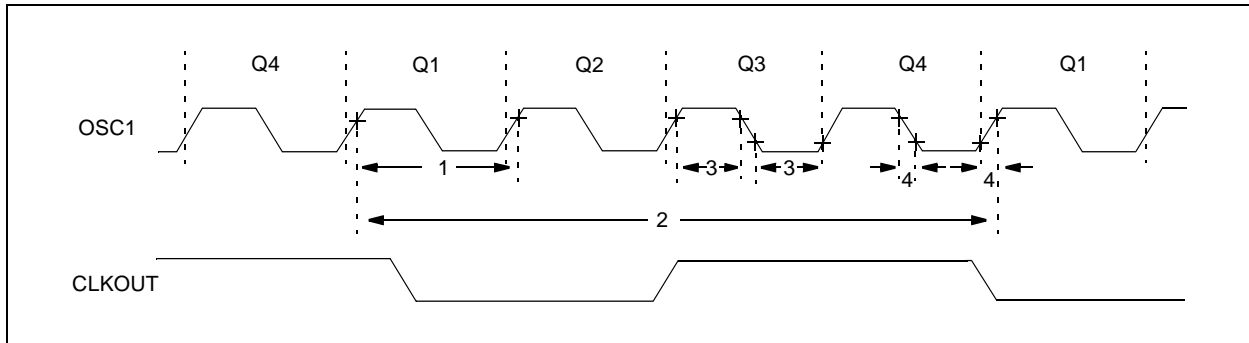
TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I −40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency(1)	DC	—	4.0	MHz	XT OSC mode
			DC	—	2.0	MHz	XT OSC mode (PIC16LV54A)
			DC	—	4.0	MHz	HS OSC mode (04)
			DC	—	10	MHz	HS OSC mode (10)
			DC	—	20	MHz	HS OSC mode (20)
			DC	—	200	kHz	LP OSC mode
		Oscillator Frequency(1)	DC	—	4.0	MHz	RC OSC mode
			DC	—	2.0	MHz	RC OSC mode (PIC16LV54A)
			0.1	—	4.0	MHz	XT OSC mode
			0.1	—	2.0	MHz	XT OSC mode (PIC16LV54A)
			4.0	—	4.0	MHz	HS OSC mode (04)
			4.0	—	10	MHz	HS OSC mode (10)
			4.0	—	20	MHz	HS OSC mode (20)
			5.0	—	200	kHz	LP OSC mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

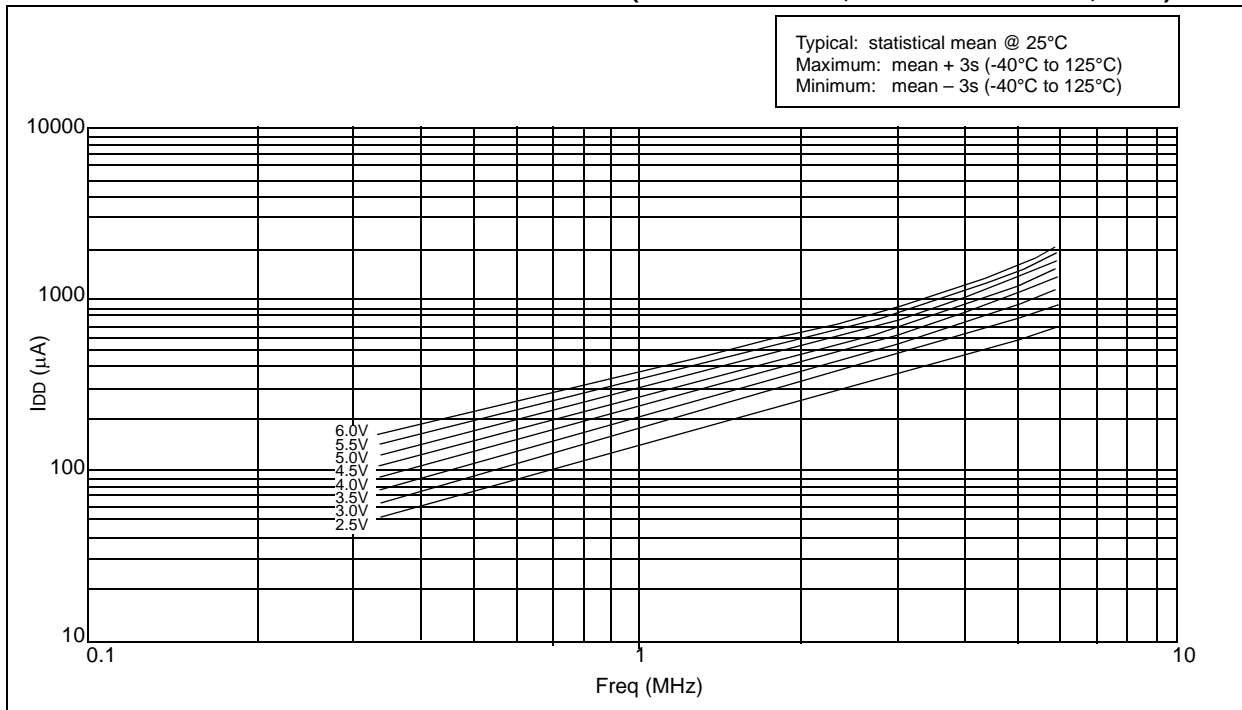**FIGURE 16-10:** **TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 PF, 25°C)**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

IDD (µA)

6.0V
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V

Freq (MHz)

FIGURE 16-11: **MAXIMUM IDD vs. FREQUENCY**
(WDT DISABLED, RC MODE @ 20 PF, –40°C to +85°C)

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

IDD (µA)

6.0V
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V

Freq (MHz)
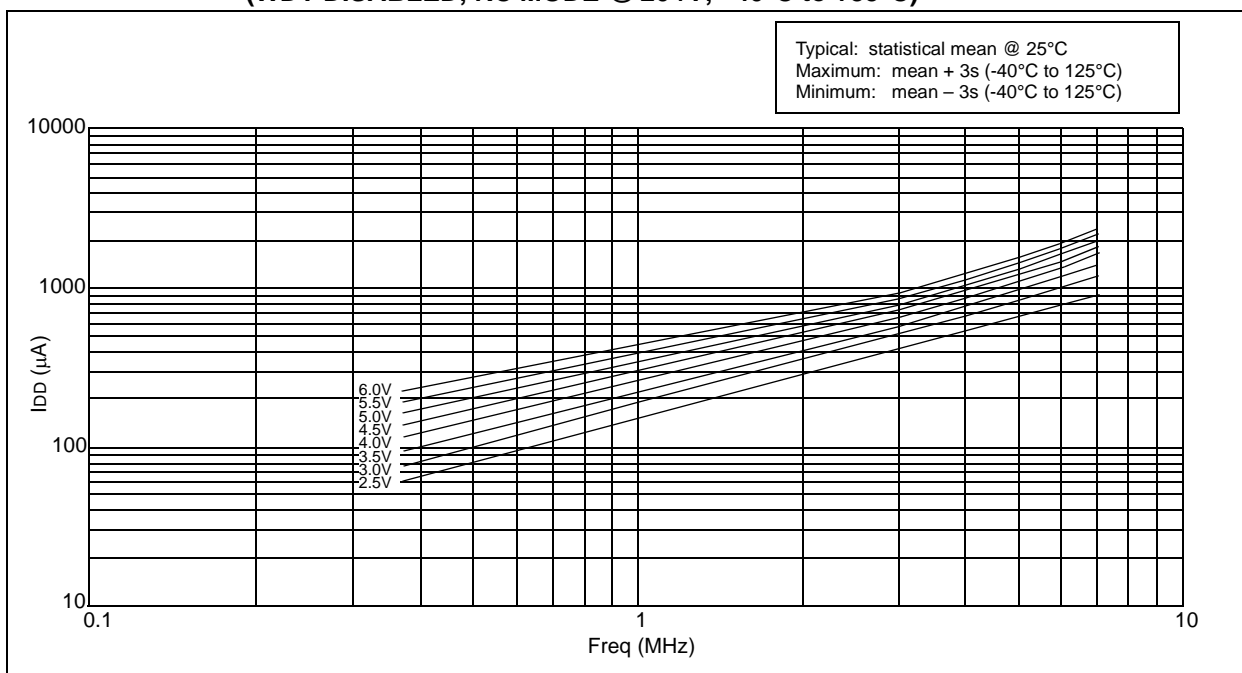
FIGURE 16-22: **PORTA, B AND C I$_{OL}$ vs. V$_{OL}$, V$_{DD}$ = 3V**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
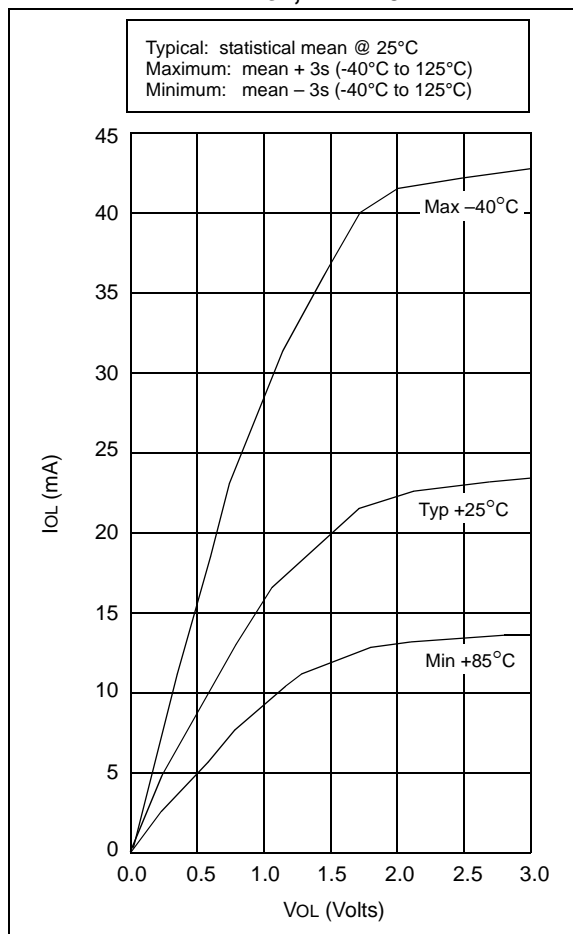
FIGURE 16-23: **PORTA, B AND C I$_{OL}$ vs. V$_{OL}$, V$_{DD}$ = 5V**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
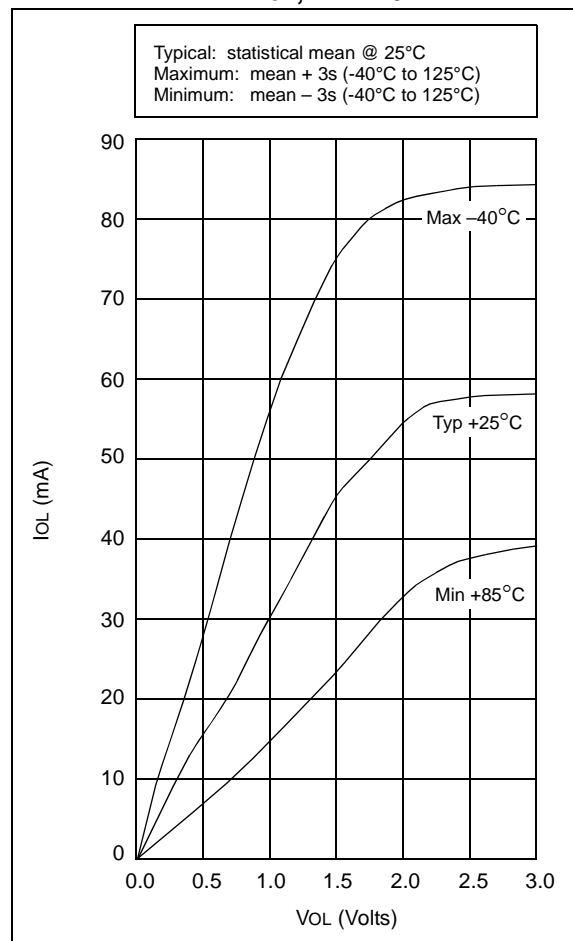
TABLE 16-2: **INPUT CAPACITANCE FOR PIC16C54A/C58A**

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

PIC16C5X

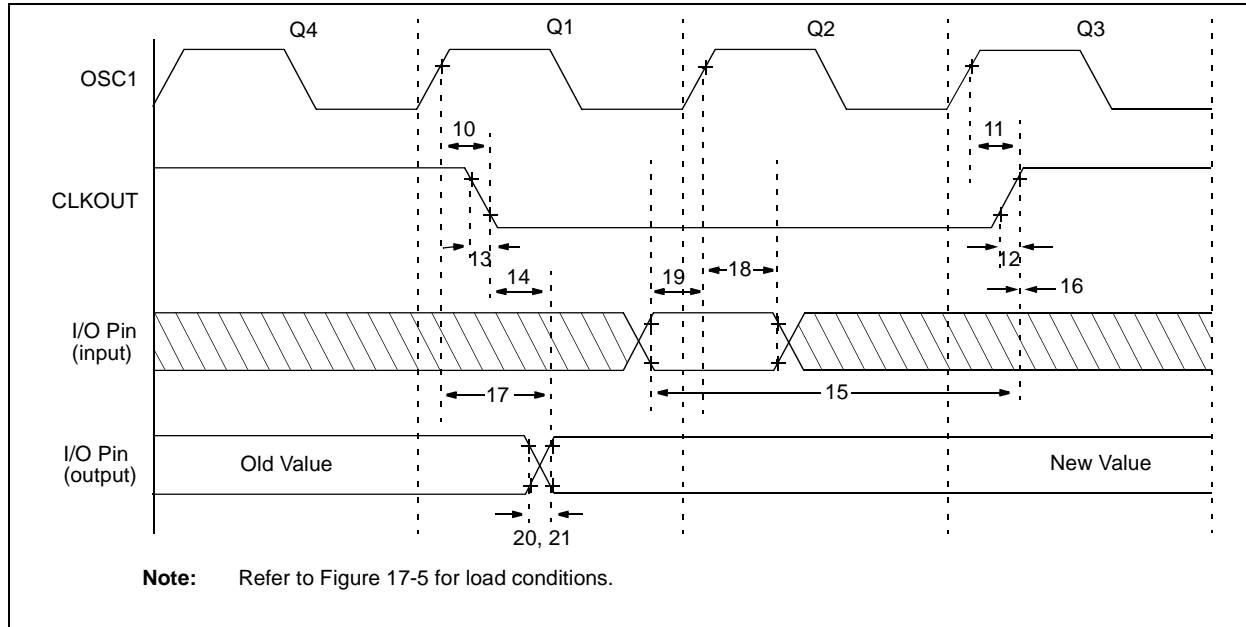**FIGURE 17-7:** CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X

Note: Refer to Figure 17-5 for load conditions.

TABLE 17-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-40°C \leq T_A \leq +85°C$ for industrial $-40°C \leq T_A \leq +125°C$ for extended					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓[1]	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑[1]	—	15	30**	ns
12	TckR	CLKOUT rise time[1]	—	5.0	15**	ns
13	TckF	CLKOUT fall time[1]	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid[1]	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑[1]	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑[1]	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid[2]	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time[2]	—	10	25**	ns
21	TioF	Port output fall time[2]	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.
   2: Refer to Figure 17-5 for load conditions.

Preliminary

FIGURE 19-4:   CLKOUT AND I/O TIMING - PIC16C5X-40

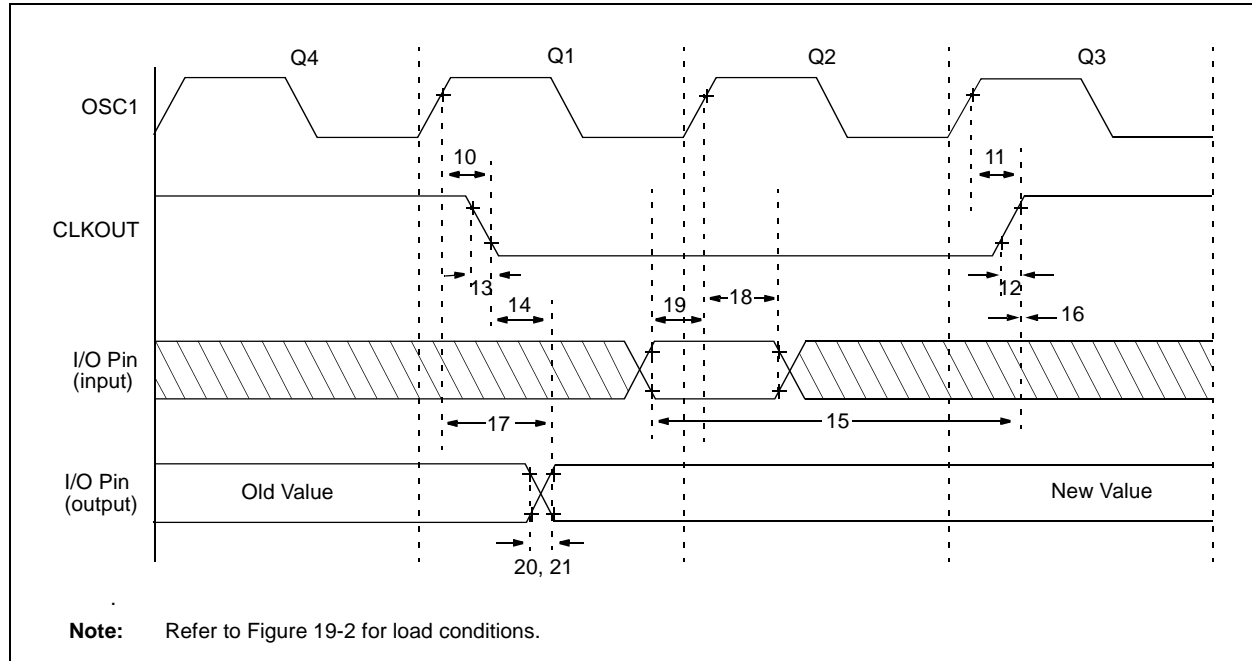Note: Refer to Figure 19-2 for load conditions.

TABLE 19-2:   CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓[1,2]	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑[1,2]	—	15	30**	ns
12	TckR	CLKOUT rise time[1,2]	—	5.0	15**	ns
13	TckF	CLKOUT fall time[1,2]	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid[1,2]	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑[1,2]	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑[1,2]	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid[2]	—	—	100	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time[2]	—	10	25**	ns
21	TioF	Port output fall time[2]	—	10	25**	ns

*   These parameters are characterized but not tested.

**   These parameters are design targets and are not tested. No characterization data available at this time.

†   Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
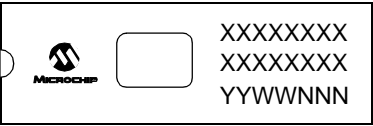
Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.
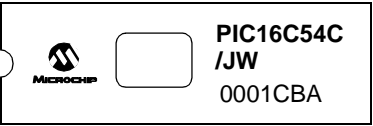   2: Refer to Figure 19-2 for load conditions.
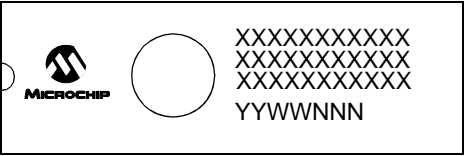
PIC16C5X

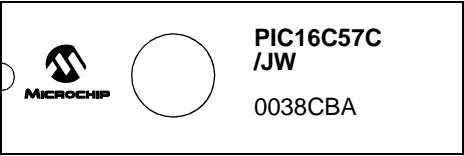## Package Marking Information (Cont'd)

18-Lead CERDIP Windowed

```
Microchip    XXXXXXX
             XXXXXXX
             YYWWNNN
```

Example

```
Microchip    PIC16C54C
             /JW
             0001CBA
```

28-Lead CERDIP Windowed

```
Microchip    XXXXXXXXXX
             XXXXXXXXXX
             XXXXXXXXXX
             YYWWNNN
```

Example

```
Microchip    PIC16C57C
             /JW
             0038CBA
```

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

PIC16C5X

18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
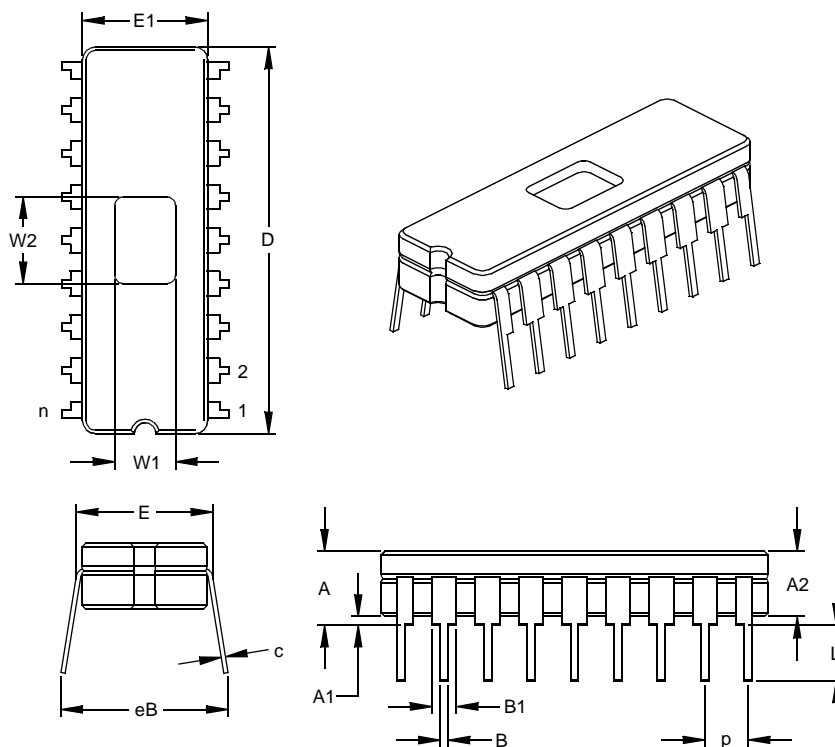
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	B	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-036
Drawing No. C04-010

PIC16C5X

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.

2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.

3. Eliminate any special function register page switching. Redefine data variables to reallocate them.

4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.

5. Change RESET vector to proper value for processor used.

6. Remove any use of the `ADDLW, RETURN` and `SUBLW` instructions.

7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

NOTES: