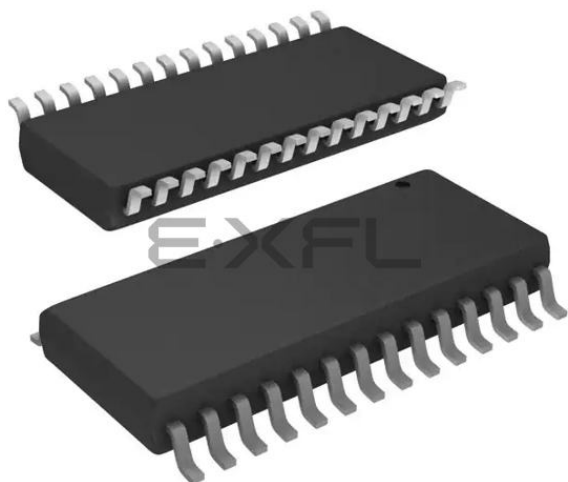




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Details

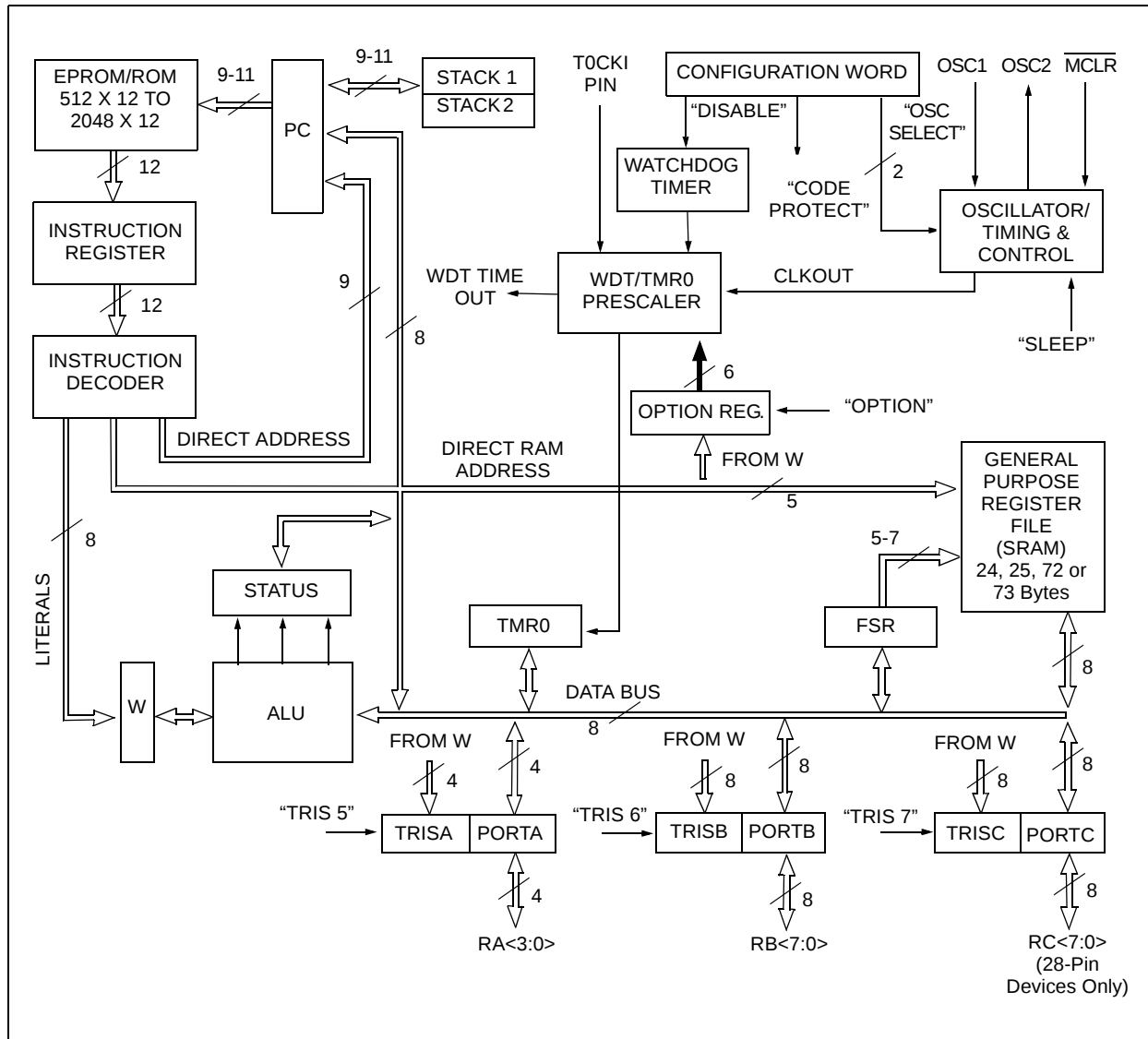
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc55at-04-so

PIC16C5X

NOTES:

PIC16C5X

FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM



4.3 External Crystal Oscillator Circuit

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 4-3 shows an implementation example of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 4-3: EXAMPLE OF EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)

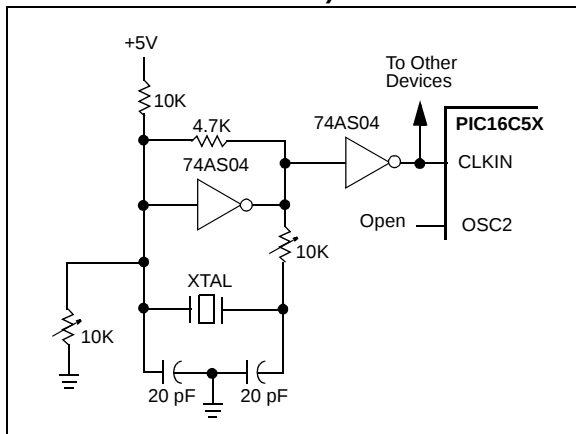
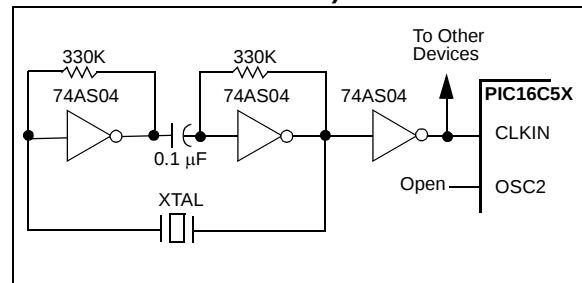


Figure 4-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 4-4: EXAMPLE OF EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



PIC16C5X

FIGURE 5-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO VDD)

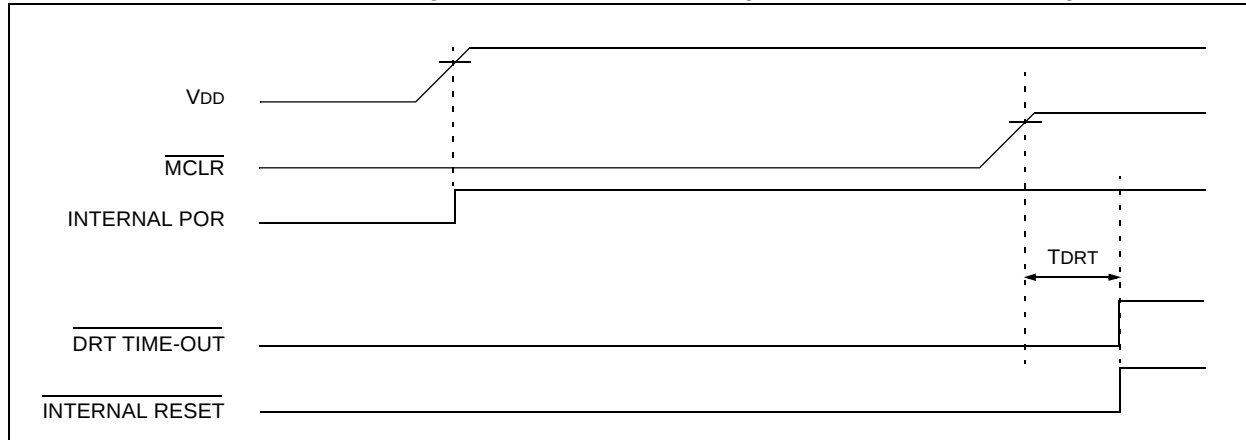


FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD): FAST VDD RISE TIME

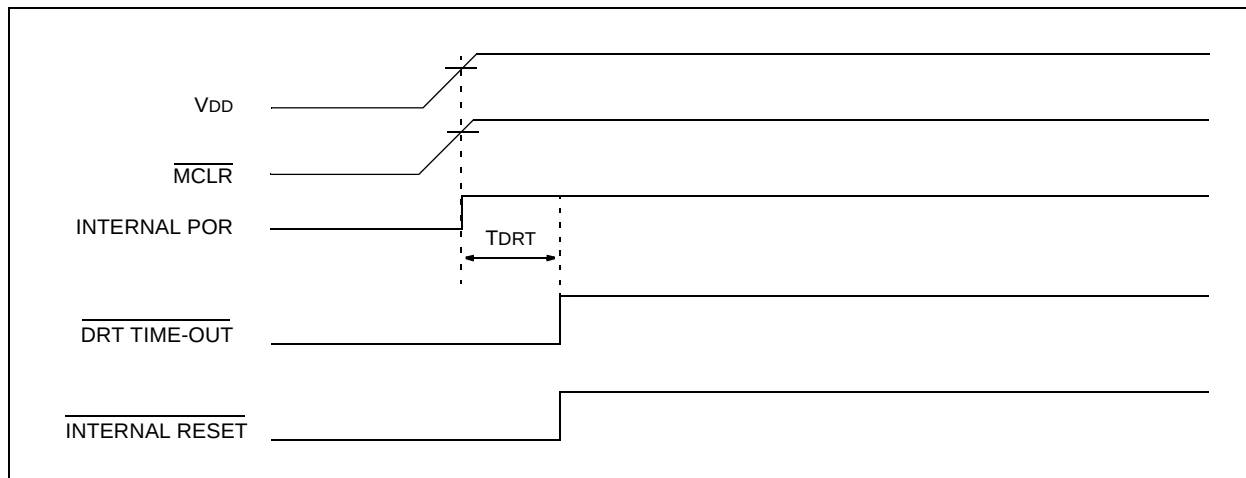
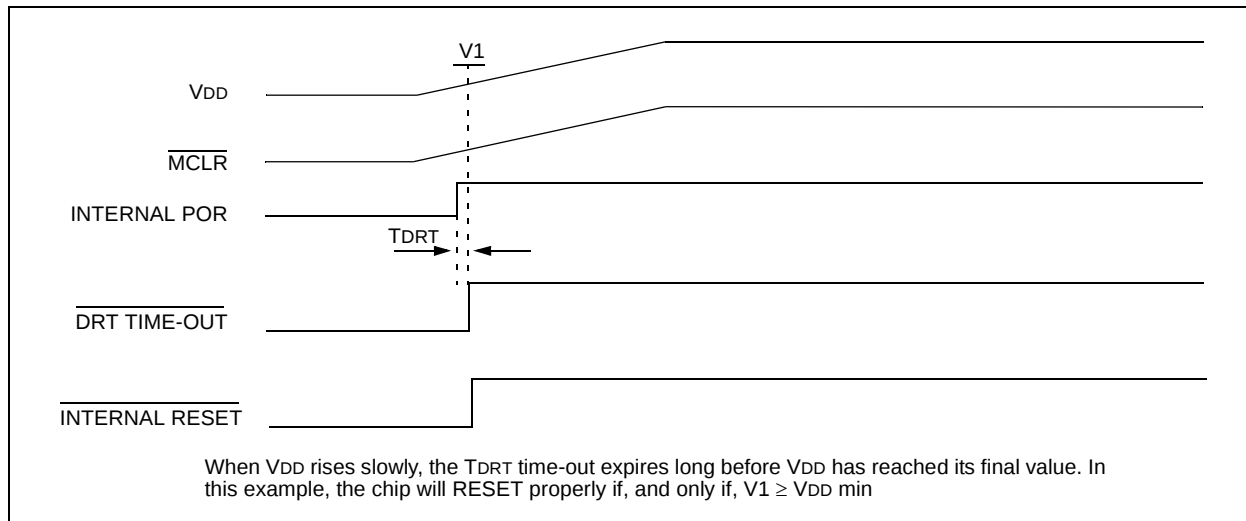


FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD): SLOW VDD RISE TIME



PIC16C5X

6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 6-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	35
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	30
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32
01h	TMR0	Timer0 Module Register								xxxx xxxx	38
02h ⁽¹⁾	PCL	Low order 8 bits of PC								1111 1111	31
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	29
04h	FSR	Indirect data memory address pointer								1xxx xxxx ⁽³⁾	32
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	35
07h ⁽²⁾	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	35

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

3: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for $\overline{MCLR}$ and WDT Reset, the value is 111u uuuu.

8.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1,x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

8.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 8-1: CHANGING PRESCALER (TIMER0→WDT)

```
CLRWDT          ;Clear WDT
CLRF    TMR0     ;Clear TMR0 & Prescaler
MOVLW  B'00xx1111' ;Last 3 instructions in
                    this example
OPTION         ;are required only if
                ;desired
CLRWDT          ;PS<2:0> are 000 or
                ;001
MOVLW  B'00xx1xxx' ;Set Prescaler to
OPTION         ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 8-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT          ;Clear WDT and
                ;prescaler
MOVLW  B'xxxx0xxx' ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

PIC16C5X

9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16C54C, PIC16CR54C, PIC16C55A, PIC16C56A, PIC16CR56A, PIC16C57C, PIC16CR57C,

PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit 11										bit 0	

bit 11-3: **CP**: Code Protection Bit

1 = Code protection off
0 = Code protection on

bit 2: **WDTE**: Watchdog timer enable bit

1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection Bit

00 = LP oscillator
01 = XT oscillator
10 = HS oscillator
11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

PIC16C5X

IORLW **Inclusive OR literal with W**

Syntax: `[label] IORLW k`

Operands: $0 \leq k \leq 255$

Operation: $(W) .OR. (k) \rightarrow (W)$

Status Affected: Z

Encoding:

1101	kkkk	kkkk
------	------	------

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `IORLW 0x35`

Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 0

IORWF **Inclusive OR W with f**

Syntax: `[label] IORWF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .OR. (f) \rightarrow (dest)$

Status Affected: Z

Encoding:

0001	00df	ffff
------	------	------

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: `IORWF            RESULT, 0`

Before Instruction
RESULT = 0x13
W = 0x91
After Instruction
RESULT = 0x13
W = 0x93
Z = 0

MOVF **Move f**

Syntax: `[label] MOVF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) \rightarrow (dest)$

Status Affected: Z

Encoding:

0010	00df	ffff
------	------	------

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example: `MOVF    FSR,    0`

After Instruction
W = value in FSR register

MOVLW **Move Literal to W**

Syntax: `[label] MOVLW k`

Operands: $0 \leq k \leq 255$

Operation: $k \rightarrow (W)$

Status Affected: None

Encoding:

1100	kkkk	kkkk
------	------	------

Description: The eight bit literal 'k' is loaded into the W register.

Words: 1

Cycles: 1

Example: `MOVLW 0x5A`

After Instruction
W = 0x5A

PIC16C5X

XORLW Exclusive OR literal with W

Syntax: `[label] XORLW k`

Operands: $0 \leq k \leq 255$

Operation: $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Encoding:

1111	kkkk	kkkk
------	------	------

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `XORLW 0xAF`

Before Instruction

W = 0xB5

After Instruction

W = 0x1A

XORWF Exclusive OR W with f

Syntax: `[label] XORWF f,d`

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .XOR. (f) \rightarrow (dest)$

Status Affected: Z

Encoding:

0001	10df	ffff
------	------	------

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example `XORWF REG, 1`

Before Instruction

REG = 0xAF

W = 0xB5

After Instruction

REG = 0x1A

W = 0xB5

11.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

11.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in Stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

11.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

11.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

11.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I²C™ bus and separate headers for connection to an LCD module and a keypad.

PIC16C5X

FIGURE 12-3: CLKOUT AND I/O TIMING - PIC16C54/55/56/57

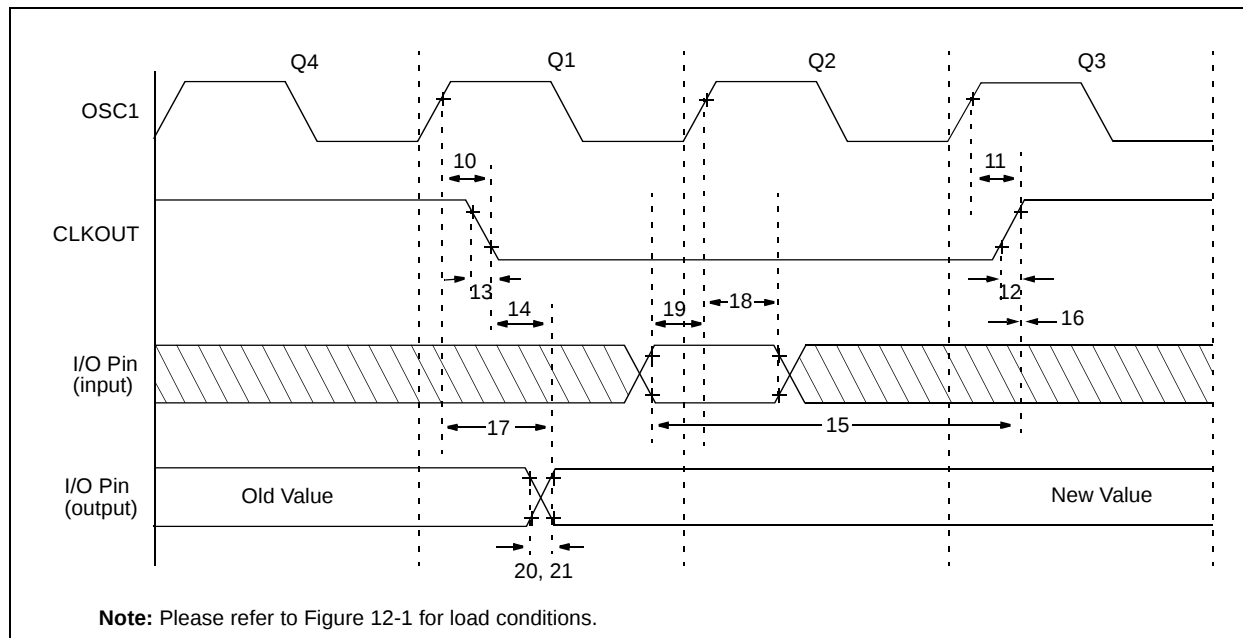


TABLE 12-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57

Standard Operating Conditions (unless otherwise specified)						
AC Characteristics		Operating Temperature				
		0°C ≤ TA ≤ +70°C for commercial				
		-40°C ≤ TA ≤ +85°C for industrial				
		-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽¹⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

Note 2: Please refer to Figure 12-1 for load conditions.

13.5 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T		T	Time
F	Frequency		

Lowercase letters (pp) and their meanings:

pp		mc	MCLR
2	to	osc	oscillator
ck	CLKOUT	os	OSC1
cy	cycle time	t0	T0CKI
drt	device reset timer	wdt	watchdog timer
io	I/O port		

Uppercase letters and their meanings:

S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

FIGURE 13-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16CR54A

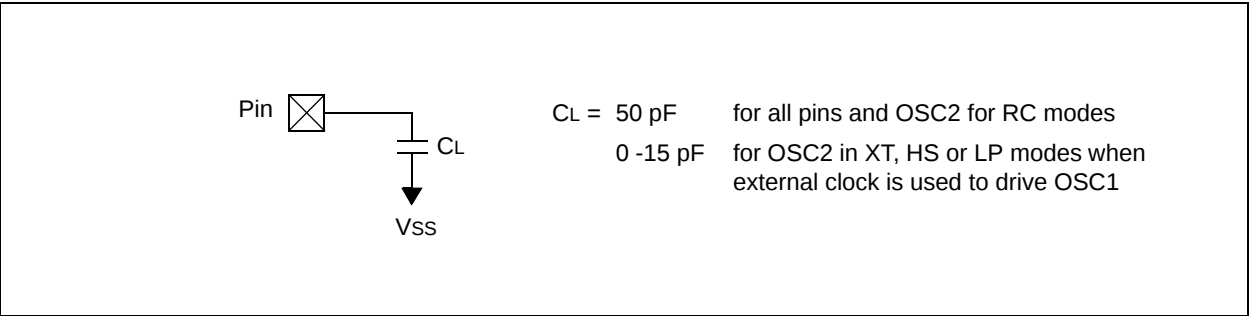


FIGURE 14-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

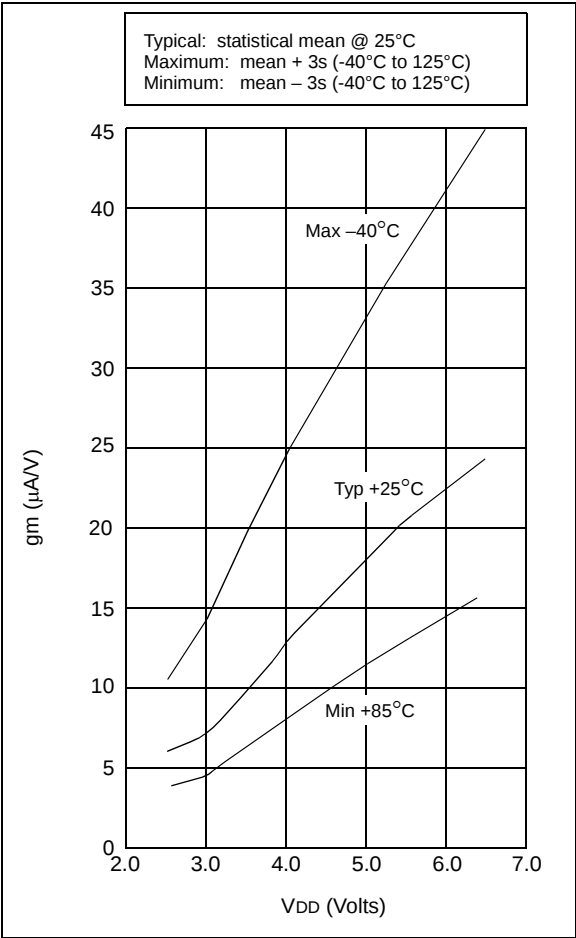
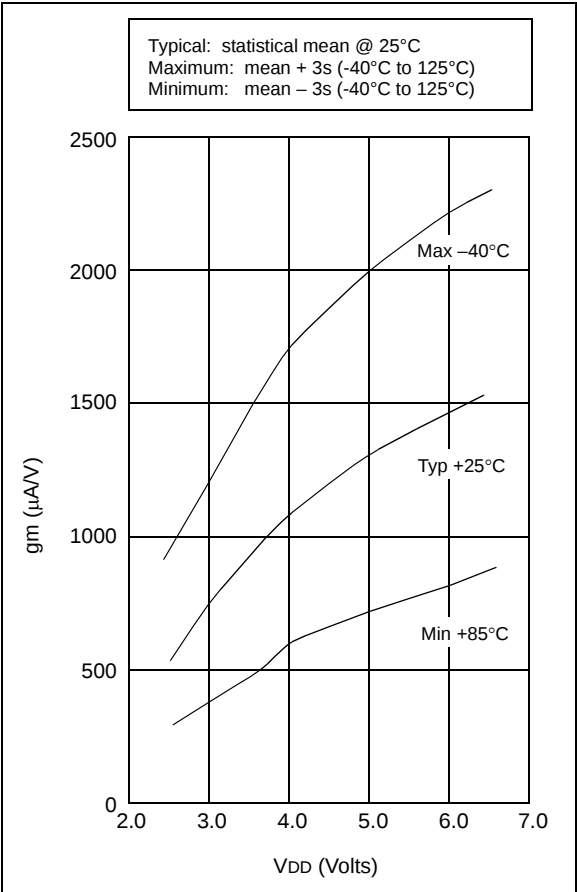


FIGURE 14-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



PIC16C5X

15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16LC54A-04E (Extended)		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
PIC16C54A-04E, 10E, 20E (Extended)		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage					
		PIC16LC54A	3.0 2.5	— —	6.25 6.25	V V	XT and RC modes LP mode
D001A		PIC16C54A	3.5 4.5	— —	5.5 5.5	V V	RC and XT modes HS mode
D002	VDR	RAM Data Retention Voltage⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current⁽²⁾					
		PIC16LC54A	—	0.5	25	mA	FOSC = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes
			—	11	27	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial
			—	11	35	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial
			—	11	37	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Extended
D010A		PIC16C54A	—	1.8	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V, RC ⁽³⁾ and XT modes
			—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V, HS mode
			—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

Note 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

15.4 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04E, 10E, 20E, PIC16LC54A-04E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial-PIC16LV54A-02I $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VSS VSS VSS VSS VSS	— — — — —	0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes
D040	VIH	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.2 VDD + 1 2.0 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD	— — — — — —	VDD VDD VDD VDD VDD VDD	V V V V V V	For all VDD ⁽⁴⁾ 4.0V < VDD ≤ 5.5V ⁽⁴⁾ RC mode only ⁽³⁾ XT, HS and LP modes
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 VDD*	—	—	V	
D060	IIL	Input Leakage Current^(1,2) I/O ports MCLR MCLR T0CKI OSC1	-1.0 -5.0 — -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0 —	μA μA μA μA μA	For VDD ≤ 5.5V: VSS ≤ VPIN ≤ VDD, pin at hi-impedance VPIN = VSS + 0.25V VPIN = VDD VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
D080	VOL	Output Low Voltage I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	IOH = 8.7 mA, VDD = 4.5V IOH = 1.6 mA, VDD = 4.5V, RC mode only
	VOH	Output High Voltage⁽²⁾ I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7	— —	— —	V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC mode only

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

PIC16C5X

FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A

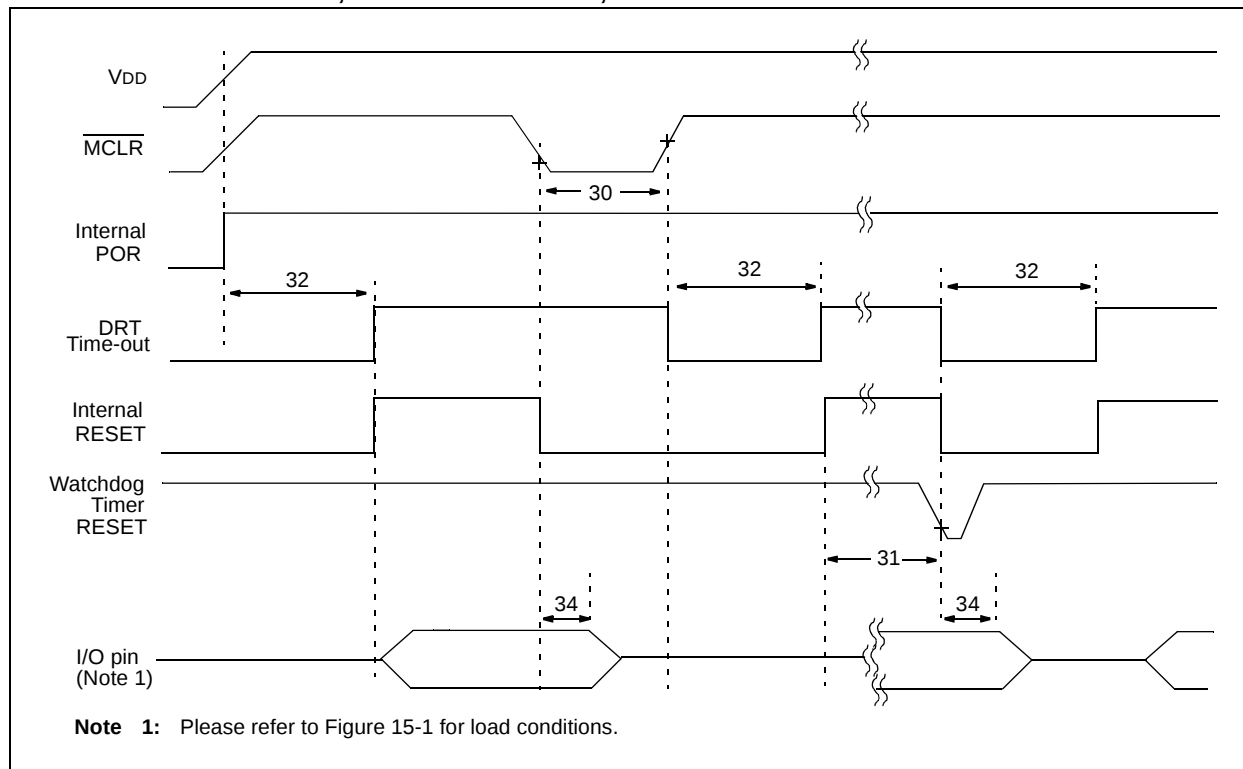


TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

Standard Operating Conditions (unless otherwise specified)							
AC Characteristics							
		Operating Temperature					
		0°C ≤ TA ≤ +70°C for commercial					
		-40°C ≤ TA ≤ +85°C for industrial					
		-20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I					
		-40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (low)	100* 1	— —	— —	ns μs	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	TioZ	I/O Hi-impedance from MCLR Low	— —	— —	100* 1μs	ns —	(PIC16LV54A only)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C5X

FIGURE 16-20: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 3V$

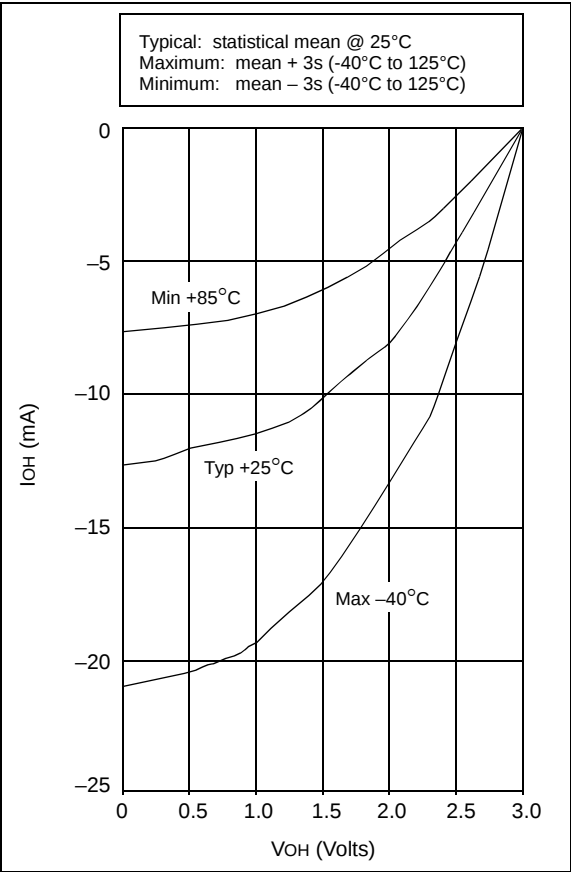
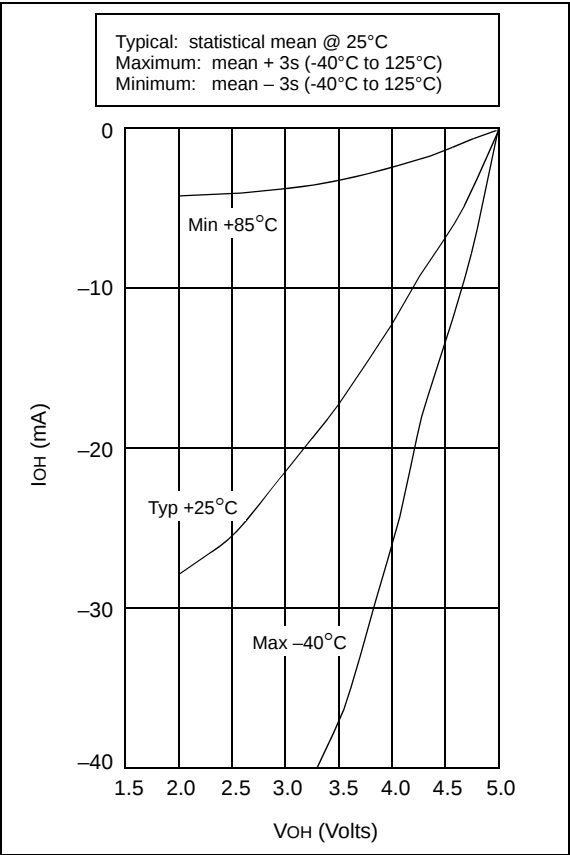


FIGURE 16-21: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 5V$



17.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)				Standard Operating Conditions (unless otherwise specified)			
				Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended			
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0 4.5	— —	5.5 5.5	V V	RC, XT, LP, and HS mode from 0 - 10 MHz from 10 - 20 MHz
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ XT and RC ⁽³⁾ modes HS mode	— —	1.8 9.0	3.3 20	mA mA	FOSC = 4.0 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
D020	IPD	Power-down Current ⁽²⁾	— — — — — —	0.3 10 12 4.8 18 26	17 50* 60* 31* 68* 90*	μA μA μA μA μA μA	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled VDD = 3.0V, WDT enabled VDD = 4.5V, WDT enabled VDD = 5.5V, WDT enabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

FIGURE 18-6: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG ENABLED (25°C)

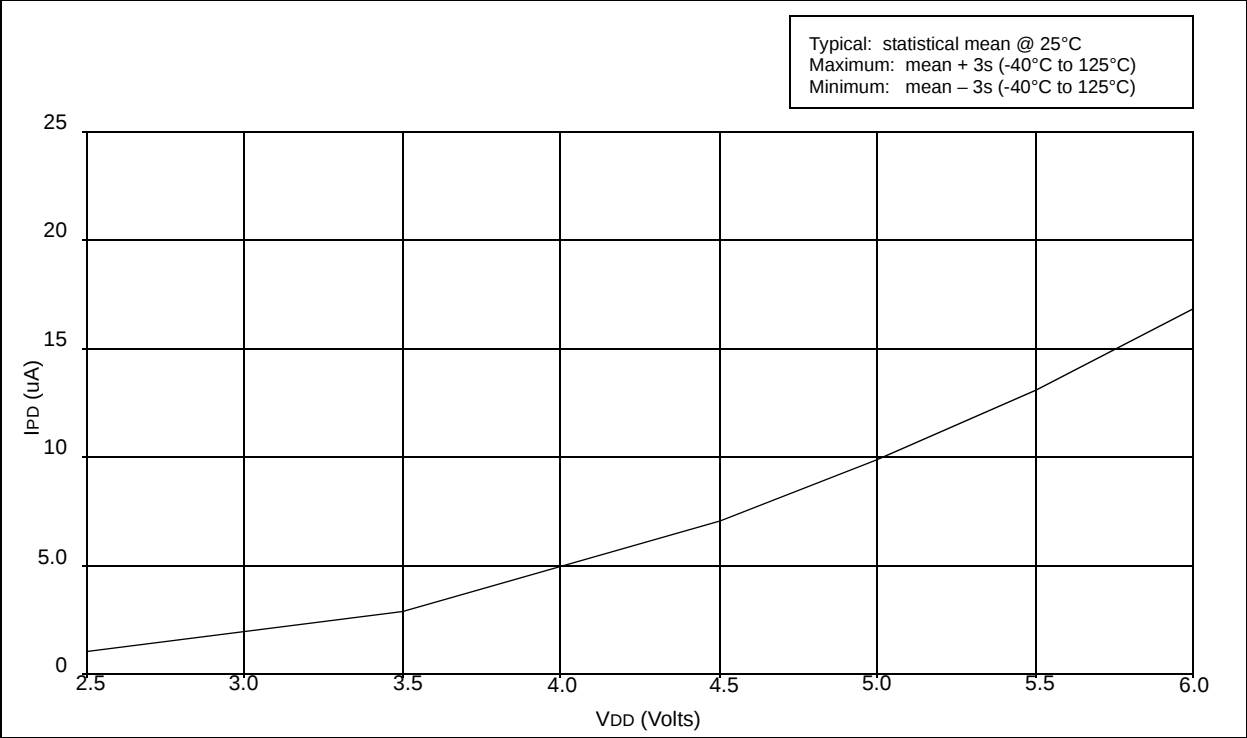
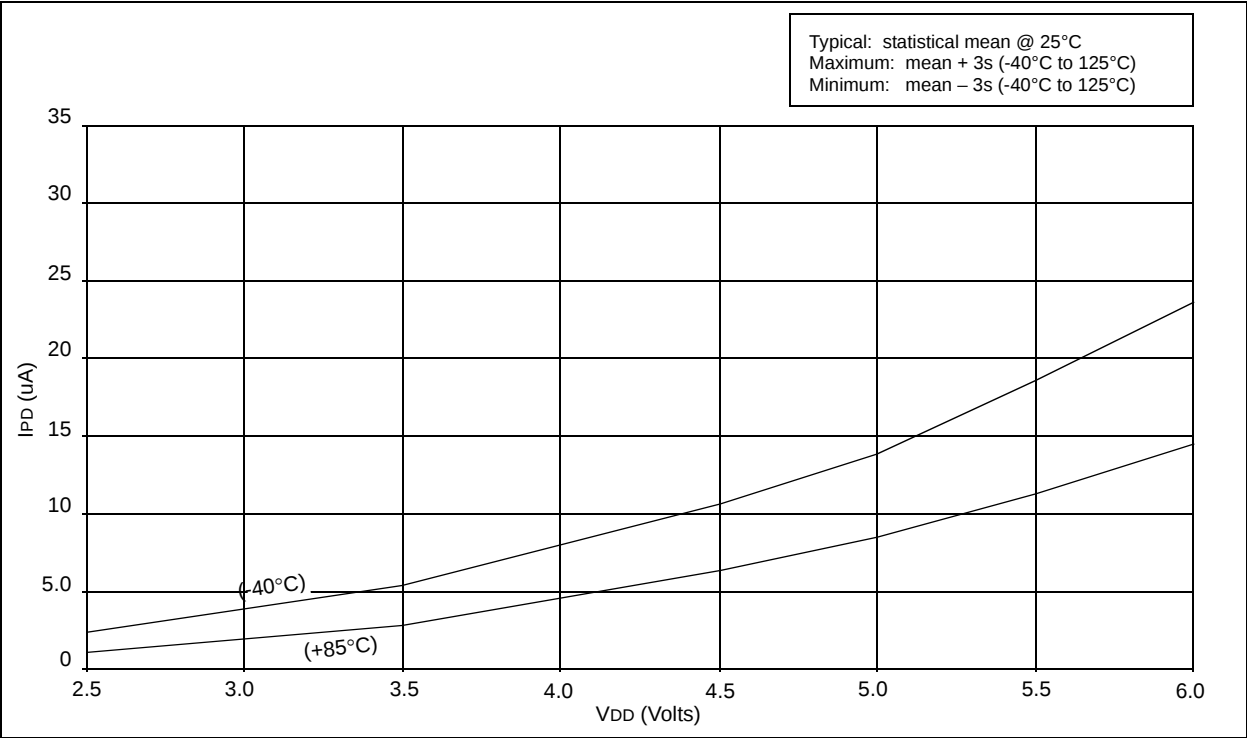
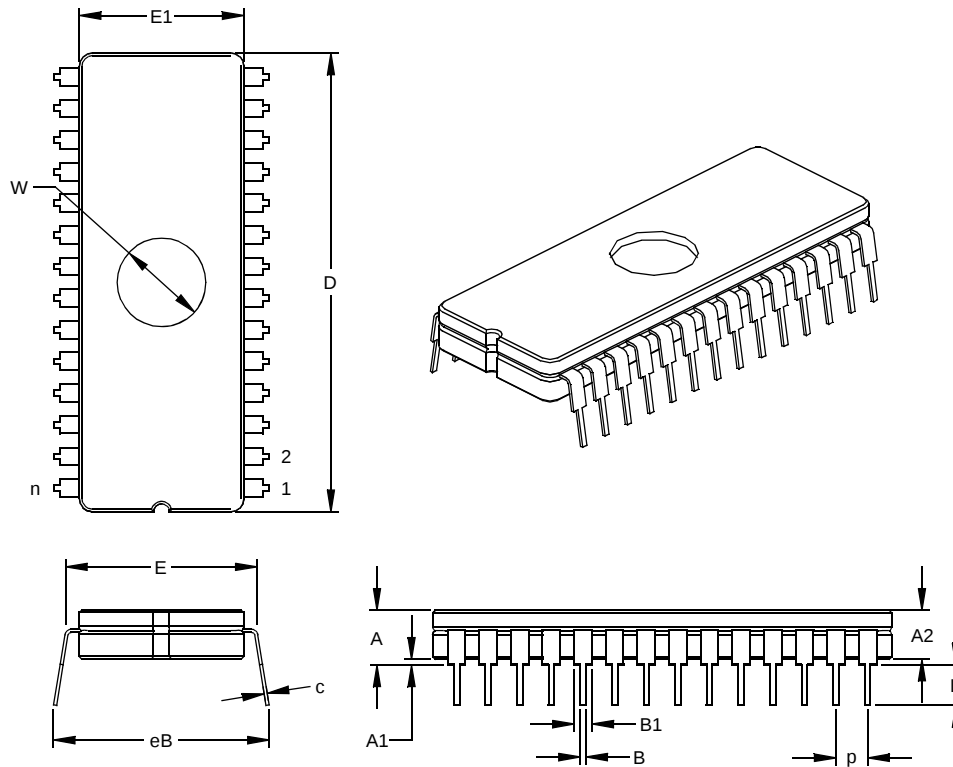


FIGURE 18-7: TYPICAL I_{PD} vs. V_{DD} , WATCHDOG ENABLED (-40°C, 85°C)



28-Lead Ceramic Dual In-line with Window (JW) – 600 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.195	.210	.225	4.95	5.33	5.72
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.038	.060	0.38	0.95	1.52
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	B	.016	.020	.023	0.41	0.51	0.58
Overall Row Spacing	§	eB	.610	.660	15.49	16.76	18.03
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37

* Controlling Parameter
 § Significant Characteristic
 JEDEC Equivalent: MO-103
 Drawing No. C04-013