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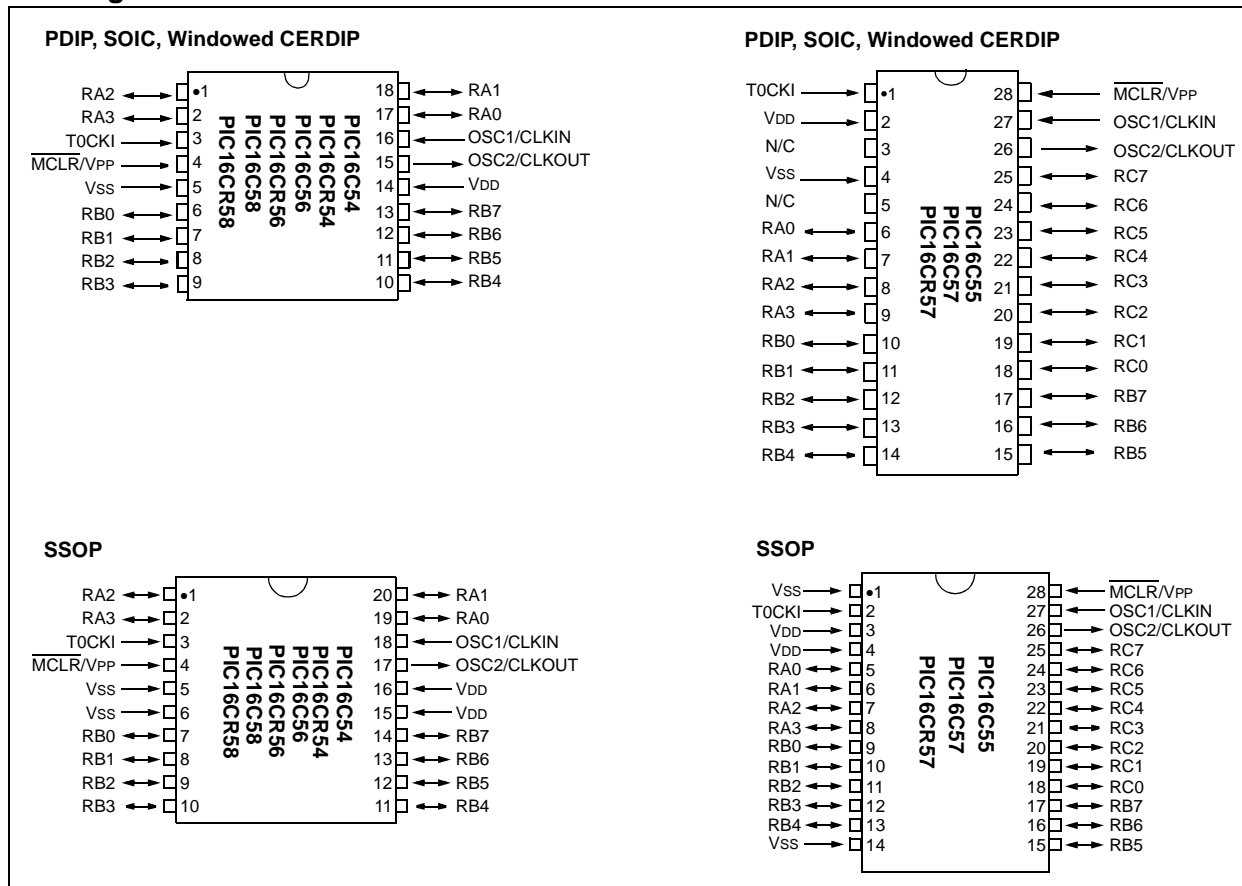
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	20
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lc57c-04i-sp">https://www.e-xfl.com/product-detail/microchip-technology/pic16lc57c-04i-sp</a>

# PIC16C5X

## Pin Diagrams



## Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See <b>Note 1</b>	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See <b>Note 1</b>	0.9	—	No
PIC16C54C	2.5-5.5	User	See <b>Note 1</b>	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See <b>Note 1</b>	1.7	—	No
PIC16C55A	2.5-5.5	User	See <b>Note 1</b>	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See <b>Note 1</b>	1.7	—	No
PIC16C56A	2.5-5.5	User	See <b>Note 1</b>	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See <b>Note 1</b>	1.2	—	No
PIC16C57C	2.5-5.5	User	See <b>Note 1</b>	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See <b>Note 1</b>	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See <b>Note 1</b>	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See <b>Note 1</b>	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See <b>Note 1</b>	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See <b>Note 1</b>	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See <b>Note 1</b>	0.7	N/A	Yes

**Note 1:** If you change from this device to another device, please verify oscillator characteristics in your application.

**Note:** The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

## 5.0 RESET

PIC16C5X devices may be RESET in one of the following ways:

- Power-On Reset (POR)
- $\overline{\text{MCLR}}$  Reset (normal operation)
- $\overline{\text{MCLR}}$  Wake-up Reset (from SLEEP)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from SLEEP)

Table 5-1 shows these RESET conditions for the PCL and STATUS registers.

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-On Reset (POR),  $\overline{\text{MCLR}}$  or WDT Reset. A  $\overline{\text{MCLR}}$  or WDT wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

The  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits (STATUS <4:3>) are set or cleared depending on the different RESET conditions (Table 5-1). These bits may be used to determine the nature of the RESET.

Table 5-3 lists a full description of RESET states of all registers. Figure 5-1 shows a simplified block diagram of the On-chip Reset circuit.

**TABLE 5-1: STATUS BITS AND THEIR SIGNIFICANCE**

Condition	$\overline{\text{TO}}$	$\overline{\text{PD}}$
Power-On Reset	1	1
$\overline{\text{MCLR}}$ Reset (normal operation)	u	u
$\overline{\text{MCLR}}$ Wake-up (from SLEEP)	1	0
WDT Reset (normal operation)	0	1
WDT Wake-up (from SLEEP)	0	0

Legend: u = unchanged, x = unknown, – = unimplemented read as '0'.

**TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH RESET**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on $\overline{\text{MCLR}}$ and WDT Reset
03h	STATUS	PA2	PA1	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, q = see Table 5-1 for possible values.

# PIC16C5X

## 6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

**TABLE 6-1: SPECIAL FUNCTION REGISTER SUMMARY**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	35
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	30
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	32
01h	TMR0	Timer0 Module Register								xxxx xxxx	38
02h <sup>(1)</sup>	PCL	Low order 8 bits of PC								1111 1111	31
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	29
04h	FSR	Indirect data memory address pointer								1xxx xxxx <sup>(3)</sup>	32
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	35
07h <sup>(2)</sup>	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	35

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

- Note 1:** The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.
- 2:** File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.
- 3:** These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for  $\overline{MCLR}$  and WDT Reset, the value is 111u uuuu.

## 6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the  $\overline{TO}$  and  $\overline{PD}$  bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS Register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

### REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7			bit 0				

bit 7: **PA2:** This bit unused at this time.

Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>:** Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)

00 = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

01 = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

10 = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58

11 = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58

Each page is 512 words.

Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4:  **$\overline{TO}$ :** Time-out bit

1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction

0 = A WDT time-out occurred

bit 3:  **$\overline{PD}$ :** Power-down bit

1 = After power-up or by the `CLRWDT` instruction

0 = By execution of the `SLEEP` instruction

bit 2: **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (for `ADDWF` and `SUBWF` instructions)

**ADDWF**

1 = A carry from the 4th low order bit of the result occurred

0 = A carry from the 4th low order bit of the result did not occur

**SUBWF**

1 = A borrow from the 4th low order bit of the result did not occur

0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C:** Carry/borrow bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

**ADDWF**

1 = A carry occurred

0 = A carry did not occur

**SUBWF**

1 = A borrow did not occur

0 = A borrow occurred

**RRF or RLF**

Loaded with LSb or MSb, respectively

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

# PIC16C5X

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NOTES:

FIGURE 8-3: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER

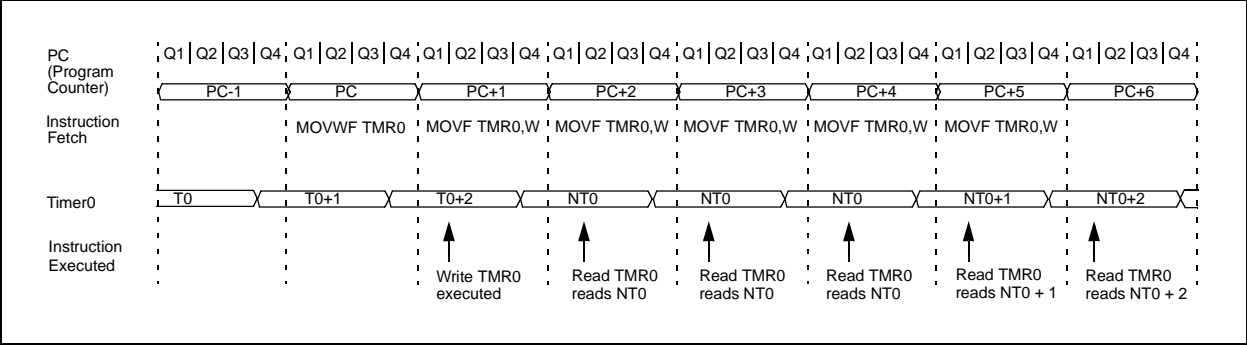


FIGURE 8-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2

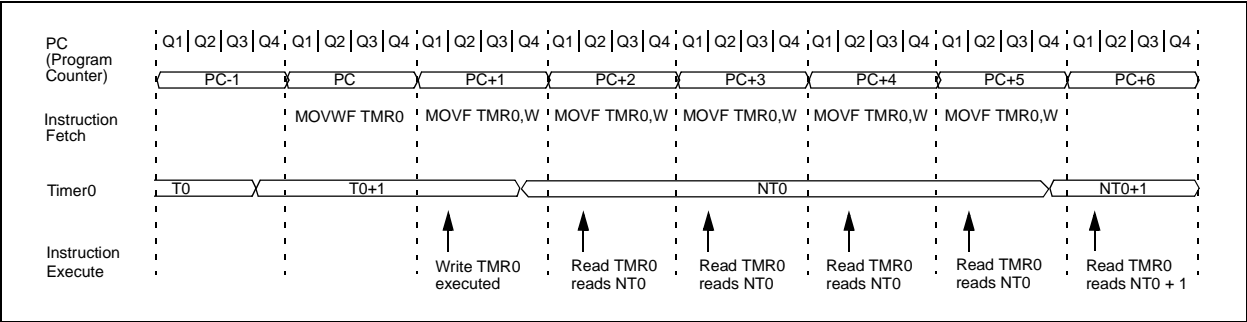


TABLE 8-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells not used by Timer0.

# PIC16C5X

**TABLE 10-2: INSTRUCTION SET SUMMARY**

Mnemonic, Operands		Description	Cycles	12-Bit Opcode			Status Affected	Notes
				MSb	LSb			
ADDWF	f, d	Add W and f	1	0001	11df	ffff	C, DC, Z	1, 2, 4
ANDWF	f, d	AND W with f	1	0001	01df	ffff	Z	2, 4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	—	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2, 4
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	0010	11df	ffff	None	2, 4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2, 4
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	0011	11df	ffff	None	2, 4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2, 4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2, 4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1, 4
NOP	—	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	C	2, 4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	C	2, 4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C, DC, Z	1, 2, 4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2, 4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2, 4
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	0100	bbbbf	ffff	None	2, 4
BSF	f, b	Bit Set f	1	0101	bbbbf	ffff	None	2, 4
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	0110	bbbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS								
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	1
CALL	k	Call subroutine	2	1001	kkkk	kkkk	None	
CLRWDT	k	Clear Watchdog Timer	1	0000	0000	0100	TO, PD	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	—	Go into standby mode	1	0000	0000	0011	TO, PD	
TRIS	f	Load TRIS register	1	0000	0000	0fff	None	3
XORLW	k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

**Note 1:** The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO (see Section 6.5 for more on program counter).

- When an I/O register is modified as a function of itself (e.g. `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- The instruction `TRIS f`, where  $f = 5, 6$  or  $7$  causes the contents of the W register to be written to the tristate latches of PORTA, B or C respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.
- If this instruction is executed on the TMR0 register (and, where applicable,  $d = 1$ ), the prescaler will be cleared (if assigned to TMR0).



## 12.4 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D030	V <sub>IL</sub>	<b>Input Low Voltage</b>					
		I/O ports	V <sub>SS</sub>	—	0.2 V <sub>DD</sub>	V	Pin at hi-impedance
		MCLR (Schmitt Trigger)	V <sub>SS</sub>	—	0.15 V <sub>DD</sub>	V	
		T0CKI (Schmitt Trigger)	V <sub>SS</sub>	—	0.15 V <sub>DD</sub>	V	
		OSC1 (Schmitt Trigger)	V <sub>SS</sub>	—	0.15 V <sub>DD</sub>	V	PIC16C5X-RC only <sup>(3)</sup>
		OSC1 (Schmitt Trigger)	V <sub>SS</sub>	—	0.3 V <sub>DD</sub>	V	PIC16C5X-XT, 10, HS, LP
D040	V <sub>IH</sub>	<b>Input High Voltage</b>					
		I/O ports	0.45 V <sub>DD</sub>	—	V <sub>DD</sub>	V	For all V <sub>DD</sub> <sup>(4)</sup>
		I/O ports	2.0	—	V <sub>DD</sub>	V	4.0V < V <sub>DD</sub> ≤ 5.5V <sup>(4)</sup>
		I/O ports	0.36 V <sub>DD</sub>	—	V <sub>DD</sub>	V	V <sub>DD</sub> > 5.5V
		MCLR (Schmitt Trigger)	0.85 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
		T0CKI (Schmitt Trigger)	0.85 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
		OSC1 (Schmitt Trigger)	0.85 V <sub>DD</sub>	—	V <sub>DD</sub>	V	PIC16C5X-RC only <sup>(3)</sup>
		OSC1 (Schmitt Trigger)	0.7 V <sub>DD</sub>	—	V <sub>DD</sub>	V	PIC16C5X-XT, 10, HS, LP
D050	V <sub>HYS</sub>	<b>Hysteresis of Schmitt Trigger inputs</b>	0.15 V <sub>DD</sub> *	—	—	V	
D060	I <sub>IL</sub>	<b>Input Leakage Current<sup>(1,2)</sup></b>					
		I/O ports	–1	0.5	+1	μA	<b>For V<sub>DD</sub> ≤ 5.5V:</b> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , pin at hi-impedance
		MCLR	–5	—	—	μA	V <sub>PIN</sub> = V <sub>SS</sub> + 0.25V
		MCLR	—	0.5	+5	μA	V <sub>PIN</sub> = V <sub>DD</sub>
		T0CKI	–3	0.5	+3	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub>
		OSC1	–3	0.5	+3	μA	V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , PIC16C5X-XT, 10, HS, LP
D080	V <sub>OL</sub>	<b>Output Low Voltage</b>					
		I/O ports	—	—	0.6	V	I <sub>OL</sub> = 8.7 mA, V <sub>DD</sub> = 4.5V
		OSC2/CLKOUT	—	—	0.6	V	I <sub>OL</sub> = 1.6 mA, V <sub>DD</sub> = 4.5V, PIC16C5X-RC
D090	V <sub>OH</sub>	<b>Output High Voltage<sup>(2)</sup></b>					
		I/O ports	V <sub>DD</sub> – 0.7	—	—	V	I <sub>OH</sub> = –5.4 mA, V <sub>DD</sub> = 4.5V
		OSC2/CLKOUT	V <sub>DD</sub> – 0.7	—	—	V	I <sub>OH</sub> = –1.0 mA, V <sub>DD</sub> = 4.5V, PIC16C5X-RC

\* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/V<sub>PP</sub> pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

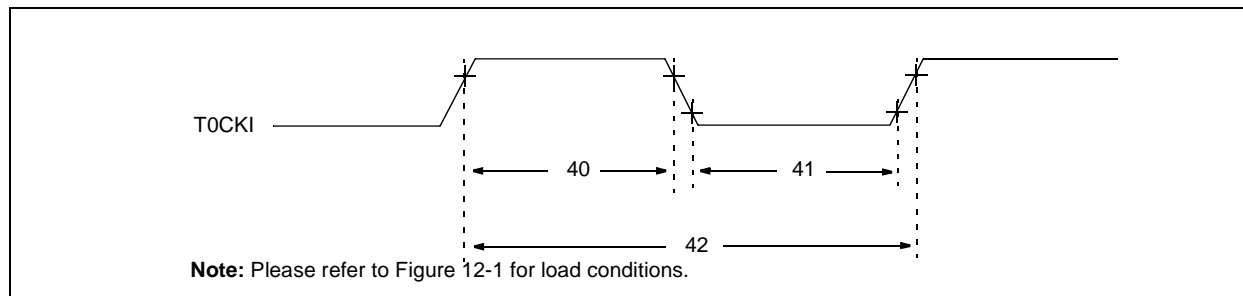
**2:** Negative current is defined as coming out of the pin.

**3:** For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.

# PIC16C5X

**FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57**



**TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57**

<b>Standard Operating Conditions (unless otherwise specified)</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
<b>AC Characteristics</b>							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	$10^*$	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	$10^*$	—	—	ns	
42	Tt0P	T0CKI Period	$20$ or $\frac{T_{CY} + 40^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# PIC16C5X

## 13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

<b>PIC16LCR54A-04</b> <b>PIC16LCR54A-04I</b> (Commercial, Industrial)			<b>Standard Operating Conditions (unless otherwise specified)</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
<b>PIC16CR54A-04, 10, 20</b> <b>PIC16CR54A-04I, 10I, 20I</b> (Commercial, Industrial)			<b>Standard Operating Conditions (unless otherwise specified)</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D001	VDD	<b>Supply Voltage</b>					
		PIC16LCR54A	2.0	—	6.25	V	
		PIC16CR54A	2.5	—	6.25	V	RC and XT modes
D001A			4.5	—	5.5	V	HS mode
D002	VDR	<b>RAM Data Retention Voltage<sup>(1)</sup></b>	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	<b>VDD Start Voltage</b> to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	<b>VDD Rise Rate</b> to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D005	IDD	<b>Supply Current<sup>(2)</sup></b>					
		PICLCR54A	—	10	20	μA	Fosc = 32 kHz, VDD = 2.0V
			—	—	70	μA	Fosc = 32 kHz, VDD = 6.0V
D005A		PIC16CR54A	—	2.0	3.6	mA	<b>RC<sup>(3)</sup> and XT modes:</b> FOSC = 4.0 MHz, VDD = 6.0V FOSC = 4.0 MHz, VDD = 3.0V FOSC = 200 kHz, VDD = 2.5V <b>HS mode:</b> FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
			—	0.8	1.8	mA	
			—	90	350	μA	
			—	4.8	10	mA	
			—	9.0	20	mA	

Legend: Rows with standard voltage device data only are shaded for improved readability.

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**Note 3:** Does not include current through REXT. The current through the resistor can be estimated by the formula:  $I_R = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.

# PIC16C5X

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**TABLE 14-2: INPUT CAPACITANCE FOR  
PIC16C54/56**

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of  $\pm 25\%$  (three standard deviations) should be taken into account.

**TABLE 14-3: INPUT CAPACITANCE FOR  
PIC16C55/57**

Pin	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
T0CKI	4.5	3.5

All capacitance values are typical at 25°C. A part-to-part variation of  $\pm 25\%$  (three standard deviations) should be taken into account.

# PIC16C5X

## 15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	V <sub>DD</sub>	<b>Supply Voltage</b> RC and XT modes	2.0	—	3.8	V	
D002	V <sub>DR</sub>	<b>RAM Data Retention Voltage<sup>(1)</sup></b>	—	1.5*	—	V	Device in SLEEP mode
D003	V <sub>POR</sub>	<b>V<sub>DD</sub> Start Voltage</b> to ensure Power-on Reset	—	V <sub>SS</sub>	—	V	See Section 5.1 for details on Power-on Reset
D004	S <sub>VDD</sub>	<b>V<sub>DD</sub> Rise Rate</b> to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	I <sub>DD</sub>	<b>Supply Current<sup>(2)</sup></b> RC <sup>(3)</sup> and XT modes LP mode, Commercial LP mode, Industrial	— — —	0.5 11 14	— 27 35	mA μA μA	FOSC = 2.0 MHz, V <sub>DD</sub> = 3.0V FOSC = 32 kHz, V <sub>DD</sub> = 2.5V WDT disabled FOSC = 32 kHz, V <sub>DD</sub> = 2.5V WDT disabled
D020	I <sub>PD</sub>	<b>Power-down Current<sup>(2,4)</sup></b> Commercial Commercial Industrial Industrial	— — — —	2.5 0.25 3.5 0.3	12 4.0 14 5.0	μA μA μA μA	V <sub>DD</sub> = 2.5V, WDT enabled V <sub>DD</sub> = 2.5V, WDT disabled V <sub>DD</sub> = 2.5V, WDT enabled V <sub>DD</sub> = 2.5V, WDT disabled

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which V<sub>DD</sub> can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all I<sub>DD</sub> measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V<sub>SS</sub>, T0CKI = V<sub>DD</sub>, MCLR = V<sub>DD</sub>; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through R<sub>EXT</sub>. The current through the resistor can be estimated by the formula:  $I_R = V_{DD}/2R_{EXT}$  (mA) with R<sub>EXT</sub> in kΩ.

**4:** The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

# PIC16C5X

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NOTES:

FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

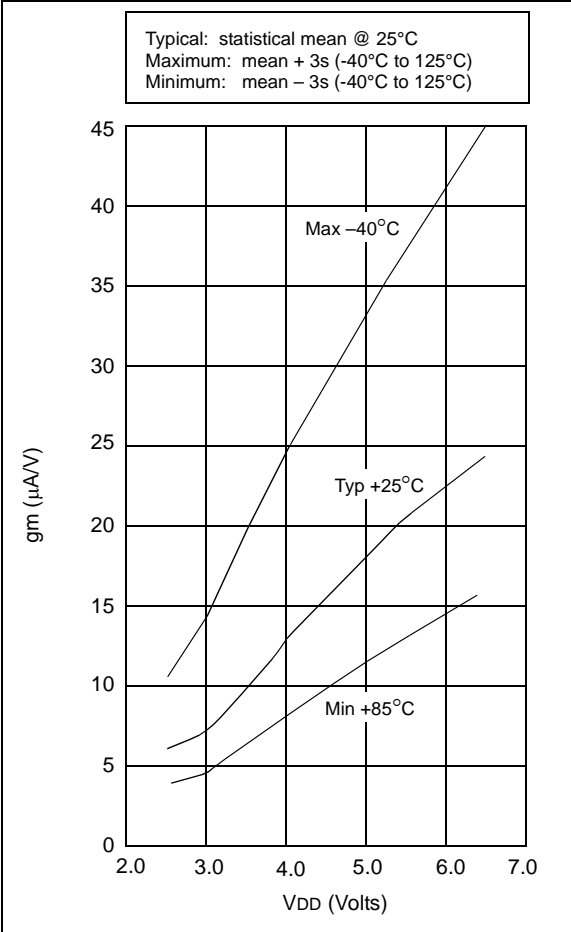
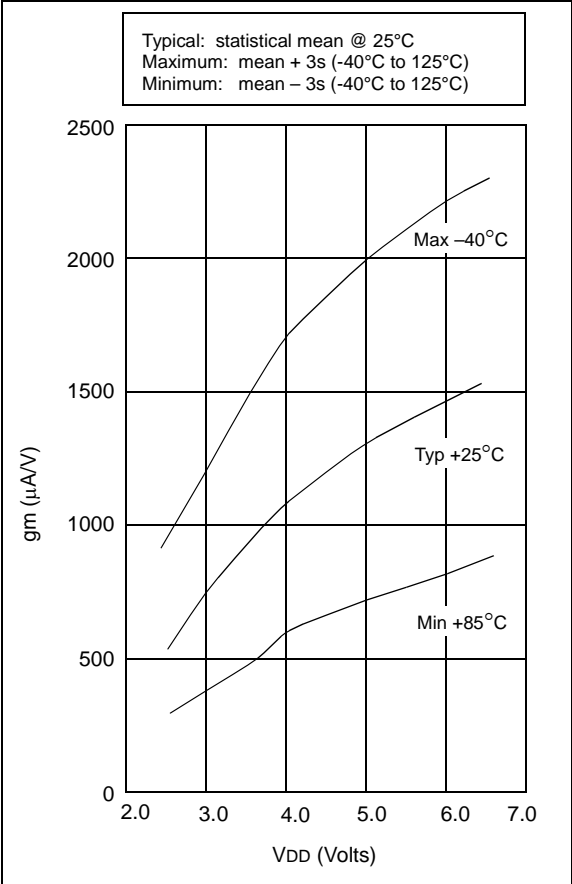


FIGURE 16-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



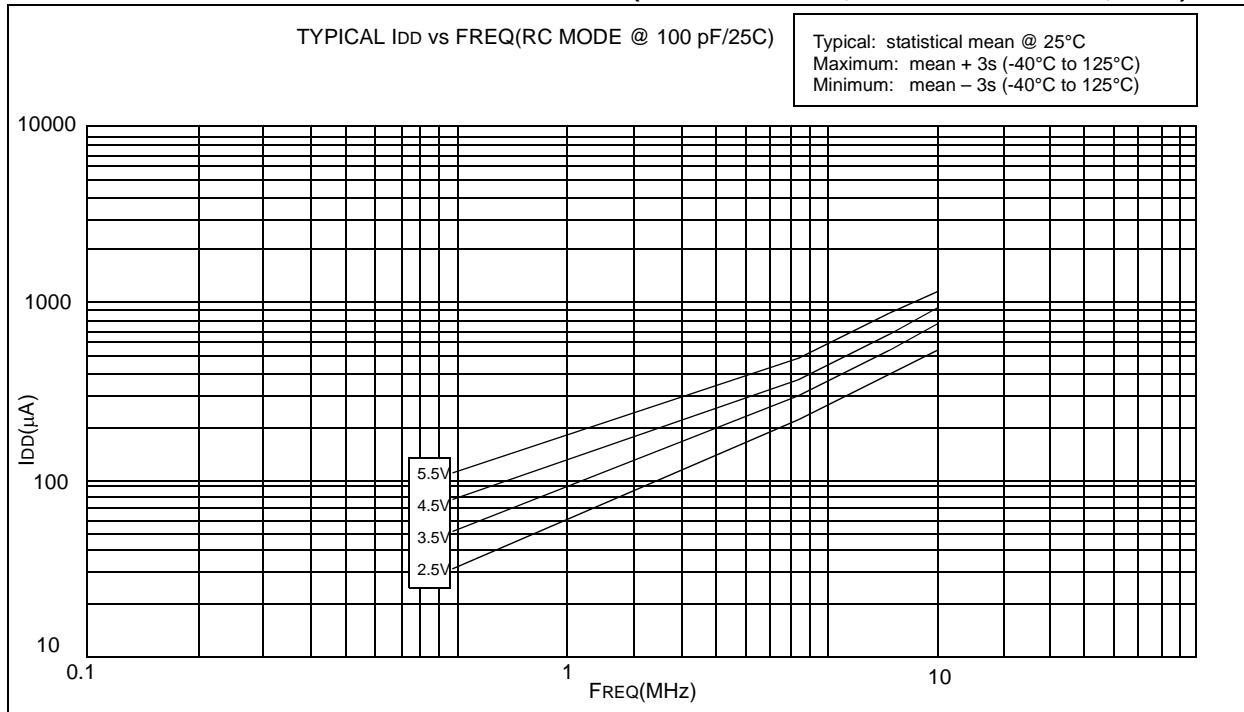
# PIC16C5X

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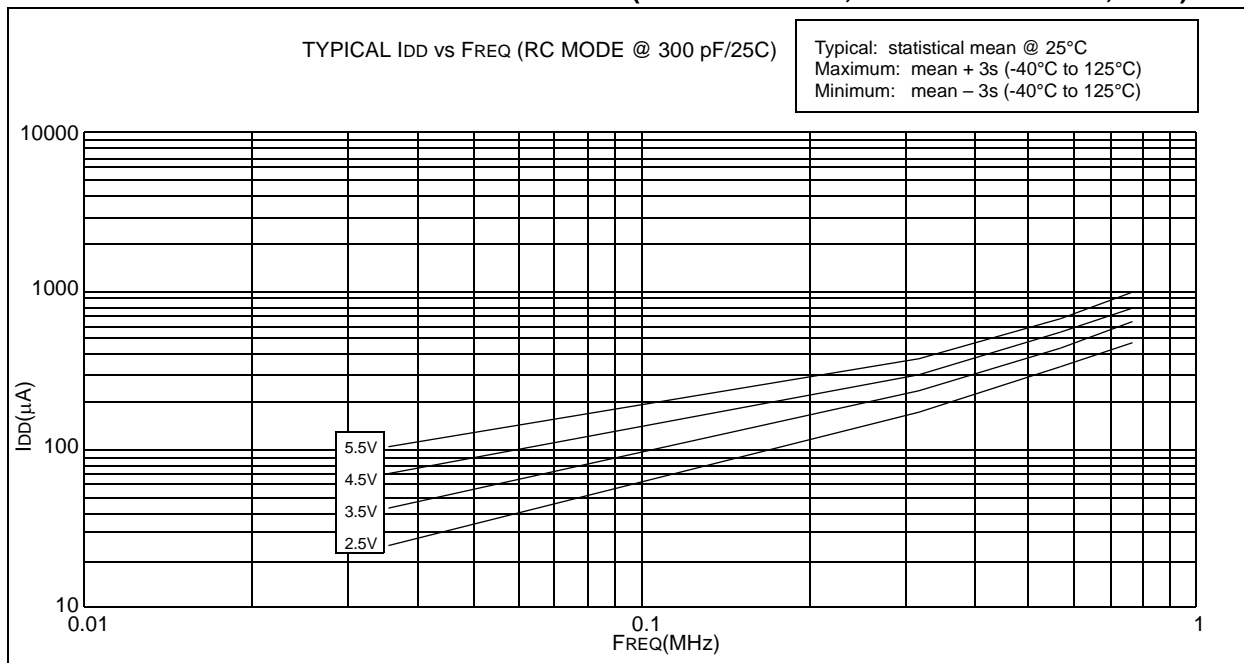
NOTES:



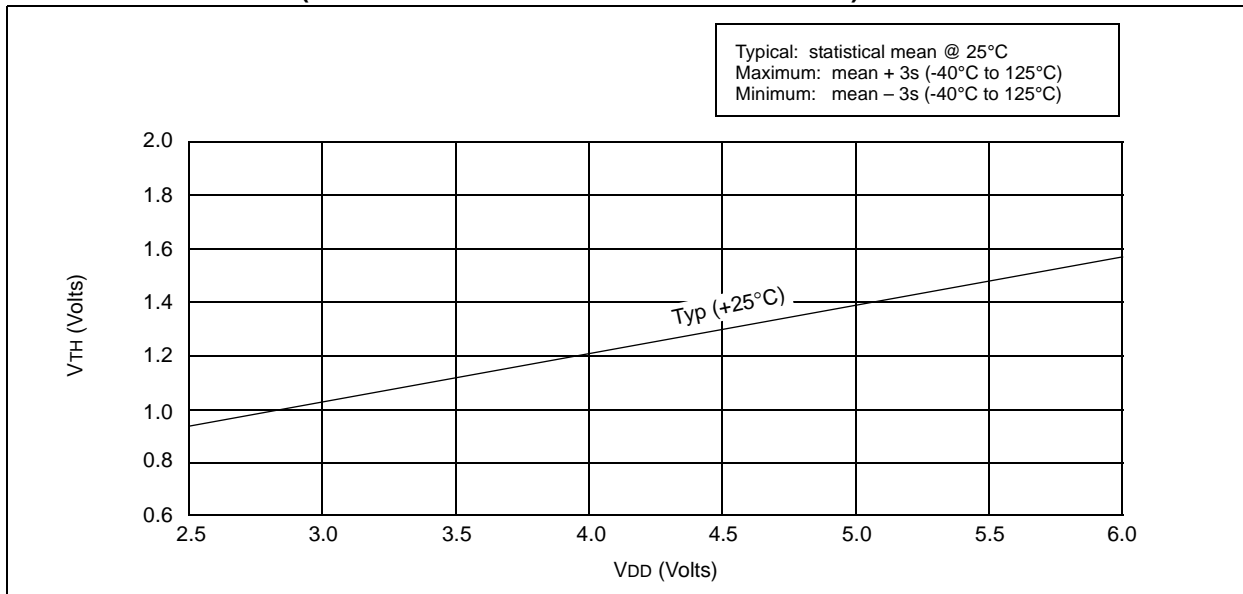
**FIGURE 18-12: TYPICAL  $I_{DD}$  vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)**



**FIGURE 18-13: TYPICAL  $I_{DD}$  vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)**



**FIGURE 20-4:  $V_{TH}$  (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs.  $V_{DD}$**



**FIGURE 20-5:  $V_{TH}$  (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (HS MODE) vs.  $V_{DD}$**

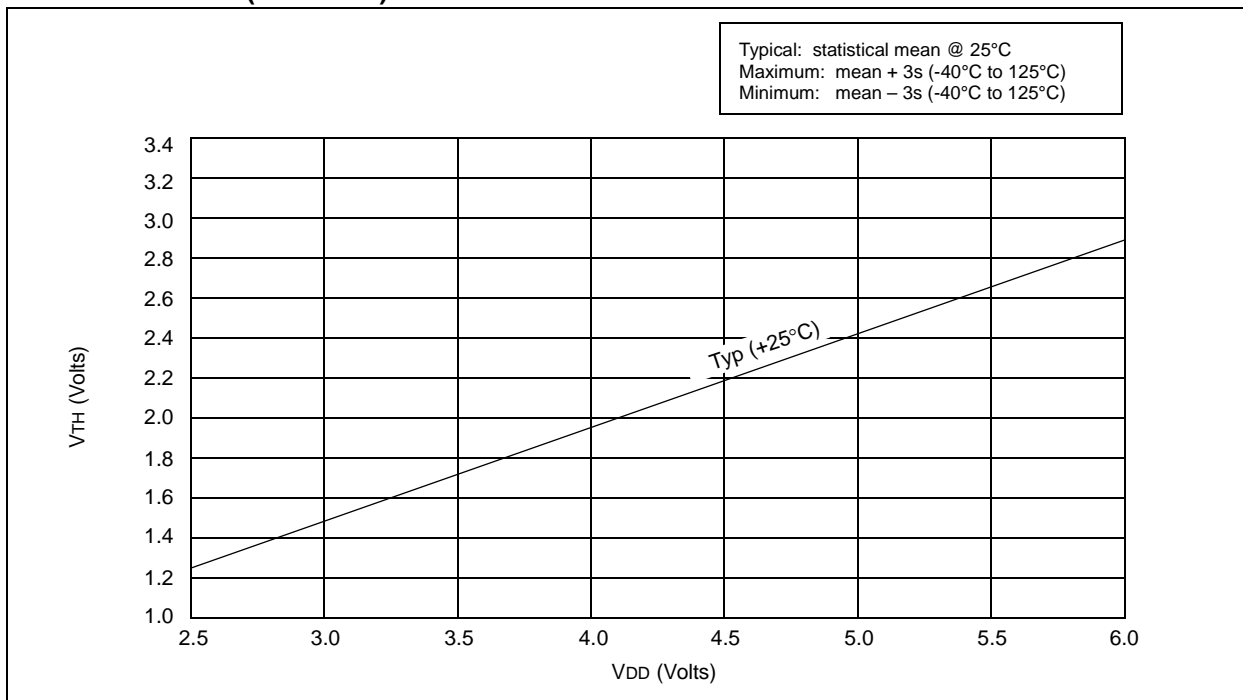
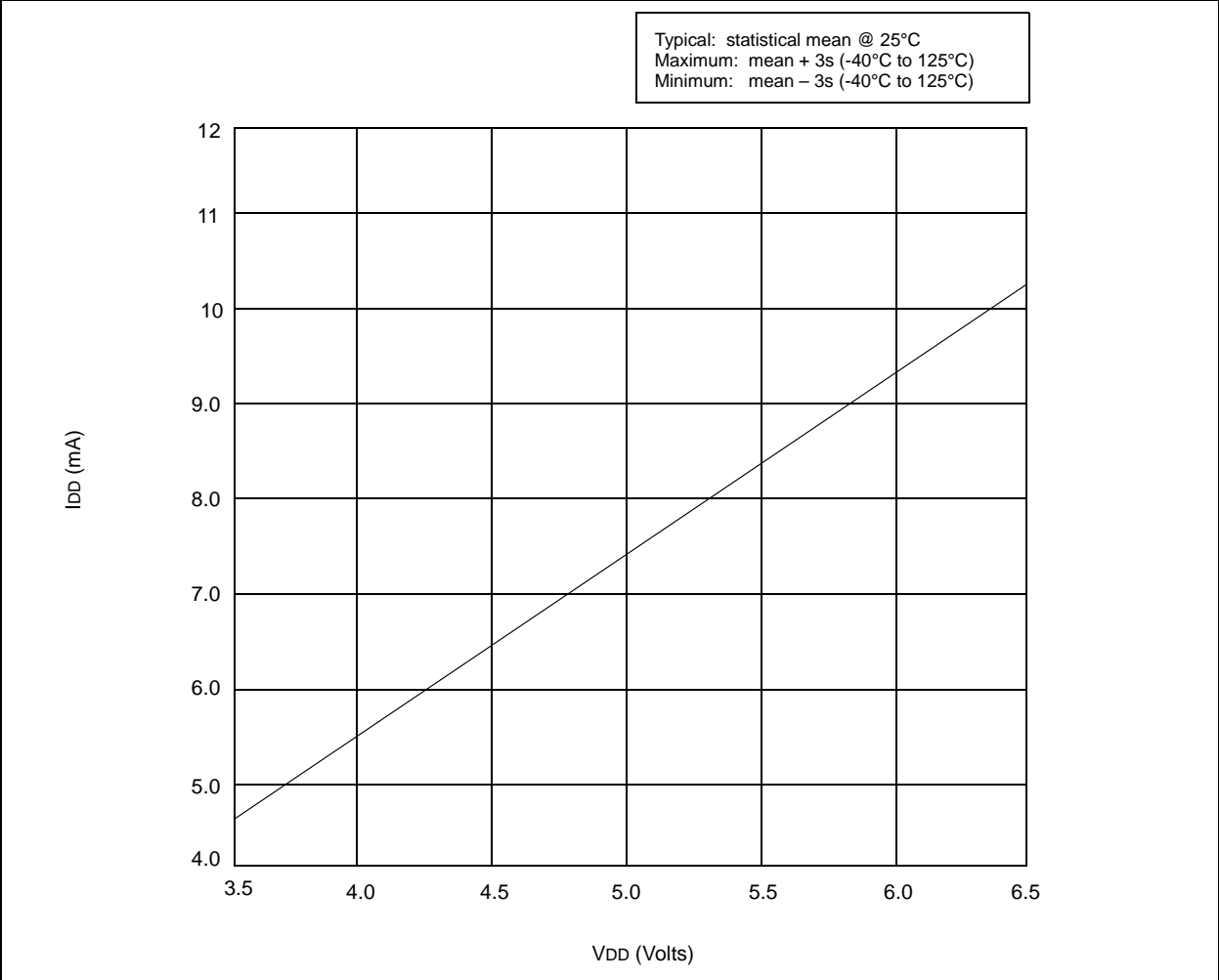


FIGURE 20-6: TYPICAL I<sub>DD</sub> vs. V<sub>DD</sub> (40 MHZ, WDT DISABLED, HS MODE, 70°C)



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