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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	3KB (2K x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	73 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc58b-04-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pi	n Numb	er	Pin	Buffer	Description
DIP	SOIC	SSOP	Туре	Туре	Description
17	17	19	I/O	TTL	Bi-directional I/O port
18	18	20	I/O	TTL	
1	1	1	I/O	TTL	
2	2	2	I/O	TTL	
6	6	7	I/O	TTL	Bi-directional I/O port
7	7	8	I/O	TTL	
8	8	9	I/O	TTL	
9	9	10	I/O	TTL	
10	10	11	I/O	TTL	
11	11	12	I/O	TTL	
12	12	13	I/O	TTL	
13	13	14	I/O	TTL	
3	3	3	Ι	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in
					use, to reduce current consumption.
4	4	4	Ι	ST	Master clear (RESET) input/programming voltage input.
					This pin is an active low RESET to the device. Voltage on
					the MCLR/VPP pin must not exceed VDD to avoid unin-
					tended entering of Programming mode.
16	16	18	I	ST	Oscillator crystal input/external clock source input.
15	15	17	0	_	Oscillator crystal output. Connects to crystal or resonator
					in crystal Oscillator mode. In RC mode, OSC2 pin outputs
					CLKOUT, which has 1/4 the frequency of OSC1 and
					denotes the instruction cycle rate.
14	14	15,16	Р	_	Positive supply for logic and I/O pins.
5	5	5,6	Р	—	Ground reference for logic and I/O pins.
	Pi DIP 17 18 1 2 6 7 8 9 10 11 12 13 3 4 16 15 14	Pin Numb DIP SOIC 17 17 18 18 1 1 2 2 6 6 7 7 8 8 9 9 10 10 11 11 12 12 13 13 3 3 4 4 16 16 15 15 14 14	Pin Number DIP SOIC SSOP 17 17 19 18 18 20 1 1 1 2 2 2 6 6 7 7 7 8 8 8 9 9 9 10 10 10 11 11 11 12 12 12 13 13 13 14 3 3 3 4 4 4 15 15 17 14 14 15,16	Pin Pin DIP SOIC SSOP Type 17 17 19 I/O 18 18 20 I/O 1 1 1 I/O 2 2 2 I/O 6 6 7 I/O 7 7 8 I/O 8 9 I/O I/O 9 9 10 I/O 10 10 11 I/O 11 11 12 I/O 12 12 13 I/O 13 13 14 I/O 3 3 3 I 16 16 18 I 15 15 17 O 14 14 15,16 P	Pin Buffer DIP SOIC SSOP Type Type 17 17 19 I/O TTL 18 18 20 I/O TTL 1 1 1/O TTL 2 2 2 I/O TTL 6 6 7 I/O TTL 7 7 8 I/O TTL 9 9 10 I/O TTL 10 10 11 I/O TTL 11 11 12 I/O TTL 9 9 10 I/O TTL 10 10 11 I/O TTL 12 12 13 I/O TTL 13 13 14 I/O TTL 3 3 3 I ST 16 16 18 I ST 15 15 17 <td< td=""></td<>

TABLE 3-1:PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58,
PIC16CR58

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

NOTES:

Mnemonic, Operands		Description	Cycles	12-Bit Opcode			Status	Mater
		Description		MSb		LSb	Affected	Notes
ADDWF	f,d	Add W and f	1	0001	11df	ffff	C,DC,Z	1,2,4
ANDWF	f,d	AND W with f	1	0001	01df	ffff	Z	2,4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	-	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2,4
DECFSZ	f, d	Decrement f, Skip if 0	1 ⁽²⁾	0010	11df	ffff	None	2,4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2,4
INCFSZ	f, d	Increment f, Skip if 0	1 ⁽²⁾	0011	11df	ffff	None	2,4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2,4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2,4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1,4
NOP	-	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	С	2,4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	С	2,4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2,4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2,4
BIT-ORIEN	TED FIL	E REGISTER OPERATIONS	•					
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	2,4
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	2,4
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL A	ND CON	ITROL OPERATIONS	•					
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	1001	kkkk	kkkk	None	1
CLRWDT	k	Clear Watchdog Timer	1	0000	0000	0100	TO, PD	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	_	Go into standby mode	1	0000	0000	0011	TO, PD	
TRIS	f	Load TRIS register	1	0000	0000	Offf	None	3
XORLW	k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

TABLE 10-2: INSTRUCTION SET SUMMARY

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO (see Section 6.5 for more on program counter).

2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction TRIS f, where f = 5, 6 or 7 causes the contents of the W register to be written to the tristate latches of PORTA, B or C respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

PIC16C5X

COMF	Complement f								
Syntax:	[label] COMF f,d								
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$								
Operation:	$(\overline{f}) \rightarrow (dest)$								
Status Affected:	Z								
Encoding:	0010 01df ffff								
Description:	The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example:	COMF REG1,0								
Before Instru REG1 After Instruct REG1 W	= 0x13								

DECF	Decrement f								
Syntax:	[label]	[<i>label</i>] DECF f,d							
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$								
Operation:	$(f) - 1 \rightarrow$	(dest)							
Status Affected:	Z								
Encoding:	0000	11df	ffff						
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example:	DECF	CNT,	1						
Before Instru CNT Z After Instruct CNT Z	= 0 = 0 ion	<01							

DECFSZ	Decrement f, Skip if 0							
Syntax:	[label] DECFSZ f,d							
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$							
Operation:	(f) $-1 \rightarrow d$; skip if result = 0							
Status Affected:	None							
Encoding:	0010 11df ffff							
Description:	The contents of register 'f' are dec- remented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruc- tion, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.							
Words:	1							
Cycles:	1(2)							
Example:	HERE DECFSZ CNT, 1 GOTO LOOP CONTINUE • •							
Before Instru PC	= address (HERE)							
After Instruct CNT if CNT PC if CNT PC	tion = CNT - 1; = 0, = address (CONTINUE); ≠ 0, = address (HERE+1)							

PIC16C5X

IORLW	Inclusive OR literal with W						
Syntax:	[<i>label</i>] IORLW k						
Operands:	$0 \leq k \leq 255$						
Operation:	(W) .OR. (k) \rightarrow (W)						
Status Affected:	Z						
Encoding:	1101 kkkk kkkk						
Description:	The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W regis- ter.						
Words:	1						
Cycles:	1						
Example:	IORLW 0x35						
Before Instru W = After Instruc W = Z =	0x9A tion						

IORWF	Inclusive OR W with f						
Syntax:	[<i>label</i>] IORWF f,d						
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$						
Operation:	(W).OR. (f) \rightarrow (dest)						
Status Affected:	Z						
Encoding:	0001 00df ffff						
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.						
Words:	1						
Cycles:	1						
Example:	IORWF RESULT, 0						
Before Instru RESUL W After Instruct RESUL W Z	Γ = 0x13 = 0x91 tion						

MOVF	Move f								
Syntax:	[<i>label</i>] MOVF f,d								
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$								
Operation:	$(f) \rightarrow (dest)$								
Status Affected:	Z								
Encoding:	0010 00df ffff								
Description:	The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.								
Words:	1								
Cycles:	1								
Example:	MOVF FSR, 0								
After Instruct W =	tion - value in FSR register								

MOVLW	Move Literal to W								
Syntax:	[label]	MOVLW	k						
Operands:	$0 \le k \le 255$								
Operation:	$k \rightarrow (W)$								
Status Affected:	None								
Encoding:	1100	kkkk	kkkk						
Description:	The eigh the W re		'k' is loaded	d into					
Words:	1								
Cycles:	1								
Example:	MOVLW	0x5A							
After Instruction W = 0x5A									

11.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial ProgrammingTM protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

11.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in Stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

11.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

11.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A). PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE incircuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

11.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I^2C^{TM} bus and separate headers for connection to an LCD module and a keypad.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)			$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$						
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
	IPD	Power-down Current ⁽²⁾							
D006		PIC16LCR54A-Commercial		1.0 2.0 3.0 5.0	6.0 8.0* 15 25	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled		
D006A		PIC16CR54A-Commercial		1.0 2.0 3.0 5.0	6.0 8.0* 15 25	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled		
D007		PIC16LCR54A-Industrial		1.0 2.0 3.0 3.0 5.0	8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled		
D007A		PIC16CR54A-Industrial		1.0 2.0 3.0 3.0 5.0	8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- **Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

			$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array} $					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD	V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes	
D040	VIн	Input High Voltage I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	2.0 0.6 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V	VDD = 3.0V to 5.5V ⁽⁴⁾ Full VDD range ⁽⁴⁾ RC mode only ⁽³⁾ XT, HS and LP modes	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 VDD*	—	—	V		
D060	lι∟	Input Leakage Current ^(1,2) I/O ports	-1.0	_	+1.0	μA	For VDD \leq 5.5V: VSS \leq VPIN \leq VDD, pin at hi-impedance	
		MCLR MCLR TOCKI OSC1	-5.0 -3.0 -3.0	— 0.5 0.5 0.5	 +5.0 +3.0 +3.0	μΑ μΑ μΑ	$\label{eq:VPIN} \begin{array}{l} VPIN = VSS + 0.25V \\ VPIN = VDD \\ VSS \leq VPIN \leq VDD \\ VSS \leq VPIN \leq VDD, \\ XT, HS \text{and} LP \text{modes} \end{array}$	
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.5 0.5	V V	IOL = 10 mA, VDD = 6.0 V IOL = 1.9 mA, VDD = 6.0 V, RC mode only	
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd - 0.5 Vdd - 0.5	_		V V	IOH = -4.0 mA, VDD = 6.0 V IOH = -0.8 mA, VDD = 6.0 V, RC mode only	

* These parameters are characterized but not tested.

- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- **Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - 2: Negative current is defined as coming out of the pin.
 - **3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
 - 4: The user may use the better of the two specifications.

FIGURE 14-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD







16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

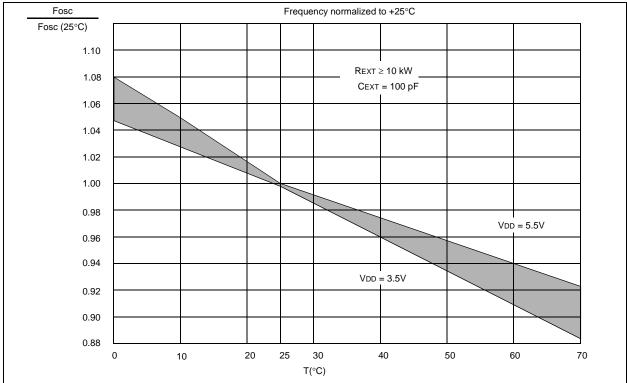


FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

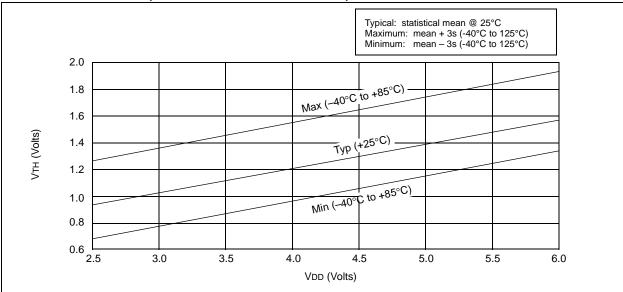
TABLE 16-1:	RC OSCILLATOR FREQUENCIES
-------------	---------------------------

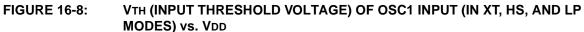
Сехт	Rext	Average Fosc @ 5 V, 25°C		
20 pF	3.3K	5 MHz	± 27%	
	5K	3.8 MHz	± 21%	
	10K	2.2 MHz	± 21%	
	100K	262 kHz	± 31%	
100 pF	3.3K	1.6 MHz	± 13%	
	5K	1.2 MHz	± 13%	
	10K	684 kHz	± 18%	
	100K	71 kHz	± 25%	
300 pF	3.3K	660 kHz	± 10%	
	5.0K	484 kHz	± 14%	
	10K	267 kHz	± 15%	
	100K	29 kHz	± 19%	

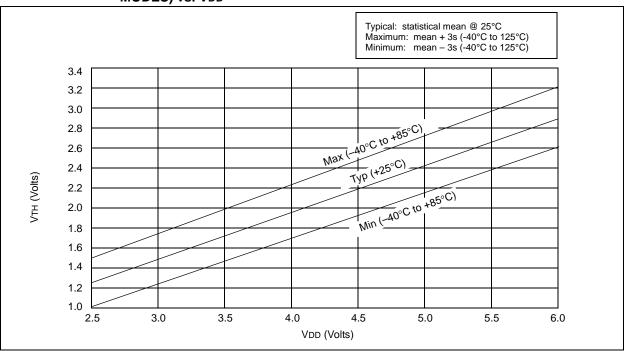
The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.

FIGURE 16-7: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS - VDD









	ALVAUT AND VA TIMINA DEALUDENENTA DIALAASY DIALAADSY
IABLE 17-2:	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Chara	acteristics	$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array} $					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	_	15	30**	ns	
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	_	15	30**	ns	
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns	
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns	
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns	
15	TioV2ckH	Port in valid before CLKOUT ⁽¹⁾	0.25 TCY+30*	—	_	ns	
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	—	_	ns	
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	_	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns	
20	TioR	Port output rise time ⁽²⁾	_	10	25**	ns	
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns	

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Refer to Figure 17-5 for load conditions.

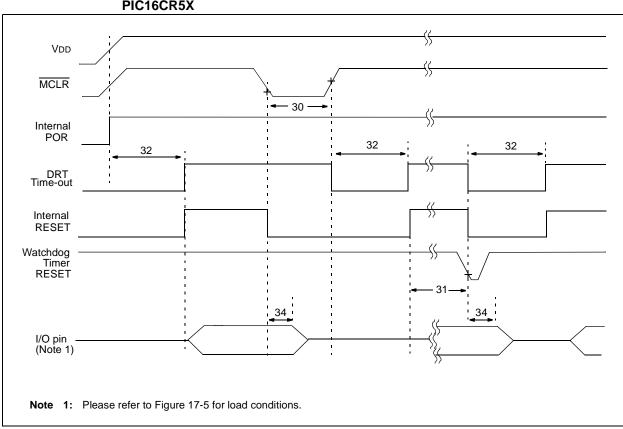


FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X

TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

$\label{eq:AC Characteristics} \begin{array}{ c c c } \mbox{Standard Operating Conditions (unless otherwise specified)} \\ Operating Temperature \\ Operating Temperature \\ -40^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$							
Param Symbol Characteristic Min Typ† Ma					Мах	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000*		_	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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19.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. Tp	pS	
Т		
F	Frequency	T Time
Lowe	ercase letters (pp) and their meanings:	
рр		
2	to	mc MCLR
ck	CLKOUT	osc oscillator
су	cycle time	os OSC1
drt	device reset timer	t0 T0CKI
io	I/O port	wdt watchdog timer
Uppe	ercase letters and their meanings:	
S		
F	Fall	P Period
н	High	R Rise
Ι	Invalid (Hi-impedance)	V Valid
L	Low	Z Hi-impedance

FIGURE 19-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS -PIC16C54C/C55A/C56A/C57C/C58B-40











FIGURE 20-4: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD

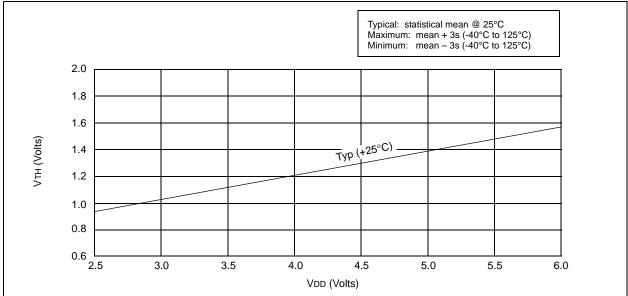
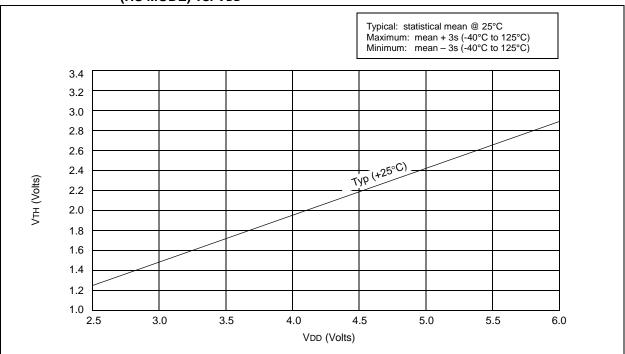


FIGURE 20-5: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (HS MODE) vs. VDD



21.0 PACKAGING INFORMATION

21.1 Package Marketing Information

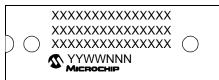
18-Lead PDIP



28-Lead Skinny PDIP (.300")



28-Lead PDIP (.600")



18-Lead SOIC



28-Lead SOIC

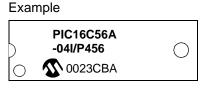


20-Lead SSOP



28-Lead SSOP

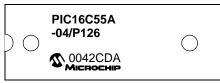




Example



Example



Example



Example



Example



Example



28-Lead Ceramic Dual In-line with Window (JW) - 600 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units				MILLIMETERS			
Dimensior	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.100			2.54		
Top to Seating Plane	Α	.195	.210	.225	4.95	5.33	5.72	
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19	
Standoff	A1	.015	.038	.060	0.38	0.95	1.52	
Shoulder to Shoulder Width	Е	.595	.600	.625	15.11	15.24	15.88	
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36	
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85	
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81	
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30	
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65	
Lower Lead Width	В	.016	.020	.023	0.41	0.51	0.58	
Overall Row Spacing §	eB	.610	.660	.710	15.49	16.76	18.03	
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37	

Sontolling Parameter
Significant Characteristic
JEDEC Equivalent: MO-103
Drawing No. C04-013

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PART NO.	- <u>xx</u>	Ť	<u>/xx</u>	<u>xxx</u>	Exa	nples	S:
Device	Frequency Range/OSC Type PIC16C54 PIC16C54A PIC16C54C PIC16C55A PIC16C55A PIC16C55A PIC16C56A PIC16C56A PIC16C57C PIC16C57C PIC16C58B PIC16C58B	Temperature Range	$\begin{array}{c} -(2) \\ \lambda_{T}(2) \\ (2) \\ C_{T}(2) \\ C_{T}(2) \\ 2) \\ -(2) \\ -(2) \\ \lambda_{T}(2) \\ 2) \\ -(2) \\ C_{T}(2) \\ C_{T}(2) \\ -(2) \\ -(2) \\ C_{T}(2) \\ -(2)$	Pattern	a) b) c) d) Note	PDIP QTP PIC16 packa PIC16 cial te dard ' PIC1 temp MHz, #123	C = normal voltage range LC = extended
Frequency Range/ Oscillator Type	04 200 KHz (LI 10 10 MHz (HS 20 20 MHz (HS 40 40 MHz (HS b ⁽⁴⁾ No oscillato *RC/LP/XT/HS a -02 is available for -04/10/20 options	Crystal ystal/Resonator Crystal P) or 2 MHz (XT an P) or 4 MHz (XT an conly) conly) conly) r type for JW packa re for 16C54/55/56/	nd RC) ages ⁽³⁾ /57 devices on all other device	S		3:	T = in tape and reel - SOIC and SSOP packages only JW Devices are UV erasable and can be programmed to any device configura- tion. JW Devices meet the electrical requirements of each oscillator type, including LC devices. b = Blank
Temperature Range	$b^{(4)} = 0^{\circ}C$ $I = -40^{\circ}C$ $E = -40^{\circ}C$	to +85°C					
Package	JW = 28-pin DIP ⁽³⁾ P = 28-pin SO = 300 m SS = 209 m SP = 28-pin	Waffle Pack 600 mil/18-pin 300 600 mil/18-pin 300 il SOIC il SSOP 300 mil Skinny PD for additional packa	0 mil PDIP DIP				
Pattern		I code (factory spe lank for OTP and W					

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