## What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "**Embedded - Microcontrollers**"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 12 |
| Program Memory Size | 3KB (2K x 12) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 73 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lc58bt-04i-ss |

# PIC16C5X

## 8-Bit EPROM/ROM-Based CMOS Microcontrollers

## 1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low cost, high performance, 8-bit fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches which take two cycles. The PIC16C5X delivers performance in an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external RESET circuitry. There are four oscillator configurations to choose from, including the power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and Code Protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

## 1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high speed automotive and appliance motor control to low power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low cost, low power, high performance ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, co-processor applications).

## 4.0 OSCILLATOR CONFIGURATIONS

### 4.1 Oscillator Types

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

1. LP: Low Power Crystal
2. XT: Crystal/Resonator
3. HS: High Speed Crystal/Resonator
4. RC: Resistor/Capacitor

> **Note:** Not all oscillator selections available for all parts. See Section 9.1.

### 4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

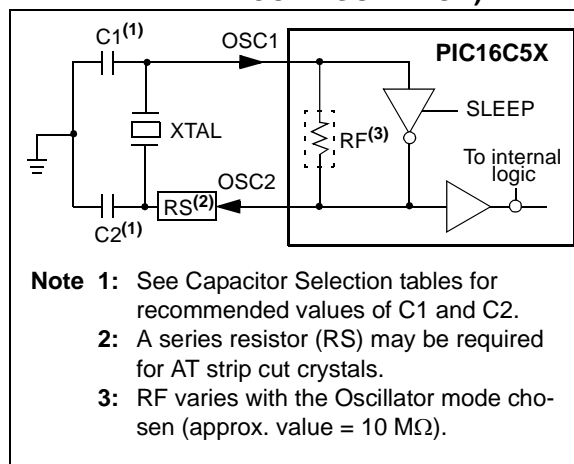**FIGURE 4-1:** CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



**Note 1:** See Capacitor Selection tables for recommended values of C1 and C2.
**2:** A series resistor (RS) may be required for AT strip cut crystals.
**3:** RF varies with the Oscillator mode chosen (approx. value = 10 MΩ).

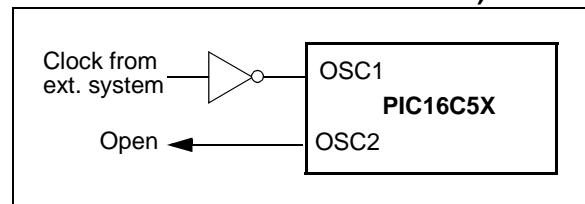**FIGURE 4-2:** EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



**TABLE 4-1:** CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16C5X, PIC16CR5X

| Osc Type | Resonator Freq | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| XT | 455 kHz | 68-100 pF | 68-100 pF |
|  | 2.0 MHz | 15-33 pF | 15-33 pF |
|  | 4.0 MHz | 10-22 pF | 10-22 pF |
| HS | 8.0 MHz | 10-22 pF | 10-22 pF |
|  | 16.0 MHz | 10 pF | 10 pF |

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 4-2:** CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C5X, PIC16CR5X

| Osc Type | Crystal Freq | Cap.Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz[1] | 15 pF | 15 pF |
| XT | 100 kHz | 15-30 pF | 200-300 pF |
|  | 200 kHz | 15-30 pF | 100-200 pF |
|  | 455 kHz | 15-30 pF | 15-100 pF |
|  | 1 MHz | 15-30 pF | 15-30 pF |
|  | 2 MHz | 15 pF | 15 pF |
|  | 4 MHz | 15 pF | 15 pF |
| HS | 4 MHz | 15 pF | 15 pF |
|  | 8 MHz | 15 pF | 15 pF |
|  | 20 MHz | 15 pF | 15 pF |

**Note 1:** For $V_{DD} > 4.5V$, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

> **Note:** If you change from this device to another device, please verify oscillator characteristics in your application.

## 5.0    RESET

PIC16C5X devices may be RESET in one of the following ways:

- Power-On Reset (POR)
- $\overline{\text{MCLR}}$ Reset (normal operation)
- $\overline{\text{MCLR}}$ Wake-up Reset (from SLEEP)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from SLEEP)

Table 5-1 shows these RESET conditions for the PCL and STATUS registers.

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-On Reset (POR), $\overline{\text{MCLR}}$ or WDT Reset. A $\overline{\text{MCLR}}$ or WDT wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS <4:3>) are set or cleared depending on the different RESET conditions (Table 5-1). These bits may be used to determine the nature of the RESET.

Table 5-3 lists a full description of RESET states of all registers. Figure 5-1 shows a simplified block diagram of the On-chip Reset circuit.

### TABLE 5-1:    STATUS BITS AND THEIR SIGNIFICANCE

| Condition | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ |
|---|---|---|
| Power-On Reset | 1 | 1 |
| $\overline{\text{MCLR}}$ Reset (normal operation) | u | u |
| $\overline{\text{MCLR}}$ Wake-up (from SLEEP) | 1 | 0 |
| WDT Reset (normal operation) | 0 | 1 |
| WDT Wake-up (from SLEEP) | 0 | 0 |

Legend:    u = unchanged, x = unknown, − = unimplemented read as '0'.

### TABLE 5-2:    SUMMARY OF REGISTERS ASSOCIATED WITH RESET

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR | Value on $\overline{\text{MCLR}}$ and WDT Reset |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 03h | STATUS | PA2 | PA1 | PA0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 0001 1xxx | 000q quuu |

Legend:    u = unchanged, x = unknown, q = see Table 5-1 for possible values.

**NOTES:**

# PIC16C5X

## 6.2    Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 6-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-6).

### 6.2.1    GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 6.7.

**FIGURE 6-4:    PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER FILE MAP**

| File Address | |
|---|---|
| 00h | INDF[1] |
| 01h | TMR0 |
| 02h | PCL |
| 03h | STATUS |
| 04h | FSR |
| 05h | PORTA |
| 06h | PORTB |
| 07h | PORTC[2] |
| 08h | |
| | General Purpose Registers |
| 1Fh | |

**Note 1:** Not a physical register. See Section 6.7.
**2:** PIC16C55 only, in all other devices this is implemented as a a general purpose register.
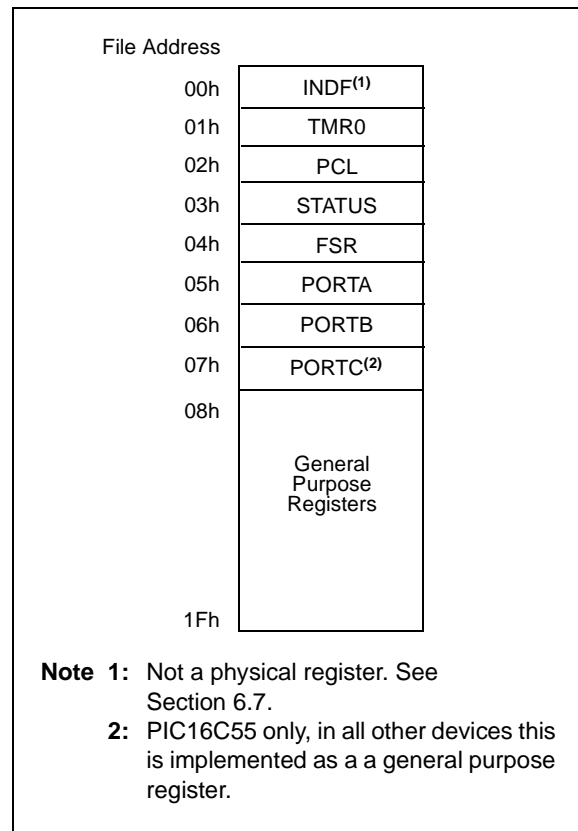
# PIC16C5X

| **IORLW** | **Inclusive OR literal with W** |
|---|---|
| Syntax: | [ *label* ]   IORLW   k |
| Operands: | $0 \leq k \leq 255$ |
| Operation: | (W) .OR. (k) $\rightarrow$ (W) |
| Status Affected: | Z |

Encoding:

| 1101 | kkkk | kkkk |
|---|---|---|

| Description: | The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register. |
|---|---|
| Words: | 1 |
| Cycles: | 1 |
| Example: | IORLW   0x35 |

Before Instruction
 W   =   0x9A
After Instruction
 W   =   0xBF
 Z   =   0

| **IORWF** | **Inclusive OR W with f** |
|---|---|
| Syntax: | [ *label* ]   IORWF   f,d |
| Operands: | $0 \leq f \leq 31$<br>$d \in [0,1]$ |
| Operation: | (W).OR. (f) $\rightarrow$ (dest) |
| Status Affected: | Z |

Encoding:

| 0001 | 00df | ffff |
|---|---|---|

| Description: | Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. |
|---|---|
| Words: | 1 |
| Cycles: | 1 |
| Example: | IORWF        RESULT, 0 |

Before Instruction
 RESULT   =   0x13
 W        =   0x91
After Instruction
 RESULT   =   0x13
 W        =   0x93
 Z        =   0

| **MOVF** | **Move f** |
|---|---|
| Syntax: | [ *label* ]   MOVF   f,d |
| Operands: | $0 \leq f \leq 31$<br>$d \in [0,1]$ |
| Operation: | (f) $\rightarrow$ (dest) |
| Status Affected: | Z |

Encoding:

| 0010 | 00df | ffff |
|---|---|---|

| Description: | The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected. |
|---|---|
| Words: | 1 |
| Cycles: | 1 |
| Example: | MOVF   FSR,   0 |

After Instruction
 W   =   value in FSR register

| **MOVLW** | **Move Literal to W** |
|---|---|
| Syntax: | [ *label* ]   MOVLW   k |
| Operands: | $0 \leq k \leq 255$ |
| Operation: | k $\rightarrow$ (W) |
| Status Affected: | None |

Encoding:

| 1100 | kkkk | kkkk |
|---|---|---|

| Description: | The eight bit literal 'k' is loaded into the W register. |
|---|---|
| Words: | 1 |
| Cycles: | 1 |
| Example: | MOVLW   0x5A |

After Instruction
 W   =   0x5A

**Preliminary**

# PIC16C5X

## 12.7 Timing Diagrams and Specifications

**FIGURE 12-2:** **EXTERNAL CLOCK TIMING - PIC16C54/55/56/57**
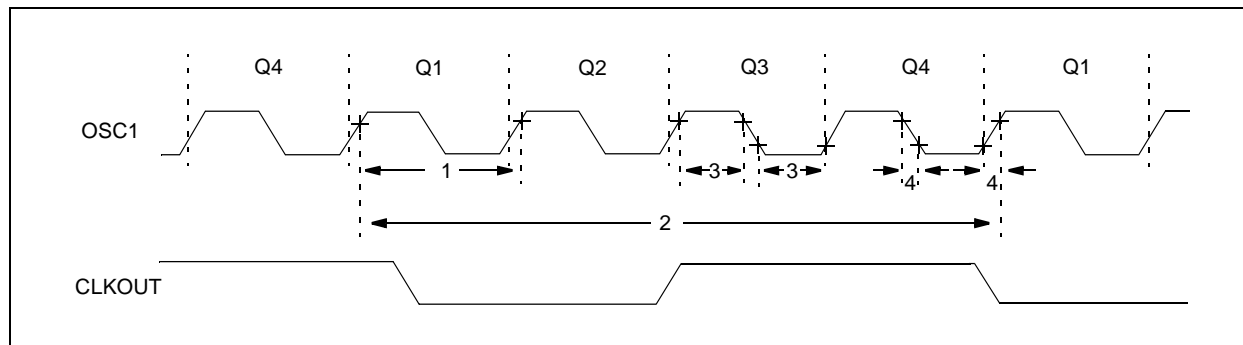


**TABLE 12-1:** **EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified) Operating Temperature   0°C ≤ TA ≤ +70°C for commercial −40°C ≤ TA ≤ +85°C for industrial −40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
| 1A | FOSC | External CLKIN Frequency[1] | DC | — | 4.0 | MHz | XT OSC mode |
| | | | DC | — | 10 | MHz | 10 MHz mode |
| | | | DC | — | 20 | MHz | HS OSC mode (Comm/Ind) |
| | | | DC | — | 16 | MHz | HS OSC mode (Ext) |
| | | | DC | — | 40 | kHz | LP OSC mode |
| | | Oscillator Frequency[1] | DC | — | 4.0 | MHz | RC OSC mode |
| | | | 0.1 | — | 4.0 | MHz | XT OSC mode |
| | | | 4.0 | — | 10 | MHz | 10 MHz mode |
| | | | 4.0 | — | 20 | MHz | HS OSC mode (Comm/Ind) |
| | | | 4.0 | — | 16 | MHz | HS OSC mode (Ext) |
| | | | DC | — | 40 | kHz | LP OSC mode |

\*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

# PIC16C5X

## 13.4    DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature    –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
| D030 | VIL | **Input Low Voltage**<br>I/O ports<br>MCLR (Schmitt Trigger)<br>T0CKI (Schmitt Trigger)<br>OSC1 (Schmitt Trigger)<br>OSC1 | Vss<br>Vss<br>Vss<br>Vss<br>Vss | —<br>—<br>—<br>—<br>— | 0.15 VDD<br>0.15 VDD<br>0.15 VDD<br>0.15 VDD<br>0.3 VDD | V<br>V<br>V<br>V<br>V | Pin at hi-impedance<br><br><br>RC mode only[3]<br>XT, HS and LP modes |
| D040 | VIH | **Input High Voltage**<br>I/O ports<br>I/O ports<br>I/O ports<br>MCLR (Schmitt Trigger)<br>T0CKI (Schmitt Trigger)<br>OSC1 (Schmitt Trigger)<br>OSC1 | 0.45 VDD<br>2.0<br>0.36 VDD<br>0.85 VDD<br>0.85 VDD<br>0.85 VDD<br>0.7 VDD | —<br>—<br>—<br>—<br>—<br>—<br>— | VDD<br>VDD<br>VDD<br>VDD<br>VDD<br>VDD<br>VDD | V<br>V<br>V<br>V<br>V<br>V<br>V | For all VDD[4]<br>4.0V < VDD ≤ 5.5V[4]<br>VDD > 5.5V<br><br><br>RC mode only[3]<br>XT, HS and LP modes |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current**[1,2]<br>I/O ports<br><br>MCLR<br>MCLR<br>T0CKI<br>OSC1 | −1.0<br><br>−5.0<br>—<br>−3.0<br>−3.0 | 0.5<br><br>—<br>0.5<br>0.5<br>0.5 | +1.0<br><br>—<br>+5.0<br>+3.0<br>+3.0 | μA<br><br>μA<br>μA<br>μA<br>μA | **For VDD ≤ 5.5V:**<br>VSS ≤ VPIN ≤ VDD,<br>pin at hi-impedance<br>VPIN = VSS + 0.25V<br>VPIN = VDD<br>VSS ≤ VPIN ≤ VDD<br>VSS ≤ VPIN ≤ VDD,<br>XT, HS and LP modes |
| D080 | VOL | **Output Low Voltage**<br>I/O ports<br>OSC2/CLKOUT | —<br>— | —<br>— | 0.6<br>0.6 | V<br>V | IOL = 8.7 mA, VDD = 4.5V<br>IOL = 1.6 mA, VDD = 4.5V,<br>RC mode only |
| D090 | VOH | **Output High Voltage**[2]<br>I/O ports<br>OSC2/CLKOUT | VDD − 0.7<br>VDD − 0.7 | —<br>— | —<br>— | V<br>V | IOH = −5.4 mA, VDD = 4.5V<br>IOH = −1.0 mA, VDD = 4.5V,<br>RC mode only |

\*    These parameters are characterized but not tested.

†    Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note  1:**   The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:**   Negative current is defined as coming out of the pin.

**3:**   For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:**   The user may use the better of the two specifications.

**Preliminary**

**FIGURE 13-4:** **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A**



**Note 1:** Please refer to Figure 13.1 for load conditions.
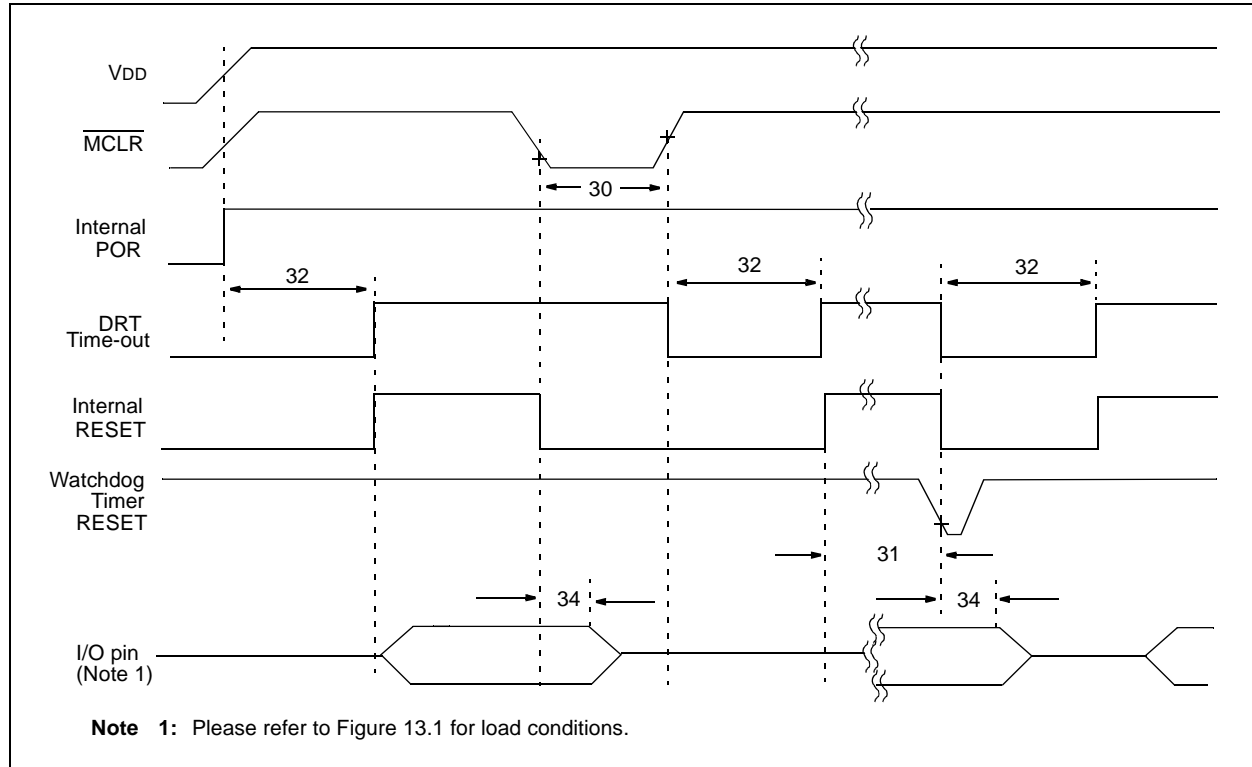
**TABLE 13-3:** **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A**

| AC Characteristics | | **Standard Operating Conditions** (unless otherwise specified) Operating Temperature $\quad 0°C \leq T_A \leq +70°C$ for commercial $\quad\quad -40°C \leq T_A \leq +85°C$ for industrial $\quad\quad -40°C \leq T_A \leq +125°C$ for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 1.0* | — | — | μs | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7.0* | 18* | 40* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 7.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | TioZ | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | — | — | 1.0* | μs | |

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# PIC16C5X

**FIGURE 14-2:** **TYPICAL RC OSC FREQUENCY vs. V_DD, CEXT = 20 PF**
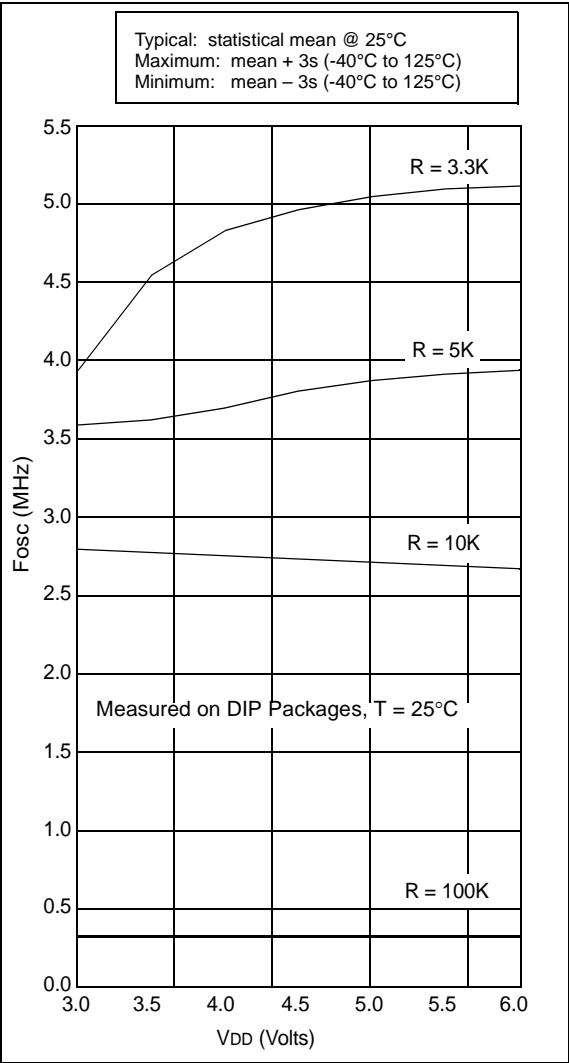


**FIGURE 14-3:** **TYPICAL RC OSC FREQUENCY vs. V_DD, CEXT = 100 PF**

**Preliminary** © 1997-2013 Microchip Technology Inc.
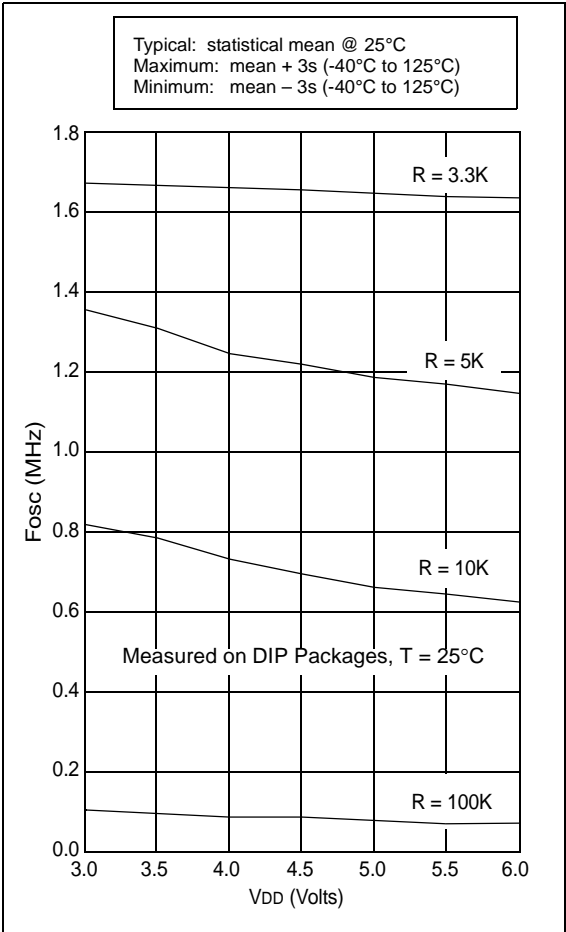
**FIGURE 14-13:** MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK, −40°C TO +85°C)



Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean − 3s (-40°C to 125°C)
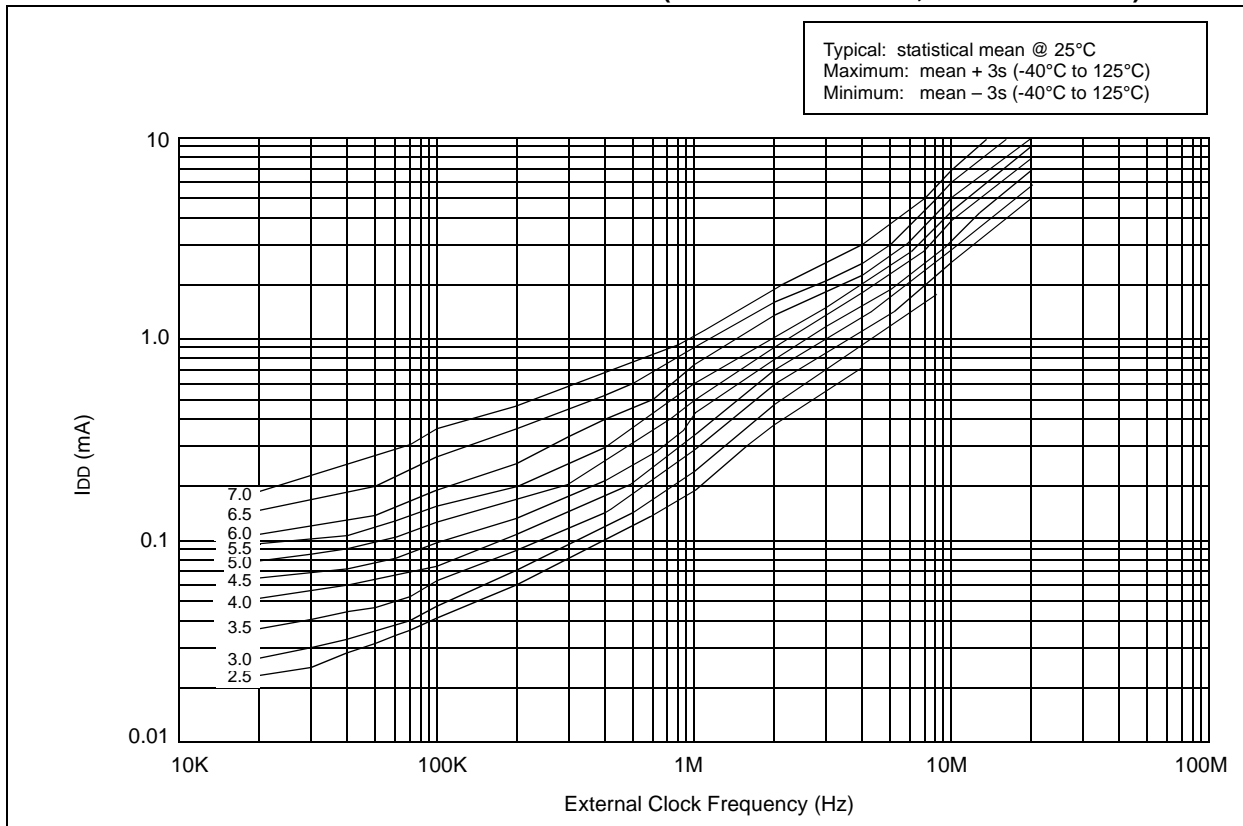
**FIGURE 14-14:** MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK −55°C TO +125°C)



Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean − 3s (-40°C to 125°C)
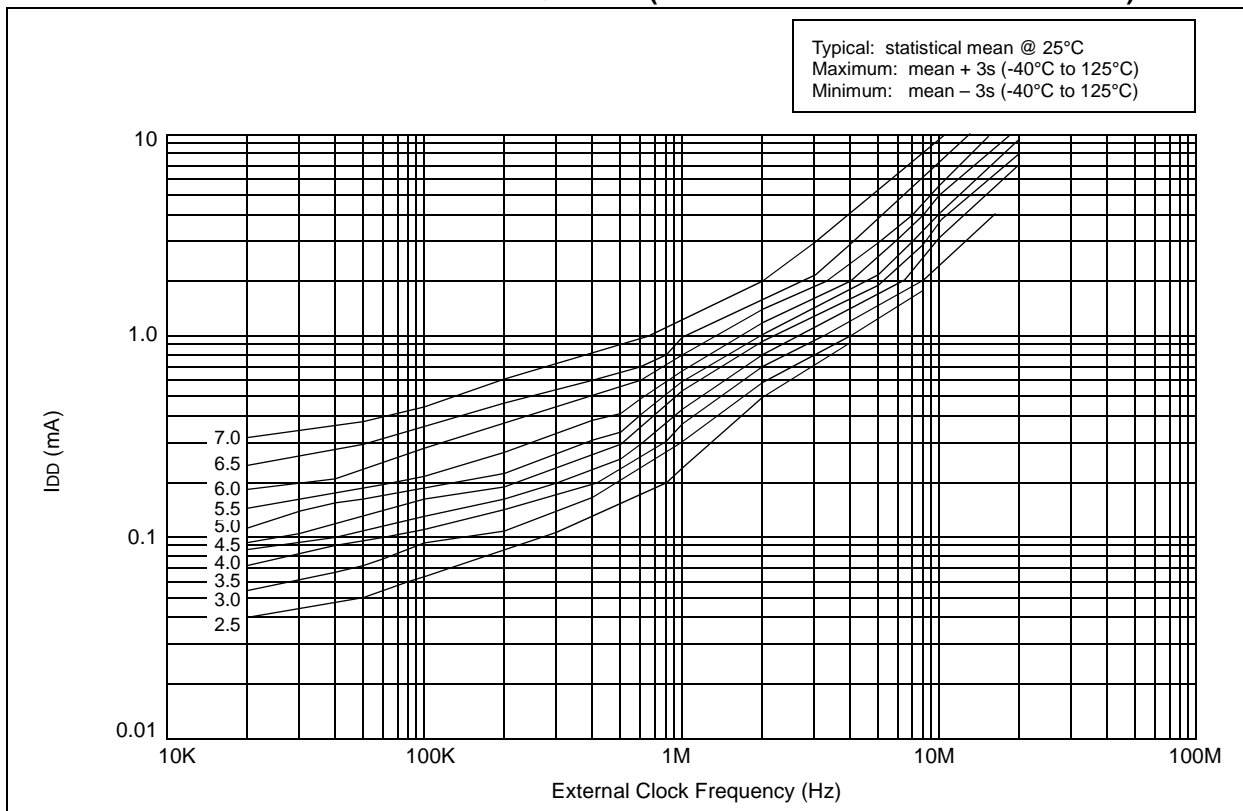
**FIGURE 14-17:** **TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**
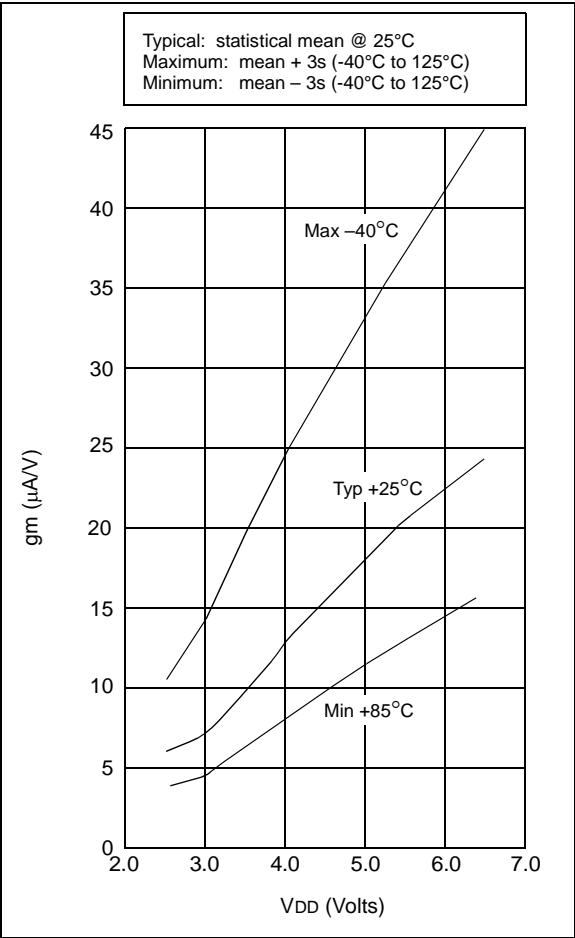


**FIGURE 14-18:** **TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**
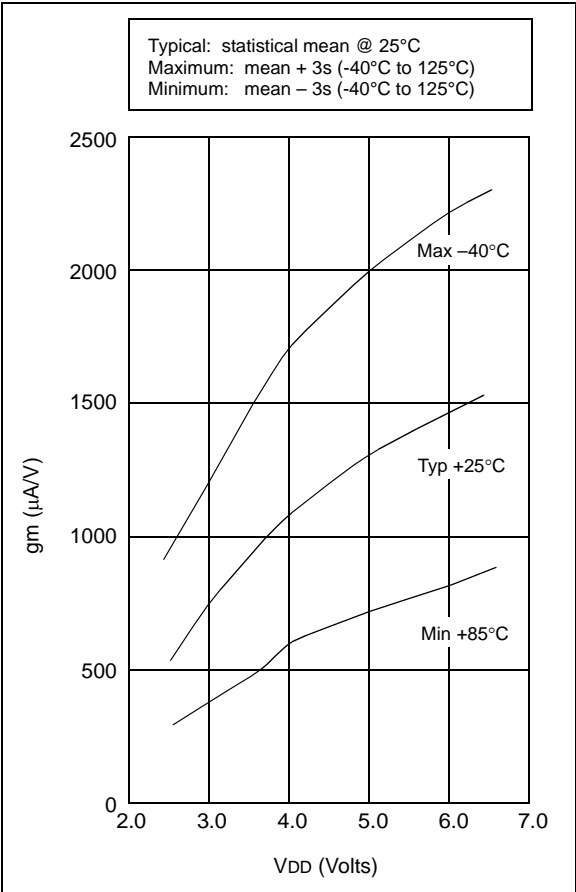
# PIC16C5X

**FIGURE 15-4:** **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A**



**Note 1:** Please refer to Figure 15-1 for load conditions.
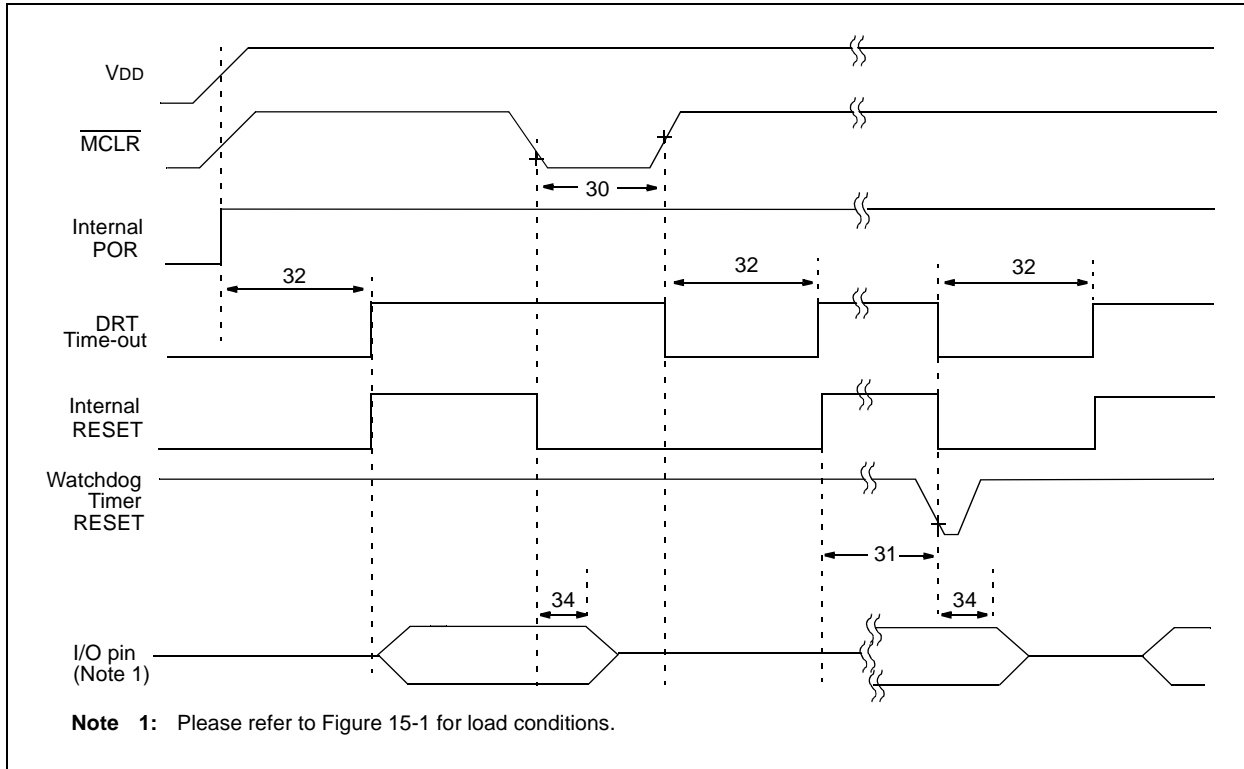
**TABLE 15-3:** **RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A**

| AC Characteristics | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature $\quad$ $0°C \leq TA \leq +70°C$ for commercial $\quad -40°C \leq TA \leq +85°C$ for industrial $\quad -20°C \leq TA \leq +85°C$ for industrial - PIC16LV54A-02I $\quad -40°C \leq TA \leq +125°C$ for extended | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
| 30 | TmcL | $\overline{MCLR}$ Pulse Width (low) | 100*<br>1 | —<br>— | —<br>— | ns<br>µs | VDD = 5.0V<br>VDD = 5.0V (PIC16LV54A only) |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | TioZ | I/O Hi-impedance from $\overline{MCLR}$ Low | —<br>— | —<br>— | 100*<br>1µs | ns<br>— | (PIC16LV54A only) |

$\quad$ * These parameters are characterized but not tested.

$\quad$ † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 15-5:** **TIMER0 CLOCK TIMINGS - PIC16C54A**



T0CKI

40 41

42

**Note:** Please refer to Figure 15-1 for load conditions.
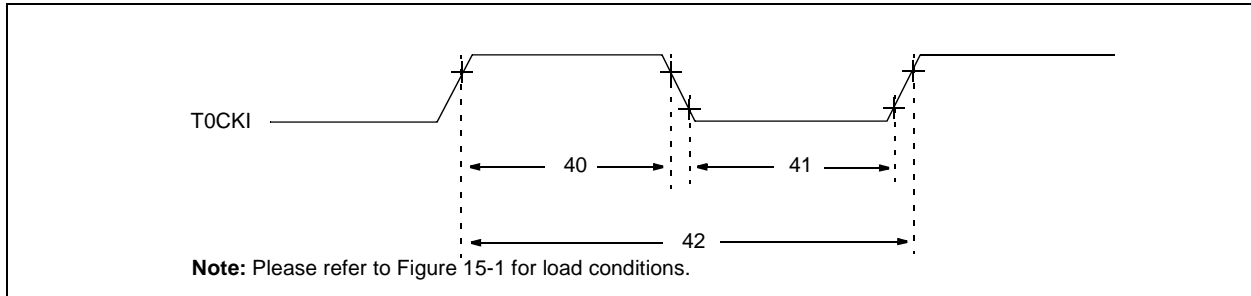
**TABLE 15-4:** **TIMER0 CLOCK REQUIREMENTS - PIC16C54A**

| AC Characteristics | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature $\quad 0°C \leq T_A \leq +70°C$ for commercial<br>$-40°C \leq T_A \leq +85°C$ for industrial<br>$-20°C \leq T_A \leq +85°C$ for industrial - PIC16LV54A-02I<br>$-40°C \leq T_A \leq +125°C$ for extended | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
| 40 | Tt0H | T0CKI High Pulse Width | | | | | |
| | | - No Prescaler | 0.5 Tcy + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | | | | | |
| | | - No Prescaler | 0.5 Tcy + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | $\frac{20 \text{ or } Tcy + 40^*}{N}$ | — | — | ns | Whichever is greater.<br>N = Prescale Value<br>(1, 2, 4,..., 256) |

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## 17.2    DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended)
##              PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

| PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E<br>PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E<br>(Extended) | | | | | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature    −40°C ≤ TA ≤ +125°C for extended |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
| D001 | VDD | **Supply Voltage** | 3.0<br>4.5 | —<br>— | 5.5<br>5.5 | V<br>V | RC, XT, LP, and HS mode<br>from 0 - 10 MHz<br>from 10 - 20 MHz |
| D002 | VDR | **RAM Data Retention Voltage**[1] | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD start voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD rise rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current**[2]<br>XT and RC[3] modes<br>HS mode | —<br>— | 1.8<br>9.0 | 3.3<br>20 | mA<br>mA | FOSC = 4.0 MHz, VDD = 5.5V<br>FOSC = 20 MHz, VDD = 5.5V |
| D020 | IPD | **Power-down Current**[2] | —<br>—<br>—<br>—<br>—<br>— | 0.3<br>10<br>12<br>4.8<br>18<br>26 | 17<br>50*<br>60*<br>31*<br>68*<br>90* | μA<br>μA<br>μA<br>μA<br>μA<br>μA | VDD = 3.0V, WDT disabled<br>VDD = 4.5V, WDT disabled<br>VDD = 5.5V, WDT disabled<br>VDD = 3.0V, WDT enabled<br>VDD = 4.5V, WDT enabled<br>VDD = 5.5V, WDT enabled |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

    a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

    b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

# PIC16C5X

## 17.3 DC Characteristics: 
PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended)
PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial)
PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended)
PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \leq T_A \leq +70°C$ for commercial $-40°C \leq T_A \leq +85°C$ for industrial $-40°C \leq T_A \leq +125°C$ for extended | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
| D030 | $V_{IL}$ | **Input Low Voltage** I/O Ports I/O Ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 | $V_{SS}$ $V_{SS}$ $V_{SS}$ $V_{SS}$ $V_{SS}$ $V_{SS}$ | — — — — — — | 0.8 V $0.15 V_{DD}$ $0.15 V_{DD}$ $0.15 V_{DD}$ $0.15 V_{DD}$ $0.3 V_{DD}$ | V V V V V V | $4.5V < V_{DD} \leq 5.5V$ Otherwise RC mode only[3] XT, HS and LP modes |
| D040 | $V_{IH}$ | **Input High Voltage** I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 | 2.0 $0.25 V_{DD}+0.8$ $0.85 V_{DD}$ $0.85 V_{DD}$ $0.85 V_{DD}$ $0.7 V_{DD}$ | — — — — — — | $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ | V V V V V V | $4.5V < V_{DD} \leq 5.5V$ Otherwise RC mode only[3] XT, HS and LP modes |
| D050 | $V_{HYS}$ | **Hysteresis of Schmitt Trigger inputs** | $0.15 V_{DD}$* | — | — | V | |
| D060 | $I_{IL}$ | **Input Leakage Current**[1,2] I/O ports MCLR MCLR T0CKI OSC1 | -1.0 -5.0 -3.0 -3.0 | 0.5 — 0.5 0.5 0.5 | +1.0 +5.0 +3.0 +3.0 — | µA µA µA µA µA | **For $V_{DD} \leq 5.5V$:** $V_{SS} \leq V_{PIN} \leq V_{DD}$, pin at hi-impedance $V_{PIN} = V_{SS} +0.25V$ $V_{PIN} = V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP modes |
| D080 | $V_{OL}$ | **Output Low Voltage** I/O ports OSC2/CLKOUT | — — | — — | 0.6 0.6 | V V | $I_{OL}$ = 8.7 mA, $V_{DD}$ = 4.5V $I_{OL}$ = 1.6 mA, $V_{DD}$ = 4.5V, RC mode only |
| D090 | $V_{OH}$ | **Output High Voltage**[2] I/O ports OSC2/CLKOUT | $V_{DD}$ - 0.7 $V_{DD}$ - 0.7 | — — | — — | V V | $I_{OH}$ = -5.4 mA, $V_{DD}$ = 4.5V $I_{OH}$ = -1.0 mA, $V_{DD}$ = 4.5V, RC mode only |

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**FIGURE 18-8:** VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD
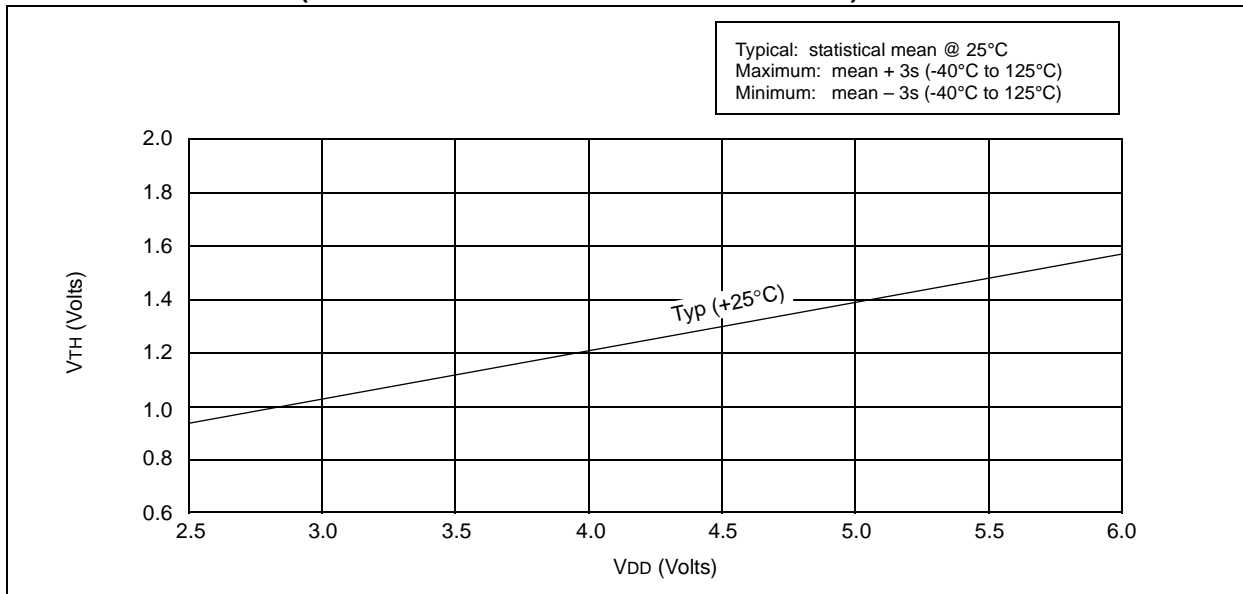


**FIGURE 18-9:** VIH, VIL OF $\overline{MCLR}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD



**Note:** These input pins have Schmitt Trigger input buffers.
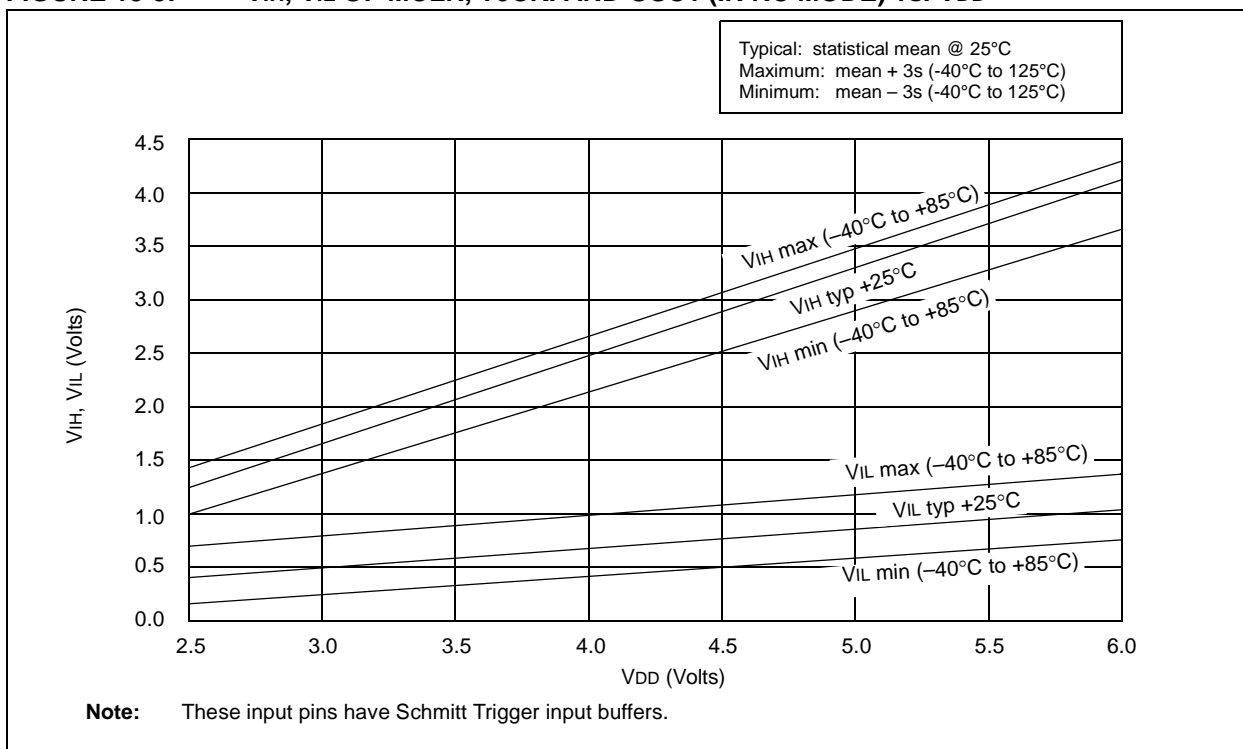
**FIGURE 18-16:** PORTA, B AND C I_OH vs. V_OH, V_DD = 5 V
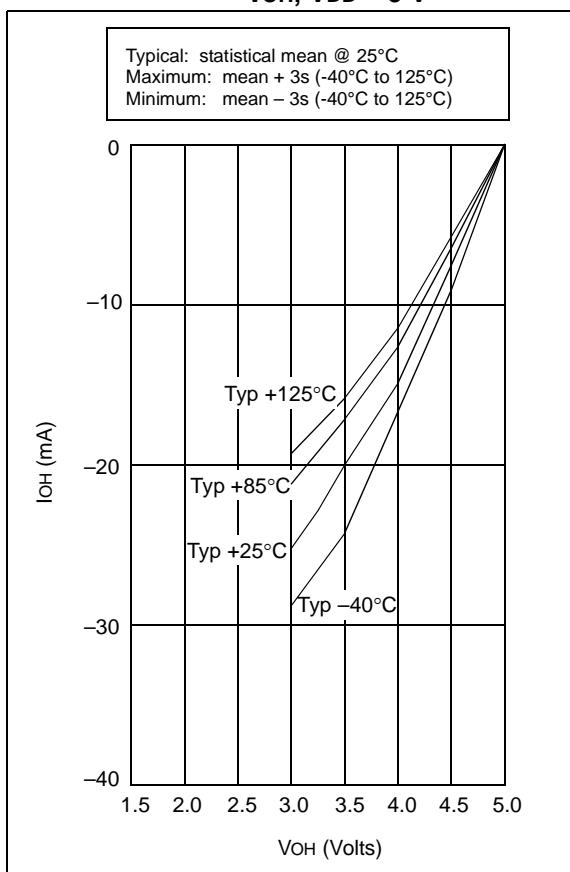


**FIGURE 18-17:** PORTA, B AND C I_OL vs. V_OL, V_DD = 3 V
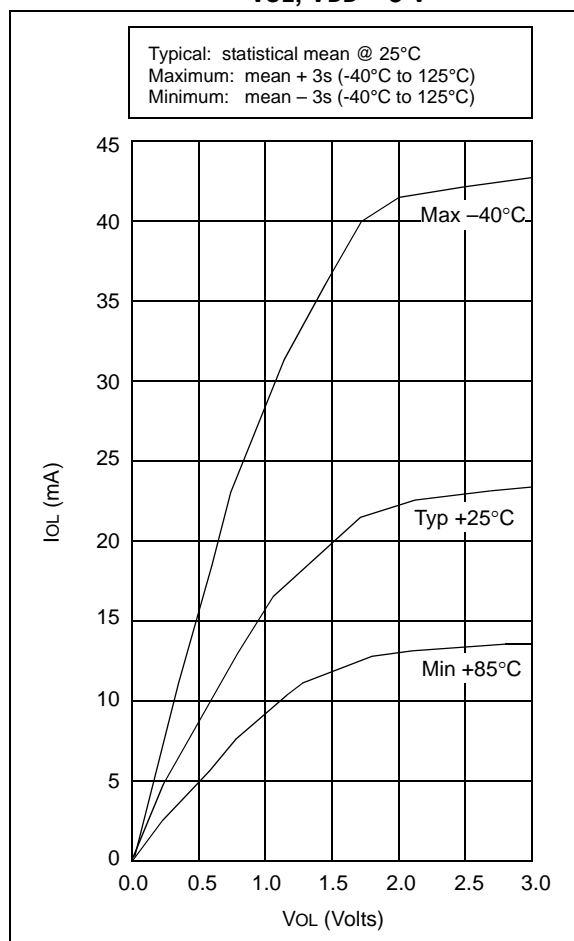
## 19.4    Timing Diagrams and Specifications

**FIGURE 19-3:**        **EXTERNAL CLOCK TIMING - PIC16C5X-40**
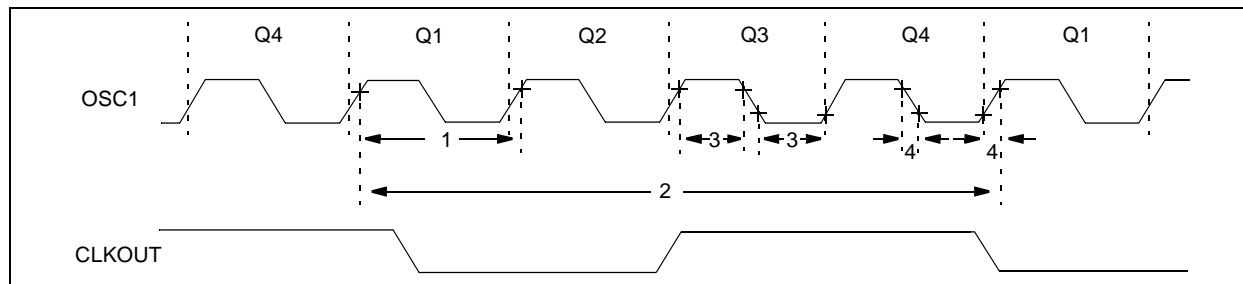


**TABLE 19-1:    EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X-40**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified) Operating Temperature        0°C ≤ TA ≤ +70°C for commercial | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
| | FOSC | External CLKIN Frequency[1] | 20 | — | 40 | MHz | HS OSC mode |
| 1 | TOSC | External CLKIN Period[1] | 25 | — | — | ns | HS OSC mode |
| 2 | Tcy | Instruction Cycle Time[2] | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 6.0* | — | — | ns | HS oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 6.5* | ns | HS oscillator |

    *    These parameters are characterized but not tested.

    †    Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note  1:**  All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
   When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

    **2:**  Instruction cycle period (TCY) equals four times the input oscillator time base period.

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