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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.8V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lv54a-02-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16lv54a-02-p</a>

# PIC16C5X

**TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	SOIC	SSOP			
RA0	6	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	7	6	I/O	TTL	
RA2	8	8	7	I/O	TTL	
RA3	9	9	8	I/O	TTL	
RB0	10	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	11	10	I/O	TTL	
RB2	12	12	11	I/O	TTL	
RB3	13	13	12	I/O	TTL	
RB4	14	14	13	I/O	TTL	
RB5	15	15	15	I/O	TTL	
RB6	16	16	16	I/O	TTL	
RB7	17	17	17	I/O	TTL	
RC0	18	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	19	I/O	TTL	
RC2	20	20	20	I/O	TTL	
RC3	21	21	21	I/O	TTL	
RC4	22	22	22	I/O	TTL	
RC5	23	23	23	I/O	TTL	
RC6	24	24	24	I/O	TTL	
RC7	25	25	25	I/O	TTL	
T0CKI	1	1	2	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
$\overline{\text{MCLR}}$	28	28	28	I	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
OSC1/CLKIN	27	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	2	2	3,4	P	—	Positive supply for logic and I/O pins.
Vss	4	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	3,5	—	—	—	Unused, do not connect.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

# PIC16C5X

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NOTES:

# PIC16C5X

## 9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a `SLEEP` instruction. During normal operation or `SLEEP`, a WDT Reset or Wake-up Reset generates a device RESET.

The  $\overline{TO}$  bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit `WDTE` as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

### 9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The `PSA` and `PS<2:0>` bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the `OPTION` register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, `VDD` and part-to-part process variations (see Device Characterization).

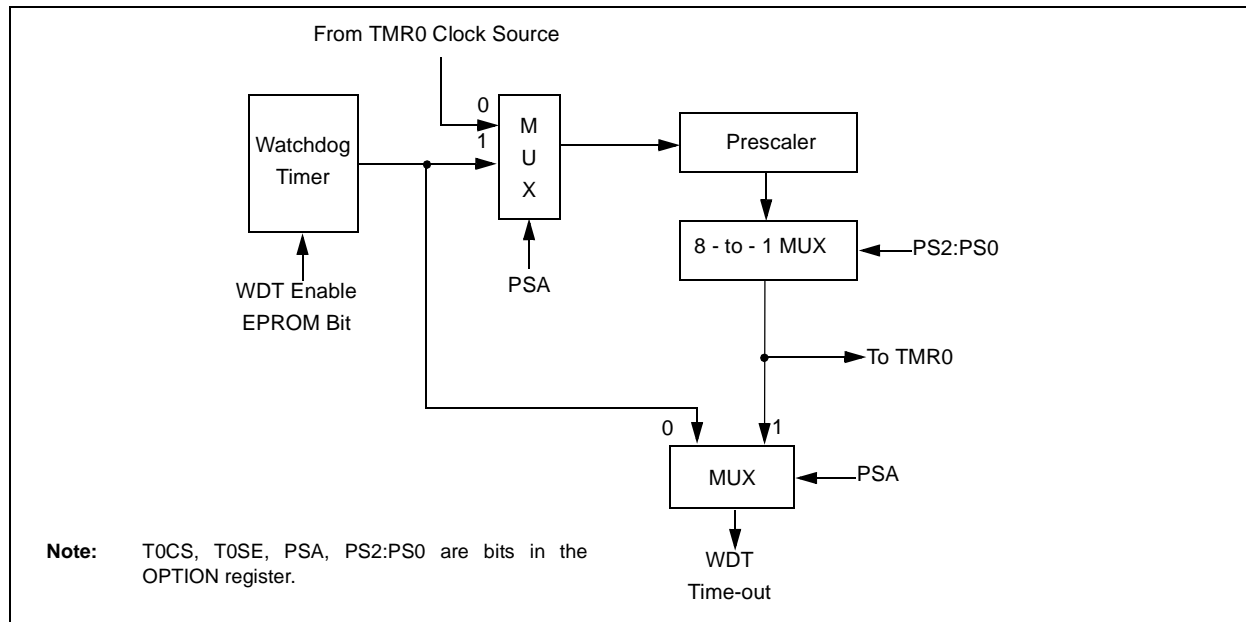
Under worst case conditions (`VDD` = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

### 9.2.2 WDT PROGRAMMING CONSIDERATIONS

The `CLRWDT` instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The `SLEEP` instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum `SLEEP` time before a WDT Wake-up Reset.

**FIGURE 9-1: WATCHDOG TIMER BLOCK DIAGRAM**



**TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	OPTION	—	—	Tosc	Tose	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

CALL		Subroutine Call				
Syntax:	[ <i>label</i> ] CALL k					
Operands:	$0 \leq k \leq 255$					
Operation:	(PC) + 1 → TOS; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>					
Status Affected:	None					
Encoding:	<table border="1"><tr><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>			1001	kkkk	kkkk
1001	kkkk	kkkk				
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction.					
Words:	1					
Cycles:	2					
Example:	HERE CALL THERE					
Before Instruction						
PC = address (HERE)						
After Instruction						
PC = address (THERE)						
TOS = address (HERE + 1)						

CLRF	Clear f			
Syntax:	[ <i>label</i> ] CLRF f			
Operands:	$0 \leq f \leq 31$			
Operation:	00h $\rightarrow$ (f); 1 $\rightarrow$ Z			
Status Affected:	Z			
Encoding:	<table border="1"><tr><td>0000</td><td>011f</td><td>ffff</td></tr></table>	0000	011f	ffff
0000	011f	ffff		
Description:	The contents of register 'f' are cleared and the Z bit is set.			
Words:	1			
Cycles:	1			
Example:	CLRF FLAG_REG			
Before Instruction				
FLAG_REG	= 0x5A			
After Instruction				
FLAG_REG	= 0x00			
Z	= 1			

CLR W				
Syntax:	[ <i>label</i> ] CLRW			
Operands:	None			
Operation:	00h → (W); 1 → Z			
Status Affected:	Z			
Encoding:	<table border="1"><tr><td>0000</td><td>0100</td><td>0000</td></tr></table>	0000	0100	0000
0000	0100	0000		
Description:	The W register is cleared. Zero bit (Z) is set.			
Words:	1			
Cycles:	1			
Example:	CLR W			
Before Instruction				
W	= 0x5A			
After Instruction				
W	= 0x00			
Z	= 1			

CLRWD	Clear Watchdog Timer			
Syntax:	[ <i>label</i> ] CLRWD			
Operands:	None			
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → $\overline{TO}$ ; 1 → $\overline{PD}$			
Status Affected:	$\overline{TO}$ , $\overline{PD}$			
Encoding:	<table border="1"><tr><td>0000</td><td>0000</td><td>0100</td></tr></table>	0000	0000	0100
0000	0000	0100		
Description:	The CLRWD instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.			
Words:	1			
Cycles:	1			
Example:	CLRWD			
Before Instruction				
WDT counter	= ?			
After Instruction				
WDT counter	= 0x00			
WDT prescaler	= 0			
$\overline{TO}$	= 1			
$\overline{PD}$	= 1			

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## IORLW Inclusive OR literal with W

Syntax: [ *label* ] IORLW *k*  
Operands:  $0 \leq k \leq 255$   
Operation: (W).OR. (*k*) → (W)  
Status Affected: Z  
Encoding: 

1101	kkkk	kkkk
------	------	------

  
Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.  
Words: 1  
Cycles: 1  
Example: IORLW 0x35

Before Instruction  
W = 0x9A  
After Instruction  
W = 0xBF  
Z = 0

## IORWF Inclusive OR W with f

Syntax: [ *label* ] IORWF *f*,*d*  
Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$   
Operation: (W).OR. (*f*) → (*dest*)  
Status Affected: Z  
Encoding: 

0001	00df	ffff
------	------	------

  
Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.  
Words: 1  
Cycles: 1  
Example: IORWF RESULT, 0

Before Instruction  
RESULT = 0x13  
W = 0x91  
After Instruction  
RESULT = 0x13  
W = 0x93  
Z = 0

## MOVF Move f

Syntax: [ *label* ] MOVF *f*,*d*  
Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$   
Operation: (*f*) → (*dest*)  
Status Affected: Z  
Encoding: 

0010	00df	ffff
------	------	------

  
Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.  
Words: 1  
Cycles: 1  
Example: MOVF FSR, 0

After Instruction  
W = value in FSR register

## MOVLW Move Literal to W

Syntax: [ *label* ] MOVLW *k*  
Operands:  $0 \leq k \leq 255$   
Operation: *k* → (W)  
Status Affected: None  
Encoding: 

1100	kkkk	kkkk
------	------	------

  
Description: The eight bit literal 'k' is loaded into the W register.  
Words: 1  
Cycles: 1  
Example: MOVLW 0x5A

After Instruction  
W = 0x5A

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## RLF Rotate Left f through Carry

Syntax: [ *label* ] RLF f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

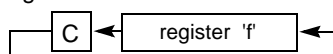
Operation: See description below

Status Affected: C

Encoding: 

0011	01df	ffff
------	------	------

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1,0

Before Instruction

REG1 = 1110 0110

C = 0

After Instruction

REG1 = 1110 0110

W = 1100 1100

C = 1

## RRF Rotate Right f through Carry

Syntax: [ *label* ] RRF f,d

Operands:  $0 \leq f \leq 31$   
 $d \in [0,1]$

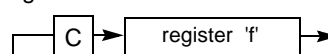
Operation: See description below

Status Affected: C

Encoding: 

0011	00df	ffff
------	------	------

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example: RRF REG1,0

Before Instruction

REG1 = 1110 0110

C = 0

After Instruction

REG1 = 1110 0110

W = 0111 0011

C = 0

## SLEEP Enter SLEEP Mode

Syntax: [ *label* ] SLEEP

Operands: None

Operation: 00h → WDT;  
 0 → WDT prescaler; if assigned  
 1 →  $\overline{TO}$ ;  
 0 →  $\overline{PD}$

Status Affected:  $\overline{TO}$ ,  $\overline{PD}$

Encoding: 

0000	0000	0011
------	------	------

Description: Time-out status bit ( $\overline{TO}$ ) is set. The power-down status bit ( $\overline{PD}$ ) is cleared. The WDT and its prescaler are cleared.  
 The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: SLEEP

# PIC16C5X

## 12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	V <sub>IL</sub>	<b>Input Low Voltage</b>					
		I/O ports	V <sub>SS</sub>	—	0.15 V <sub>DD</sub>	V	Pin at hi-impedance  PIC16C5X-RC only <sup>(3)</sup> PIC16C5X-XT, 10, HS, LP
		MCLR (Schmitt Trigger)	V <sub>SS</sub>	—	0.15 V <sub>DD</sub>	V	
		T0CKI (Schmitt Trigger)	V <sub>SS</sub>	—	0.15 V <sub>DD</sub>	V	
		OSC1 (Schmitt Trigger)	V <sub>SS</sub>	—	0.15 V <sub>DD</sub>	V	
		OSC1 (Schmitt Trigger)	V <sub>SS</sub>	—	0.3 V <sub>DD</sub>	V	
D040	V <sub>IH</sub>	<b>Input High Voltage</b>					
		I/O ports	0.45 V <sub>DD</sub>	—	V <sub>DD</sub>	V	For all V <sub>DD</sub> <sup>(4)</sup> 4.0V < V <sub>DD</sub> ≤ 5.5V <sup>(4)</sup> V <sub>DD</sub> > 5.5 V
		I/O ports	2.0	—	V <sub>DD</sub>	V	
		I/O ports	0.36 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
		MCLR (Schmitt Trigger)	0.85 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
		T0CKI (Schmitt Trigger)	0.85 V <sub>DD</sub>	—	V <sub>DD</sub>	V	PIC16C5X-RC only <sup>(3)</sup> PIC16C5X-XT, 10, HS, LP
		OSC1 (Schmitt Trigger)	0.85 V <sub>DD</sub>	—	V <sub>DD</sub>	V	
D050	V <sub>HYS</sub>	<b>Hysteresis of Schmitt Trigger inputs</b>	0.15 V <sub>DD</sub> *	—	—	V	
D060	I <sub>IL</sub>	<b>Input Leakage Current</b> <sup>(1,2)</sup>					<b>For V<sub>DD</sub> ≤ 5.5 V:</b> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , pin at hi-impedance V <sub>PIN</sub> = V <sub>SS</sub> + 0.25V V <sub>PIN</sub> = V <sub>DD</sub> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , PIC16C5X-XT, 10, HS, LP
		I/O ports	−1	0.5	+1	μA	
		MCLR	−5	—	—	μA	
		MCLR	—	0.5	+5	μA	
		T0CKI	−3	0.5	+3	μA	
D080	V <sub>OL</sub>	<b>Output Low Voltage</b>					
		I/O ports	—	—	0.6	V	I <sub>OL</sub> = 8.7 mA, V <sub>DD</sub> = 4.5V I <sub>OL</sub> = 1.6 mA, V <sub>DD</sub> = 4.5V, PIC16C5X-RC
D090	V <sub>OH</sub>	<b>Output High Voltage</b> <sup>(2)</sup>					
		I/O ports	V <sub>DD</sub> − 0.7	—	—	V	I <sub>OH</sub> = −5.4 mA, V <sub>DD</sub> = 4.5V I <sub>OH</sub> = −1.0 mA, V <sub>DD</sub> = 4.5V, PIC16C5X-RC
D090	V <sub>OH</sub>	OSC2/CLKOUT	V <sub>DD</sub> − 0.7	—	—	V	

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.



13.5 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T	T
F Frequency	T Time

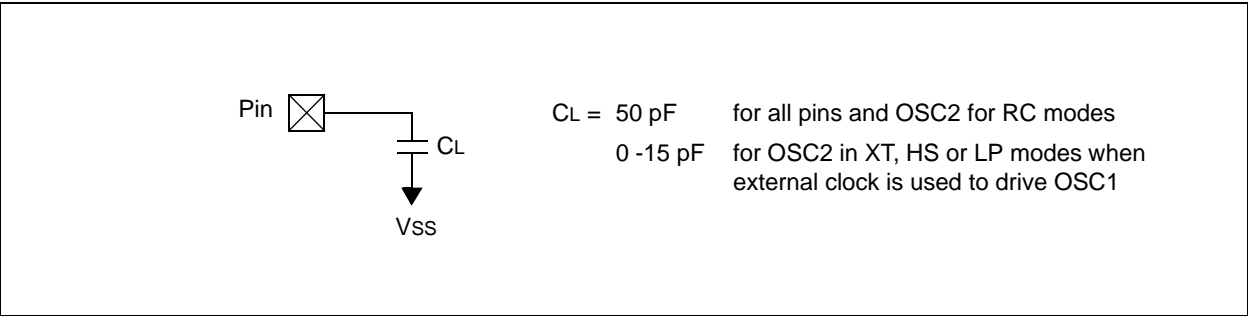
Lowercase letters (pp) and their meanings:

pp	mc MCLR
2 to	osc oscillator
ck CLKOUT	os OSC1
cy cycle time	t0 T0CKI
drt device reset timer	wdt watchdog timer
io I/O port	

Uppercase letters and their meanings:

S	P Period
F Fall	R Rise
H High	V Valid
I Invalid (Hi-impedance)	Z Hi-impedance
L Low	

FIGURE 13-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16CR54A



**TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A**

<b>Standard Operating Conditions (unless otherwise specified)</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1	Tosc	External CLKIN Period <sup>(1)</sup>	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period <sup>(1)</sup>	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode
2	Tcy	Instruction Cycle Time <sup>(2)</sup>	—	4/Fosc	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

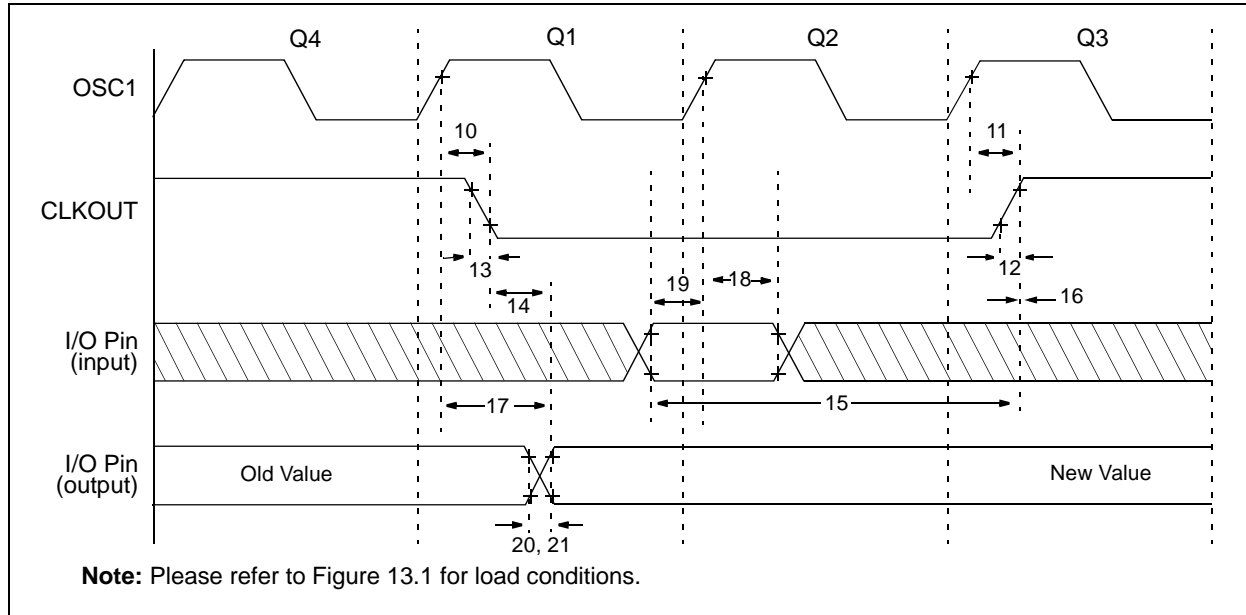
**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

# PIC16C5X

**FIGURE 13-3: CLKOUT AND I/O TIMING - PIC16CR54A**



**TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A**

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature				
		0°C ≤ TA ≤ +70°C for commercial				
		-40°C ≤ TA ≤ +85°C for industrial				
		-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ <sup>(1)</sup>	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ <sup>(1)</sup>	—	15	30**	ns
12	TckR	CLKOUT rise time <sup>(1)</sup>	—	5.0	15**	ns
13	TckF	CLKOUT fall time <sup>(1)</sup>	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid <sup>(1)</sup>	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ <sup>(1)</sup>	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ <sup>(1)</sup>	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid <sup>(2)</sup>	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time <sup>(2)</sup>	—	10	25**	ns
21	TioF	Port output fall time <sup>(2)</sup>	—	10	25**	ns

\* These parameters are characterized but not tested.

\*\* These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

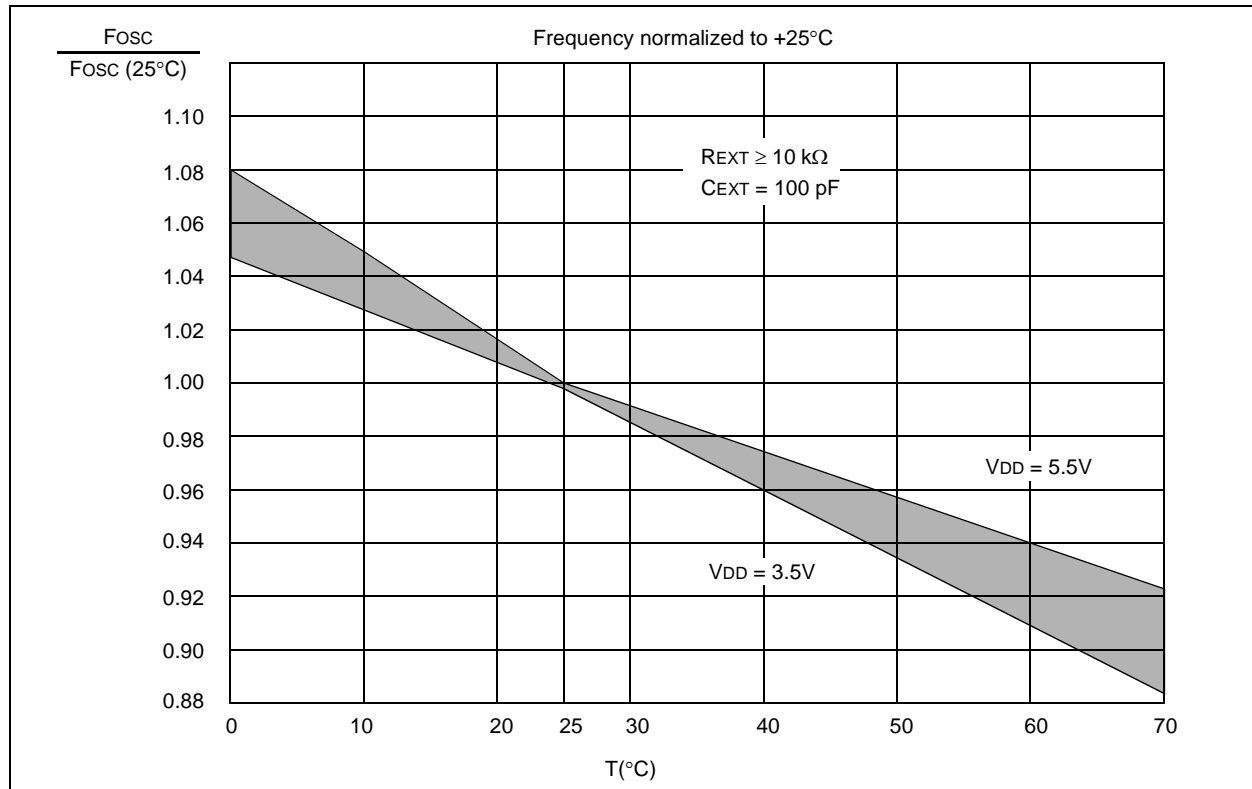
**2:** Please refer to Figure 13.1 for load conditions.

## 14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 $\sigma$ ) or (mean – 3 $\sigma$ ) respectively, where  $\sigma$  is a standard deviation, over the whole temperature range.

**FIGURE 14-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE**



**TABLE 14-1: RC OSCILLATOR FREQUENCIES**

$C_{EXT}$	$R_{EXT}$	Average $F_{osc} @ 5 \text{ V}, 25^\circ\text{C}$	
20 pF	3.3K	5 MHz	$\pm 27\%$
	5K	3.8 MHz	$\pm 21\%$
	10K	2.2 MHz	$\pm 21\%$
	100K	262 kHz	$\pm 31\%$
100 pF	3.3K	1.6 MHz	$\pm 13\%$
	5K	1.2 MHz	$\pm 13\%$
	10K	684 kHz	$\pm 18\%$
	100K	71 kHz	$\pm 25\%$
300 pF	3.3K	660 kHz	$\pm 10\%$
	5.0K	484 kHz	$\pm 14\%$
	10K	267 kHz	$\pm 15\%$
	100K	29 kHz	$\pm 19\%$

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviations from the average value for  $V_{DD} = 5\text{V}$ .

FIGURE 14-15: WDT TIMER TIME-OUT PERIOD vs. VDD<sup>(1)</sup>

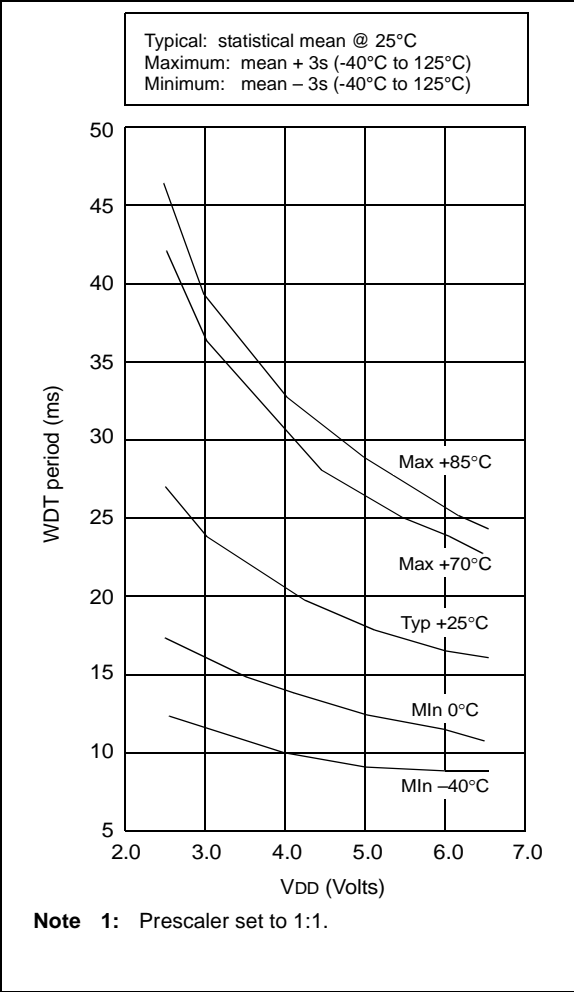
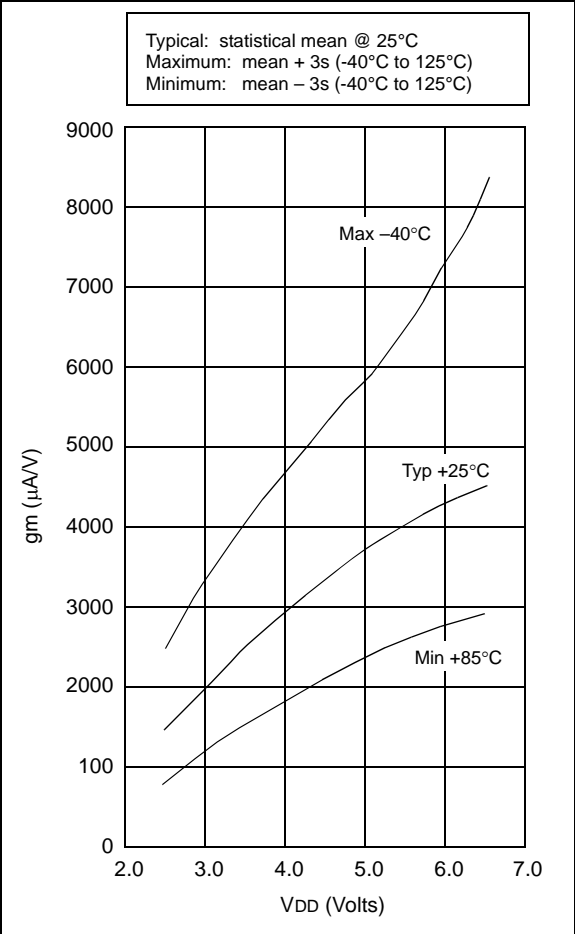


FIGURE 14-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



# PIC16C5X

## 15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

PIC16LC54A-04E (Extended)		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
PIC16C54A-04E, 10E, 20E (Extended)		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	<b>Supply Voltage</b>					
		PIC16LC54A	3.0 2.5	— —	6.25 6.25	V V	XT and RC modes LP mode
D001A		PIC16C54A	3.5 4.5	— —	5.5 5.5	V V	RC and XT modes HS mode
D002	VDR	<b>RAM Data Retention Voltage<sup>(1)</sup></b>	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	<b>VDD Start Voltage</b> to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	<b>VDD Rise Rate</b> to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	<b>Supply Current<sup>(2)</sup></b>					
		PIC16LC54A	—	0.5	25	mA	FOSC = 4.0 MHz, VDD = 5.5V, RC <sup>(3)</sup> and XT modes
			—	11	27	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial
			—	11	35	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial
			—	11	37	μA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Extended
D010A		PIC16C54A	—	1.8	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V, RC <sup>(3)</sup> and XT modes
			—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V, HS mode
			—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode

Legend: Rows with standard voltage device data only are shaded for improved readability.

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**Note 3:** Does not include current through REXT. The current through the resistor can be estimated by the formula:  $I_R = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.

## 15.4 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04E, 10E, 20E, PIC16LC54A-04E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial-PIC16LV54A-02I $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	VIL	<b>Input Low Voltage</b> I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VSS VSS VSS VSS VSS	— — — — —	0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	Pin at hi-impedance  RC mode only <sup>(3)</sup> XT, HS and LP modes
D040	VIH	<b>Input High Voltage</b> I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.2 VDD + 1 2.0 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD	— — — — — —	VDD VDD VDD VDD VDD VDD	V V V V V V	For all VDD <sup>(4)</sup> 4.0V < VDD ≤ 5.5V <sup>(4)</sup>  RC mode only <sup>(3)</sup> XT, HS and LP modes
D050	VHYS	<b>Hysteresis of Schmitt Trigger inputs</b>	0.15 VDD*	—	—	V	
D060	IIL	<b>Input Leakage Current<sup>(1,2)</sup></b> I/O ports  MCLR MCLR T0CKI OSC1	-1.0 -5.0 — -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0 —	μA μA μA μA μA	<b>For VDD ≤ 5.5V:</b> VSS ≤ VPIN ≤ VDD, pin at hi-impedance VPIN = VSS + 0.25V VPIN = VDD VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
D080	VOL	<b>Output Low Voltage</b> I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	IOH = 8.7 mA, VDD = 4.5V IOH = 1.6 mA, VDD = 4.5V, RC mode only
	VOH	<b>Output High Voltage<sup>(2)</sup></b> I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7	— —	— —	V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC mode only

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

# PIC16C5X

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NOTES:



# PIC16C5X

FIGURE 16-12: TYPICAL I<sub>DD</sub> vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)

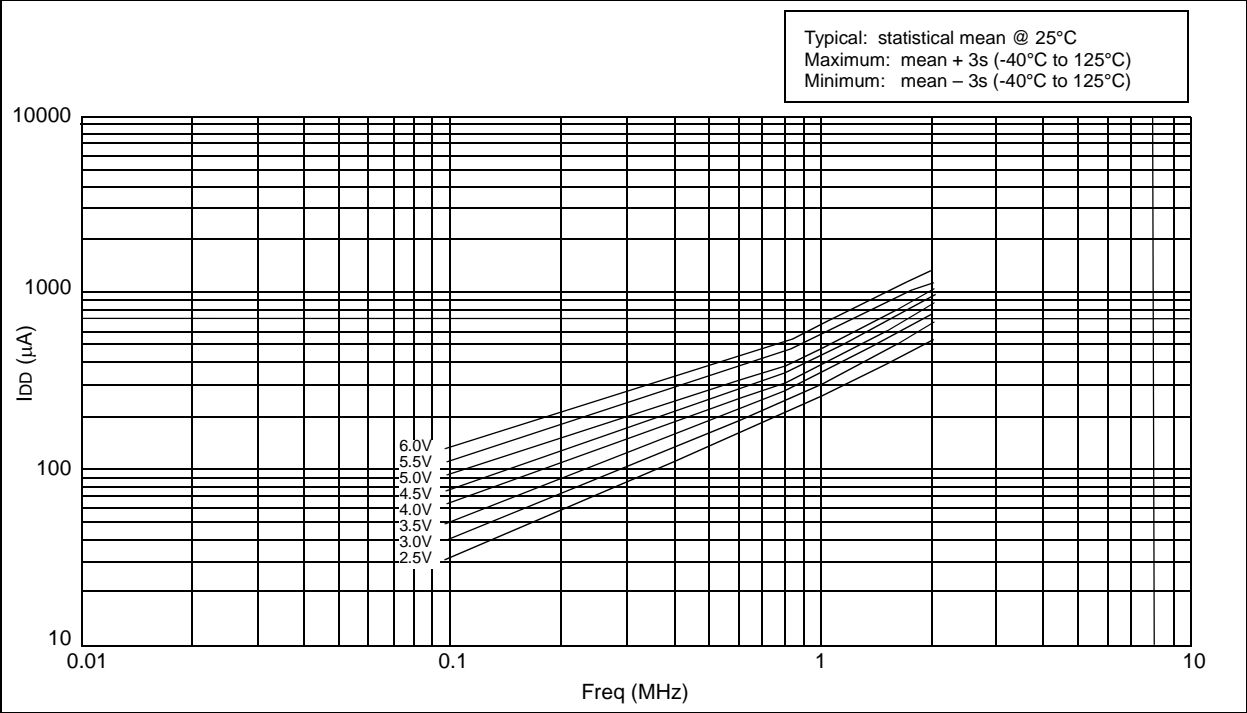
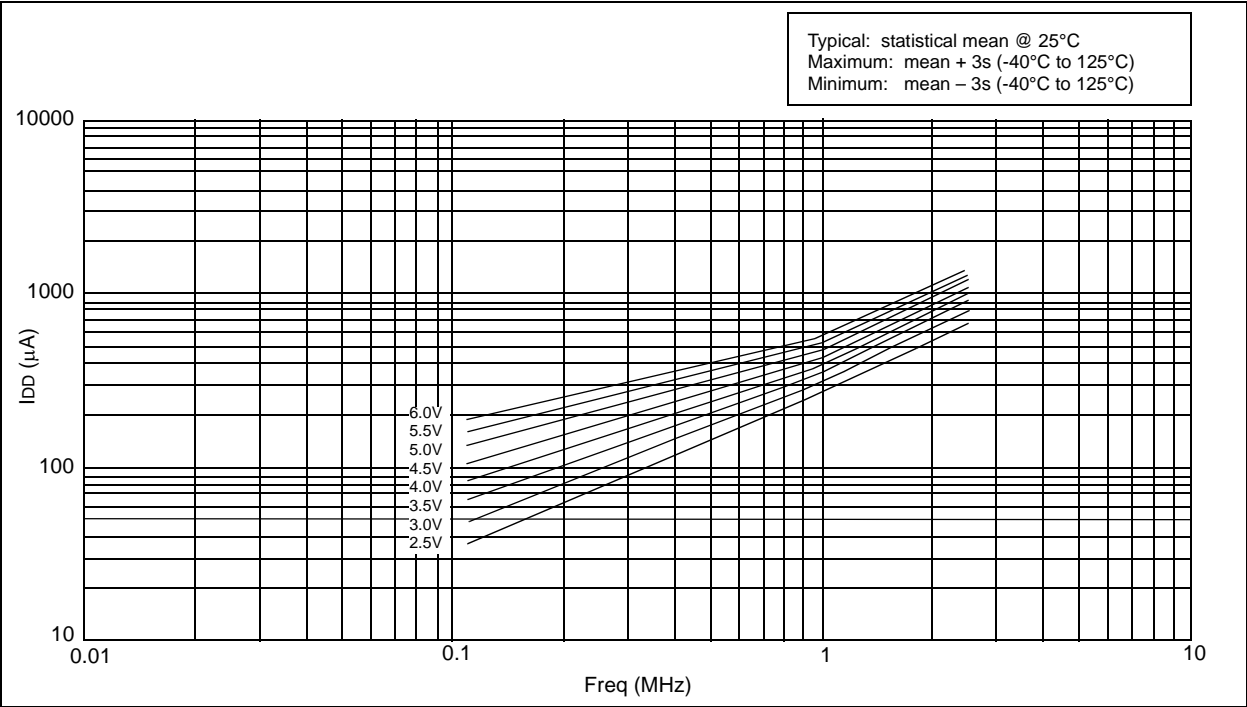


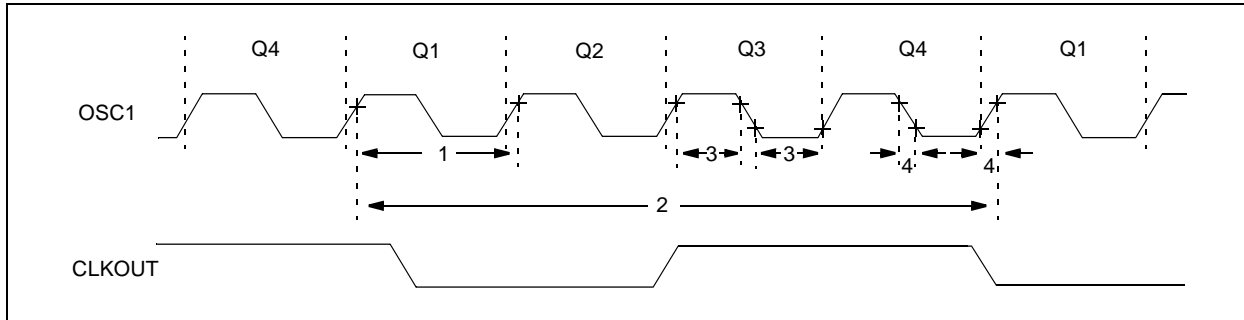
FIGURE 16-13: MAXIMUM I<sub>DD</sub> vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, -40°C to +85°C)



# PIC16C5X

## 17.5 Timing Diagrams and Specifications

**FIGURE 17-6: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X**



**TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

<b>Standard Operating Conditions (unless otherwise specified)</b> <b>AC Characteristics</b> Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency <sup>(1)</sup>	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency <sup>(1)</sup>	DC	—	4.0	MHz	RC osc mode
			0.45	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	20	MHz	HS osc mode (20)
1	TOSC	External CLKIN Period <sup>(1)</sup>	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period <sup>(1)</sup>	250	—	—	ns	RC osc mode
			250	—	2,200	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

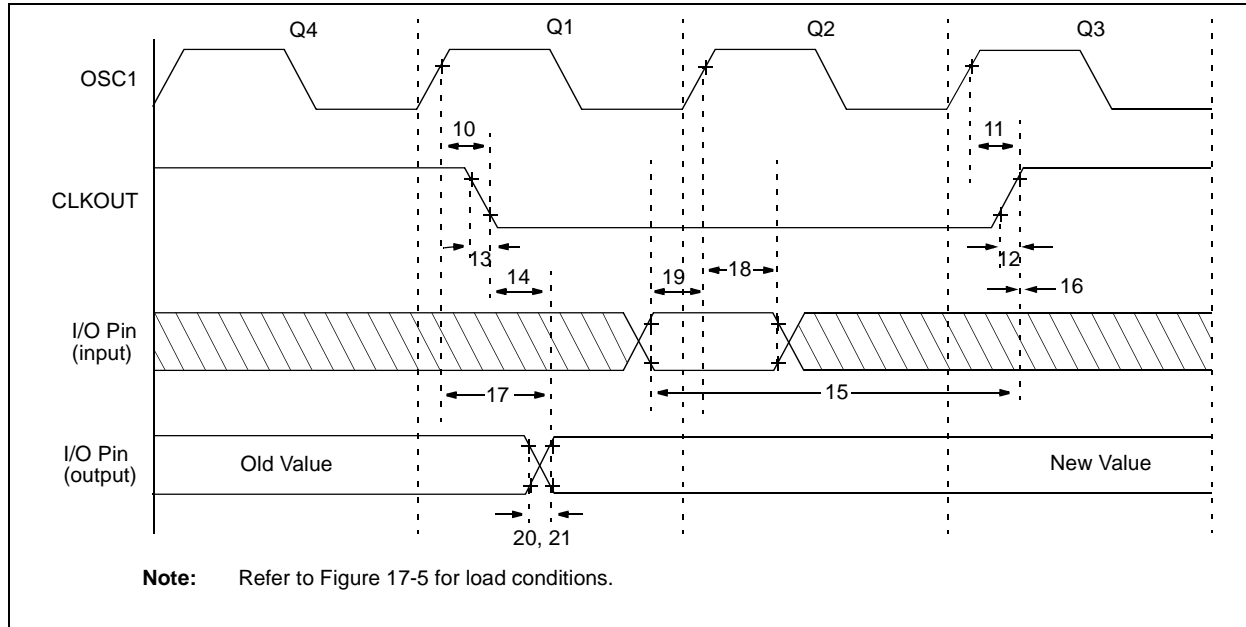
**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

# PIC16C5X

**FIGURE 17-7: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X**



**TABLE 17-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature				
		0°C ≤ TA ≤ +70°C for commercial				
		-40°C ≤ TA ≤ +85°C for industrial				
		-40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ <sup>(1)</sup>	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ <sup>(1)</sup>	—	15	30**	ns
12	TckR	CLKOUT rise time <sup>(1)</sup>	—	5.0	15**	ns
13	TckF	CLKOUT fall time <sup>(1)</sup>	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid <sup>(1)</sup>	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ <sup>(1)</sup>	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ <sup>(1)</sup>	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid <sup>(2)</sup>	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time <sup>(2)</sup>	—	10	25**	ns
21	TioF	Port output fall time <sup>(2)</sup>	—	10	25**	ns

\* These parameters are characterized but not tested.

\*\* These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Refer to Figure 17-5 for load conditions.

# PIC16C5X

## 19.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)<sup>(1)</sup>

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified)				
			Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D030	VIL	<b>Input Low Voltage</b> I/O Ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1	VSS VSS VSS VSS	— — — —	0.8 0.15 VDD 0.15 VDD 0.2 VDD	V V V V	4.5V < VDD ≤ 5.5V HS, 20 MHz ≤ FOSC ≤ 40 MHz
D040	VIH	<b>Input High Voltage</b> I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1	2.0 0.85 VDD 0.85 VDD 0.8 VDD	— — — —	VDD VDD VDD VDD	V V V V	4.5V < VDD ≤ 5.5V HS, 20 MHz ≤ FOSC ≤ 40 MHz
D050	VHYS	<b>Hysteresis of Schmitt Trigger inputs</b>	0.15 VDD*	—	—	V	
D060	IIL	<b>Input Leakage Current<sup>(2,3)</sup></b> I/O ports  MCLR MCLR T0CKI OSC1	-1.0 -5.0 — -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0 —	μA μA μA μA μA	<b>For VDD ≤ 5.5V:</b> VSS ≤ VPIN ≤ VDD, pin at hi-impedance VPIN = VSS + 0.25V VPIN = VDD VSS ≤ VPIN ≤ VDD VSS ≤ VPIN ≤ VDD, HS
D080	VOL	<b>Output Low Voltage</b> I/O ports	—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
D090	VOH	<b>Output High Voltage<sup>(3)</sup></b> I/O ports	VDD - 0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V

\* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected and HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 17.3.
- 2:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
- 3:** Negative current is defined as coming out of the pin.

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