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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.8V
Data Converters	·
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lv54a-02-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly. The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

	Pi	n Numb	er	Pin	Buffer	
Pin Name	DIP	SOIC	SSOP	Туре	Туре	Description
RA0	17	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RB0	6	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	
RB5	11	11	12	I/O	TTL	
RB6	12	12	13	I/O	TTL	
RB7	13	13	14	I/O	TTL	
TOCKI	3	3	3	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
MCLR/Vpp	4	4	4	I	ST	Master clear (RESET) input/programming voltage input. This pin is an active low RESET to the device. Voltage on the MCLR/VPP pin must not exceed VDD to avoid unin- tended entering of Programming mode.
OSC1/CLKIN	16	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	17	0		Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
Vdd	14	14	15,16	Р	_	Positive supply for logic and I/O pins.
Vss	5	5	5,6	Р	_	Ground reference for logic and I/O pins.

TABLE 3-1:PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58,
PIC16CR58

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- 1. LP: Low Power Crystal
- 2. XT: Crystal/Resonator
- 3. HS: High Speed Crystal/Resonator
- 4. RC: Resistor/Capacitor

Note: Not all oscillator selections available for all parts. See Section 9.1.

4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

FIGURE 4-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



FIGURE 4-2:

EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS -PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-33 pF	15-33 pF
	4.0 MHz	10-22 pF	10-22 pF
HS	8.0 MHz	10-22 pF	10-22 pF
	16.0 MHz	10 pF	10 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR -PIC16C5X. PIC16CR5X

Osc Type	Crystal Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Note 1: For VDD > 4.5V, C1 = C2 \approx 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

Note: If you change from this device to another device, please verify oscillator characteristics in your application.

5.0 RESET

PIC16C5X devices may be RESET in one of the following ways:

- Power-On Reset (POR)
- MCLR Reset (normal operation)
- MCLR Wake-up Reset (from SLEEP)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from SLEEP)

Table 5-1 shows these RESET conditions for the PCL and STATUS registers.

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-On Reset (POR), MCLR or WDT Reset. A MCLR or WDT wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS <4:3>) are set or cleared depending on the different RESET conditions (Table 5-1). These bits may be used to determine the nature of the RESET.

Table 5-3 lists a full description of RESET states of all registers. Figure 5-1 shows a simplified block diagram of the On-chip Reset circuit.

TABLE 5-1: STATUS BITS AND THEIR SIGNIFICANCE

Condition	то	PD
Power-On Reset	1	1
MCLR Reset (normal operation)	u	u
MCLR Wake-up (from SLEEP)	1	0
WDT Reset (normal operation)	0	1
WDT Wake-up (from SLEEP)	0	0

Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH RESET

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	<u>Value</u> on MCLR and WDT Reset
03h	STATUS	PA2	PA1	PA0	TO	PD	Z	DC	С	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, q = see Table 5-1 for possible values.

7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;

;				PORT	latch	PORT	pins
;							
	BCF	PORTB,	7	;01pp	pppp	11pp	pppp
	BCF	PORTB,	6	;10pp	pppp	11pp	pppp
	MOVLW	H'3F'		;			
	TRIS	PORTB		;10pp	pppp	10pp	pppp
;							

;Note that the user may have expected the pin ;values to be 00pp pppp. The 2nd BCF caused ;RB7 to be latched as the pin value (High).

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.



FIGURE 7-2: SUCCESSIVE I/O OPERATION

CALL	Subroutine Call				
Syntax:	[<i>label</i>] CALL k				
Operands:	$0 \leq k \leq 255$				
Operation:	(PC) + 1 \rightarrow TOS; k \rightarrow PC<7:0>; (STATUS<6:5>) \rightarrow PC<10:9>; 0 \rightarrow PC<8>				
Status Affected:	None				
Encoding:	1001 kkkk kkkk				
Description.	address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two- cycle instruction				
Words:	1				
Cycles:	2				
Example:	HERE CALL THERE				
Before Instruction PC = address (HERE) After Instruction PC = address (THERE) TOS = address (HERE + 1)					

CLRE	Clear f
	Cical I

Syntax:	[label]	CLRF f				
Operands:	$0 \leq f \leq 31$					
Operation:	$\begin{array}{l} 00h \rightarrow (f); \\ 1 \rightarrow Z \end{array}$					
Status Affected:	Z					
Encoding:	0000	011f	ffff			
Description:	The contents of register 'f' are cleared and the Z bit is set.					
Words:	1					
Cycles:	1					
Example:	CLRF	FLAG_RE	G			
Before Instru FLAG_RI After Instructi	ction EG = Ion	0x5A				
FLAG_R	EG =	0x00				
Z	=	1				

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W); \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Encoding:	0000 0100 0000
Description:	The W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Example:	CLRW
VV = After Instruct W = Z =	= 0x5A tion = 0x00 = 1
CLRWDT	Clear Watchdog Timer
CLRWDT Syntax:	Clear Watchdog Timer
CLRWDT Syntax: Operands:	Clear Watchdog Timer [<i>label</i>] CLRWDT None
CLRWDT Syntax: Operands: Operation:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow \overline{TO};$ $1 \rightarrow \overline{PD}$
CLRWDT Syntax: Operands: Operation: Status Affected:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow \overline{TO};$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding:	Clear Watchdog Timer[label]CLRWDTNone $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ \overline{TO}, PD 0000 0000
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description:	Clear Watchdog Timer[label] CLRWDTNone $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0100 The CLRWDT instruction resets theWDT. It also resets the prescaler, ifthe prescaler is assigned to theWDT and not Timer0. Status bitsTO and PD are set.
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	Clear Watchdog Timer [label] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1 1
CLRWDT Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example:	Clear Watchdog Timer [<i>label</i>] CLRWDT None $00h \rightarrow WDT;$ $0 \rightarrow WDT$ prescaler (if assigned); $1 \rightarrow TO;$ $1 \rightarrow PD$ TO, PD 0000 0000 0100 The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set. 1 1 CLRWDT

After Instruction		
WDT counter	=	0x00
WDT prescaler	=	0
TO	=	1
PD	=	1

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multiproject software development tool.

11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft[®] Windows environment were chosen to best make these features available to you, the end user.

11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.









15.6 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16C54A



TABLE 15-1:	EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Chara	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic Min Typ† Max Units Condition						
	Fosc	External CLKIN Fre-	DC		4.0	MHz	XT OSC mode	
		quency	DC	—	2.0	MHz	XT osc mode (PIC16LV54A)	
			DC	—	4.0	MHz	HS osc mode (04)	
			DC	—	10	MHz	HS osc mode (10)	
			DC	—	20	MHz	HS osc mode (20)	
			DC	—	200	kHz	LP osc mode	
		Oscillator Frequency ⁽¹⁾	DC	_	4.0	MHz	RC osc mode	
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)	
			0.1	—	4.0	MHz	XT osc mode	
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)	
			4.0	—	4.0	MHz	HS osc mode (04)	
			4.0	—	10	MHz	HS osc mode (10)	
			4.0	—	20	MHz	HS osc mode (20)	
			5.0		200	kHz	LP osc mode	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
 - Instruction cycle period (TcY) equals four times the input oscillator time base period.



TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A

AC Chara	cteristics							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units		
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾		15	30**	ns		
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾		15	30**	ns		
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns		
13	TckF	CLKOUT fall time ⁽¹⁾		5.0	15**	ns		
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾		—	40**	ns		
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	_	_	ns		
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	—	_	ns		
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	_	100*	ns		
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD		_	ns		
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	_	ns		
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns		
21	TioF	Port output fall time ⁽²⁾		10	25**	ns		

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 15-1 for load conditions.

PIC16C5X



FIGURE 16-9: VIH, VIL OF MCLR, TOCKI AND OSC1 (IN RC MODE) vs. VDD



FIGURE 18-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, 25°C)







TABLE 18-2:INPUT CAPACITANCE

Bin	Typical Capacitance (pF)					
FIII	18L PDIP	18L SOIC				
RA port	5.0	4.3				
RB port	5.0	4.3				
MCLR	17.0	17.0				
OSC1	4.0	3.5				
OSC2/CLKOUT	4.3	3.5				
TOCKI	3.2	2.8				

All capacitance values are typical at 25° C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

19.0 ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

Absolute Maximum Ratings^(†)

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	
Max. current into Vod pin	
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, IIK (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Iок (Vo < 0 or Vo > Voo)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O (Port A, B or C)	
Max. output current sunk by a single I/O (Port A, B or C)	
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VI	ор-Voh) x Ioh} + Σ (Vol x Iol)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

19.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)⁽¹⁾

PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)			$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
D001	Vdd	Supply Voltage	4.5		5.5	V	HS mode from 20 - 40 MHz		
D002	Vdr	RAM Data Retention Voltage ⁽²⁾	—	1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	-	V	See Section 5.1 for details on Power-on Reset		
D004	SVDD	VDD Rise Rate to ensure Power- on Reset	0.05*	_		V/ms	See Section 5.1 for details on Power-on Reset		
D010	IDD	Supply Current ⁽³⁾	-	5.2 6.8	12.3 16	mA mA	FOSC = 40 MHz, VDD = 4.5V, HS mode FOSC = 40 MHz, VDD = 5.5V, HS mode		
D020	IPD	Power-down Current ⁽³⁾		1.8 9.8	7.0 27*	μΑ μΑ	VDD = 5.5V, WDT disabled, Commercial VDD = 5.5V, WDT enabled, Commercial		

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- **Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected, HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 19.1.
 - **2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - **3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

FIGURE 19-6: TIMER0 CLOCK TIMINGS - PIC16C5X-40



TABLE 19-4: TIMER0 CLOCK REQUIREMENTS PIC16C5X-40

AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	_	_	ns	
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N		_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

20.0 DEVICE CHARACTERIZATION - PIC16LC54C 40MHz

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.





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28-Lead Ceramic Dual In-line with Window (JW) - 600 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.195	.210	.225	4.95	5.33	5.72
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.038	.060	0.38	0.95	1.52
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	В	.016	.020	.023	0.41	0.51	0.58
Overall Row Spacing §	eB	.610	.660	.710	15.49	16.76	18.03
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37

Sontolling Parameter
 Significant Characteristic
 JEDEC Equivalent: MO-103
 Drawing No. C04-013

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