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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.8V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lv54a-02i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly. The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).

Din Nome	Pin Number			Pin	Buffer	Deceristics
Pin Name	DIP	SOIC	SSOP	Туре	Туре	Description
RA0	6	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	7	6	I/O	TTL	
RA2	8	8	7	I/O	TTL	
RA3	9	9	8	I/O	TTL	
RB0	10	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	11	10	I/O	TTL	
RB2	12	12	11	I/O	TTL	
RB3	13	13	12	I/O	TTL	
RB4	14	14	13	I/O	TTL	
RB5	15	15	15	I/O	TTL	
RB6	16	16	16	I/O	TTL	
RB7	17	17	17	I/O	TTL	
RC0	18	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	19	I/O	TTL	
RC2	20	20	20	I/O	TTL	
RC3	21	21	21	I/O	TTL	
RC4	22	22	22	I/O	TTL	
RC5	23	23	23	I/O	TTL	
RC6	24	24	24	I/O	TTL	
RC7	25	25	25	I/O	TTL	
TOCKI	1	1	2	Ι	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
MCLR	28	28	28	Ι	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
OSC1/CLKIN	27	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	26	0	—	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
Vdd	2	2	3,4	Р	—	Positive supply for logic and I/O pins.
Vss	4	4	1,14	Р		Ground reference for logic and I/O pins.
N/C	3,5	3,5	—	_		Unused, do not connect.

TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of realtime applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

PIC16C5X

COMF	Complement f								
Syntax:	[<i>label</i>] COMF f,d								
Operands:	$0 \le f \le 31$ $d \in [0,1]$								
Operation:	$(\overline{f}) \rightarrow (dest)$								
Status Affected:	Z								
Encoding:	0010 01df ffff								
Description:	The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example:	COMF REG1,0								
Before Instru	ction								
REG1	= 0x13								
After Instruct	ion								
REG1	= 0x13								
W	= 0xEC								

DECF	Decrement f								
Syntax:	[label] DECF f,d								
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$								
Operation:	(f) – 1	\rightarrow (dest)							
Status Affected:	Z								
Encoding:	0000 11df ffff								
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example:	DECF	CNT,	1						
Before Instruc CNT Z After Instructi CNT Z	ction = = on = =	0x01 0 0x00 1							

DECFSZ	Decrement f, Skip if 0							
Syntax:	[label] DECFSZ f,d							
Operands:	$\begin{array}{l} 0\leq f\leq 31\\ d\in [0,1] \end{array}$							
Operation:	(f) $-1 \rightarrow d$; skip if result = 0							
Status Affected:	None							
Encoding:	0010 11df ffff							
Description:	remented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruc- tion, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle							
Words:	1							
Cycles:	1(2)							
Example:	HERE DECFSZ CNT, 1 GOTO LOOP							
	CONTINUE • •							
Before Instru	uction							
PC	= address (HERE)							
After Instruc	tion							
CNT	= CNI - 1;							
IT CN I	= U,							
	= address (CONTINUE);							
	\neq U, - address (UFDF, 1)							
FU	= addless (HERE+1)							

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multiproject software development tool.

11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft[®] Windows environment were chosen to best make these features available to you, the end user.

11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present. NOTES:

12.4 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

DC CHARACTERISTICS			$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array} $					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions	
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 (Schmitt Trigger)	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	Pin at hi-impedance PIC16C5X-RC only ⁽³⁾ PIC16C5X-XT, 10, HS, LP	
D040 D050	VIH	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 (Schmitt Trigger) Hysteresis of Schmitt	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD 0.15 VDD*		VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all $VDD^{(4)}$ 4.0V < $VDD \le 5.5V^{(4)}$ VDD > 5.5V PIC16C5X-RC only ⁽³⁾ PIC16C5X-XT, 10, HS, LP	
D060	lı.	Trigger inputs Input Leakage Current ^(1,2) I/O ports MCLR MCLR TOCKI OSC1	-1 -5 -3 -3	0.5 — 0.5 0.5 0.5	+1 +5 +3 +3	μΑ μΑ μΑ μΑ	$\label{eq:ForVDD} \begin{split} & \leq \textbf{5.5V:} \\ & VSS \leq VPIN \leq VDD, \\ & pin \text{ at hi-impedance} \\ & VPIN = VSS + 0.25V \\ & VPIN = VDD \\ & VSS \leq VPIN \leq VDD \\ & VSS \leq VPIN \leq VDD, \\ & PIC16C5X-XT, \ 10, \ HS, \ LP \end{split}$	
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT			0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC	
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd - 0.7 Vdd - 0.7		_	V V	ІОН = –5.4 mA, VDD = 4.5V ІОН = –1.0 mA, VDD = 4.5V, PIC16C5X-RC	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- **Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - 2: Negative current is defined as coming out of the pin.
 - **3:** For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
 - 4: The user may use the better of the two specifications.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 PIC16LCR54A-04I (Commercial, Industrial)				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			Standa Operat	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LCR54A	2.0		6.25	V			
D001 D001A		PIC16CR54A	2.5 4.5		6.25 5.5	V V	RC and XT modes HS mode		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5*	_	V	Device in SLEEP mode		
D003	Vpor	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	Svdd	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current ⁽²⁾							
D005		PICLCR54A	—	10	20 70	μA μA	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V		
D005A		PIC16CR54A		2.0 0.8 90 4.8	3.6 1.8 350 10	mA mA μA	RC ⁽³⁾ and XT modes: Fosc = 4.0 MHz, VDD = 6.0V Fosc = 4.0 MHz, VDD = 3.0V Fosc = 200 kHz, VDD = 2.5V HS mode: Fosc = 10 MHz, VDD = 5.5V		
			—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5 V		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

PIC16CR54A-04E, 10E, 20E (Extended)			Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended				
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
D001	Vdd	Supply Voltage RC, XT and LP modes HS mode	3.25 4.5		6.0 5.5	V V	
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power- on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ RC ⁽³⁾ and XT modes HS mode HS mode		1.8 4.8 9.0	3.3 10 20	mA mA mA	Fosc = 4.0 MHz, VDD = 5.5V Fosc = 10 MHz, VDD = 5.5V Fosc = 16 MHz, VDD = 5.5V
D020	IPD	Power-down Current ⁽²⁾		5.0 0.8	22 18	μΑ μΑ	VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC CH	ARACTE	RISTICS	Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions	
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes	
D040	Vih	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all VDD ⁽⁴⁾ 4.0V < VDD ≤ 5.5V ⁽⁴⁾ VDD > 5.5V RC mode only ⁽³⁾ XT, HS and LP modes	
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	—	V		
D060	lı∟	Input Leakage Current ^(1,2) I/O ports MCLR MCLR T0CKI OSC1	-1.0 -5.0 -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 	μΑ μΑ μΑ μΑ	$\label{eq:For VDD} \begin{split} & \leq \textbf{5.5V:} \\ & \forall SS \leq \forall PIN \leq \forall DD, \\ & pin \text{ at hi-impedance} \\ & \forall PIN = \forall SS + 0.25 \forall \\ & \forall PIN = \forall DD \\ & \forall SS \leq \forall \forall PIN \leq \forall DD \\ & \forall SS \leq \forall \forall PIN \leq \forall DD, \\ & \forall XT, \ HS \text{ and } \ LP \ modes \end{split}$	
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC mode only	
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7			V V	IOH = -5.4 mA, VDD = 4.5 V IOH = -1.0 mA, VDD = 4.5 V, RC mode only	

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.



TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units
10	TosH2ckL	OSC1 [↑] to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	_	40**	ns
15	TioV2ckH	Port in valid before CLKOUT ⁽¹⁾	0.25 TCY+30*	_	-	ns
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	_	-	ns
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	_	100*	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD		—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD		_	ns
20	TioR	Port output rise time ⁽²⁾		10	25**	ns
21	TioF	Port output fall time ⁽²⁾	_	10	25**	ns

* These parameters are characterized but not tested.

- ** These parameters are design targets and are not tested. No characterization data available at this time.
- † Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 13.1 for load conditions.

15.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings ^(†)	
Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	150 mA
Max. current into VDD pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O port (PORTA or B)	
Max. output current sunk by a single I/O port (PORTA or B)	50 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH	$+ \sum \{(VDD-VOH) \times IOH\} + \sum (VOL \times IOL)$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC Characteristics		$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions		
1	Tosc	External CLKIN Period ⁽¹⁾	250	_		ns	XT OSC mode		
			500	—		ns	XT osc mode (PIC16LV54A)		
			250	—		ns	HS osc mode (04)		
			100	—		ns	HS osc mode (10)		
			50	—		ns	HS osc mode (20)		
			5.0	_		μS	LP OSC mode		
		Oscillator Period ⁽¹⁾	250			ns	RC OSC mode		
			500	—		ns	RC osc mode (PIC16LV54A)		
			250	—	10,000	ns	XT OSC mode		
			500	—		ns	XT osc mode (PIC16LV54A)		
			250	—	250	ns	HS osc mode (04)		
			100	—	250	ns	HS osc mode (10)		
			50	—	250	ns	HS osc mode (20)		
			5.0	_	200	μS	LP OSC mode		
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc					
3	TosL, TosH	Clock in (OSC1) Low or	85*	—	—	ns	XT oscillator		
		High Lime	20*	—	—	ns	HS oscillator		
			2.0*		—	μS	LP oscillator		
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator		
			—	—	25*	ns	HS oscillator		
			_	—	50*	ns	LP oscillator		

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.



TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A

AC Chara	cteristics								
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units			
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾		15	30**	ns			
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾		15	30**	ns			
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns			
13	TckF	CLKOUT fall time ⁽¹⁾		5.0	15**	ns			
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾		—	40**	ns			
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	0.25 TCY+30*	_	_	ns			
16	TckH2iol	Port in hold after CLKOUT ⁽¹⁾	0*	—	_	ns			
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽²⁾	—	_	100*	ns			
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD		_	ns			
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	_	ns			
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns			
21	TioF	Port output fall time ⁽²⁾		10	25**	ns			

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 15-1 for load conditions.

17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial) PIC16C5X PIC16CR5X (Commercial, Industrial)								
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units Conditions			Conditions		
	Vdd	Supply Voltage						
D001		PIC16LC5X	2.5 2.7 2.5		5.5 5.5 5.5	V V V	$\begin{array}{l} -40^{\circ}C \leq TA \leq +\ 85^{\circ}C,\ 16LCR5X \\ -40^{\circ}C \leq TA \leq 0^{\circ}C,\ 16LC5X \\ 0^{\circ}C \leq TA \leq +\ 85^{\circ}C \ 16LC5X \end{array}$	
D001A		PIC16C5X	3.0 4.5		5.5 5.5	V V	RC, XT, LP and HS mode from 0 - 10 MHz from 10 - 20 MHz	
D002	Vdr	RAM Data Retention Volt- age ⁽¹⁾	-	1.5*	-	V	Device in SLEEP mode	
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	_	V/ms	See Section 5.1 for details on Power-on Reset	

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.
- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X PIC16LCR5X (Commercial, Industrial)				$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array} $					
PIC16C5X PIC16CR5X (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
	IPD	Power-down Current ⁽²⁾							
D020		PIC16LC5X	—	0.25	2	μΑ	VDD = 2.5V, WDT disabled, Commercial		
			—	0.25	3	μA	VDD = 2.5V, WDT disabled, Industrial		
			_	1 1 25	5	μΑ	VDD = $2.5V$, WDT enabled, Commercial VDD = $2.5V$ WDT enabled Industrial		
		PIC16C5X		0.25	4.0	μΑ	$V_{DD} = 3.0V$ WDT disabled Commercial		
DOZON			_	0.25	5.0	μ/(μΑ	$V_{DD} = 3.0V$, WDT disabled, Industrial		
			—	1.8	7.0*	μA	VDD = 5.5V, WDT disabled, Commercial		
			—	2.0	8.0*	μA	VDD = 5.5V, WDT disabled, Industrial		
			—	4	12*	μA	VDD = 3.0V, WDT enabled, Commercial		
			—	4	14*	μA	VDD = 3.0V, WDT enabled, Industrial		
			—	9.8	27*	μA	VDD = 5.5V, WDT enabled, Commercial		
			-	12	30*	μA	VDD = 5.5V, WDT enabled, Industrial		

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

- 1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to proper value for processor used.
- 6. Remove any use of the ADDLW, RETURN and SUBLW instructions.
- 7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

w

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NOTES:

ON-LINE SUPPORT

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