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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.8V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lv54a-02i-ss

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Pin Diagrams



Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	—	No
PIC16C54C	2.5-5.5	User	See Note 1	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	_	No
PIC16C55A	2.5-5.5	User	See Note 1	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C56A	2.5-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	—	No
PIC16C57C	2.5-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

NOTES:

NOTES:

TABLE 5-3: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	MCLR or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	11 1111	11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	XXXX XXXX	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000q quuu
FSR ⁽¹⁾	04h	1xxx xxxx	luuu uuuu
PORTA	05h	xxxx	uuuu
PORTB	06h	XXXX XXXX	uuuu uuuu
PORTC ⁽²⁾	07h	XXXX XXXX	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	սսսս սսսս

Legend: x = unknown u = unchanged - = unimplemented, read as '0'<math>q = see tables in Table 5-1 for possible values.

- Note 1: These values are valid for PIC16C57/CR57/CR58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.
 - **2:** General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is <u>RESET</u>. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the <u>Embedded Control Handbook</u>.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2:

EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 k Ω will limit any current flowing into \overline{MCLR} from external capacitor C in the event of \overline{MCLR} pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB, W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16CR56, PIC16CR56, PIC16CS8 and PIC16CR58.

7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the
	output data latches. That is, if an output
	driver on a pin is enabled and driven high,
	but the external system is holding it low, a
	read of the port will indicate that the pin is
	low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 7-1:	SUMMARY O	F PORT	REGISTERS
			LOIOI LIVO

Value on Value on Bit 4 Bit 3 Bit 1 Bit 0 MCLR and Address Name Bit 7 Bit 6 Bit 5 Bit 2 Power-On Reset WDT Reset TRIS N/A I/O Control Registers (TRISA, TRISB, TRISC) 1111 1111 1111 1111 05h PORTA RA3 RA2 RA1 RA0 _ _ _ _ xxxx _ _ _ _ uuuu PORTB 06h RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 XXXX XXXX uuuu uuuu 07h PORTC RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 XXXX XXXX uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



8.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

8.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 8-1: CHANGING PRESCALER (TIMER0→WDT)

CLRWDT	;Clear WDT
CLRF TMR0	;Clear TMR0 & Prescaler
MOVLW B'00xx1111'	;Last 3 instructions in
	this example
OPTION	;are required only if
	;desired
CLRWDT	;PS<2:0> are 000 or
	;001
MOVLW B'00xx1xxx'	;Set Prescaler to
OPTION	;desired WDT rate

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 8-2: CHANGING PRESCALER (WDT \rightarrow TIMER0)

CLRWDT		;Clear WDT and
		;prescaler
MOVLW	B'xxxx0xxx'	;Select TMR0, new
		;prescale value and
		;clock source

OPTION

9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.



TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	<u>Value</u> on MCLR and WDT Reset
N/A	OPTION	—	—	Tosc	Tose	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

13.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

Absolute Maximum Ratings(†)

Ambient Temperature under bias	55°C to +125°C
Storage Temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss ⁽¹⁾	0 to +14V
Voltage on all other pins with respect to Vss	0.6V to (VDD + 0.6V)
Total power dissipation ⁽²⁾	
Max. current out of Vss pin	150 mA
Max. current into Vod pin	50 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iık (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (V0 < 0 or V0 > VDD)	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port (PORTA or B)	40 mA
Max. output current sunk by a single I/O port (PORTA or B)	50 mA

- **Note 1:** Voltage spikes below Vss at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a low level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to Vss.
 - **2:** Power Dissipation is calculated as follows: PDIS = VDD x {IDD \sum IOH} + \sum {(VDD-VOH) x IOH} + \sum (VOL x IOL)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LC PIC16LC (Comm	R54A-04 R54A-04I ercial, Indus	trial)	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$						
PIC16CR54A-04, 10, 20 PIC16CR54A-04I, 10I, 20I (Commercial, Industrial)			Standa Operat	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions		
	Vdd	Supply Voltage							
D001		PIC16LCR54A	2.0		6.25	V			
D001 D001A		PIC16CR54A	2.5 4.5		6.25 5.5	V V	RC and XT modes HS mode		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5*	_	V	Device in SLEEP mode		
D003	Vpor	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset		
D004	Svdd	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset		
	IDD	Supply Current ⁽²⁾							
D005		PICLCR54A	—	10	20 70	μA μA	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V		
D005A		PIC16CR54A		2.0 0.8 90 4.8	3.6 1.8 350 10	mA mA μA	RC ⁽³⁾ and XT modes: Fosc = 4.0 MHz, VDD = 6.0V Fosc = 4.0 MHz, VDD = 3.0V Fosc = 200 kHz, VDD = 2.5V HS mode: Fosc = 10 MHz, VDD = 5.5V		
			—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5 V		

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

AC Characteristics								
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
1	Tosc	External CLKIN Period ⁽¹⁾	250		—	ns	XT OSC mode	
			250	—		ns	HS OSC mode (04)	
			100	—		ns	HS osc mode (10)	
			50	—	—	ns	HS osc mode (20)	
			5.0	_	—	μs	LP OSC mode	
		Oscillator Period ⁽¹⁾	250	—		ns	RC OSC mode	
			250	—	10,000	ns	XT OSC mode	
			250	—	250	ns	HS OSC mode (04)	
			100	—	250	ns	HS osc mode (10)	
			50	—	250	ns	HS OSC mode (20)	
			5.0		200	μS	LP OSC mode	
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc	—	—		
3	TosL, TosH	Clock in (OSC1) Low or High	50*	—	—	ns	XT oscillator	
		lime	20*	—	—	ns	HS oscillator	
			2.0*		—	μS	LP oscillator	
4	TosR, TosF	Clock in (OSC1) Rise or Fall	—	—	25*	ns	XT oscillator	
		lime	—	—	25*	ns	HS oscillator	
			—	—	50*	ns	LP oscillator	

TABLE 13-1:	EXTERNAL CLOCK TIMING REQUIREMENT	S - PIC16CR54A

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

when an external clock input is used, the "max" cycle time limit is "Du" (no clock) for all device

2: Instruction cycle period (TcY) equals four times the input oscillator time base period.

PIC16C5X

FIGURE 14-2: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 20 PF Typical: statistical mean @ 25°C Maximum: mean + 3s (-40°C to 125°C) Minimum: mean – 3s (-40°C to 125°C) 5.5 R = 3.3K5.0 4.5 R = 5K 4.0 3.5 Fosc (MHz) 3.0 R = 10K 2.5 2.0 Measured on DIP Packages, $T = 25^{\circ}C$ 1.5 1.0 R = 100K 0.5 0.0 3.0 3.5 4.0 4.5 5.0 5.5 6.0 VDD (Volts)

FIGURE 14-3:

TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 100 PF





FIGURE 14-22: PORTA, B AND C IOL vs. VoL, VDD = 5 V





FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD





TABLE 16-2:INPUT CAPACITANCE FOR
PIC16C54A/C58A

Pin	Typical Capacitance (pF)			
FIII	18L PDIP	18L SOIC		
RA port	5.0	4.3		
RB port	5.0	4.3		
MCLR	17.0	17.0		
OSC1	4.0	3.5		
OSC2/CLKOUT	4.3	3.5		
TOCKI	3.2	2.8		

All capacitance values are typical at 25°C. A part-to-part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

FIGURE 16-23: PORTA, B AND C IOL vs. VOL, VDD = 5V



17.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
D001	Vdd	Supply Voltage	3.0 4.5		5.5 5.5	V V	RC, XT, LP, and HS mode from 0 - 10 MHz from 10 - 20 MHz	
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode	
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset	
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	_	—	V/ms	See Section 5.1 for details on Power-on Reset	
D010	IDD	Supply Current ⁽²⁾ XT and RC ⁽³⁾ modes HS mode	_	1.8 9.0	3.3 20	mA mA	Fosc = 4.0 MHz, Vdd = 5.5V Fosc = 20 MHz, Vdd = 5.5V	
D020	IPD	Power-down Current ⁽²⁾		0.3 10 12 4.8 18 26	17 50* 60* 31* 68* 90*	μΑ μΑ μΑ μΑ μΑ	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled VDD = 3.0V, WDT enabled VDD = 4.5V, WDT enabled VDD = 5.5V, WDT enabled	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

- Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
 - **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40

TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40

AC Charac	teristics	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial)Operating Voltage VDD range is described in Section 19.1.							
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions		
30	TmcL	MCLR Pulse Width (low)	1000*		_	ns	VDD = 5.0V		
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)		
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)		
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns			

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

21.0 PACKAGING INFORMATION

21.1 Package Marketing Information

18-Lead PDIP



28-Lead Skinny PDIP (.300")



28-Lead PDIP (.600")



18-Lead SOIC



28-Lead SOIC



20-Lead SSOP



28-Lead SSOP





Example



Example



Example



Example



Example



Example



28-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging







	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.050			1.27	
Overall Height	А	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	Е	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	¢	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.013	0.23	0.28	0.33
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-052

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