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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	2MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.8V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lv54at-02i-so

5.1   Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the $\overline{MCLR}$/Vpp pin to Vdd. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where $\overline{MCLR}$ is not tied to Vdd is shown in Figure 5-3. Vdd is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset TDRT msec after $\overline{MCLR}$ goes high.
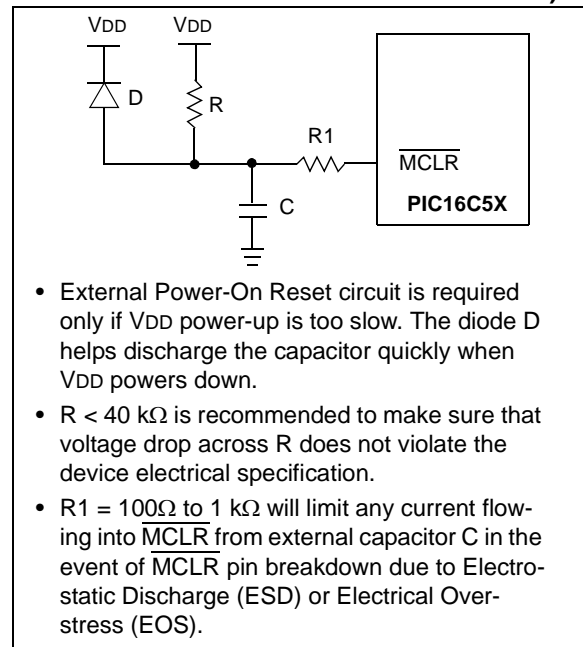
In Figure 5-4, the on-chip Power-On Reset feature is being used ($\overline{MCLR}$ and Vdd are tied together). The Vdd is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where Vdd rises too slowly. The time between when the DRT senses a high on the $\overline{MCLR}$/Vpp pin, and when the $\overline{MCLR}$/Vpp pin (and Vdd) actually reach their full value, is too long. In this situation, when the start-up timer times out, Vdd has not reached the Vdd (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

> **Note:**   When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal RESET when Vdd declines.

FIGURE 5-2:   EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

- External Power-On Reset circuit is required only if Vdd power-up is too slow. The diode D helps discharge the capacitor quickly when Vdd powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

PIC16C5X

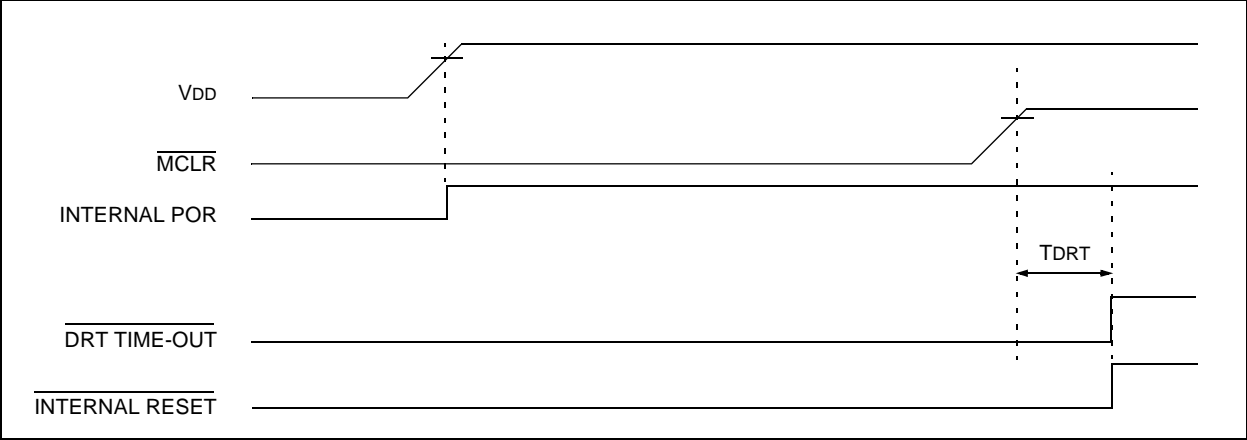**FIGURE 5-3:** TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO VDD)

FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD): FAST VDD RISE TIME
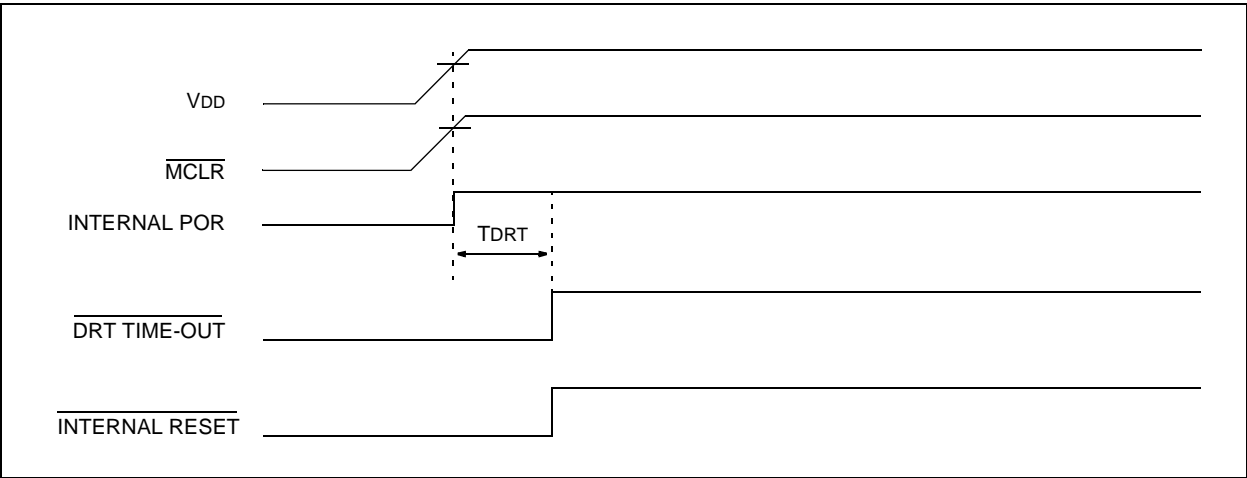
FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD): SLOW VDD RISE TIME

When VDD rises slowly, the TDRT time-out expires long before VDD has reached its final value. In this example, the chip will RESET properly if, and only if, $V1 \geq VDD$ min
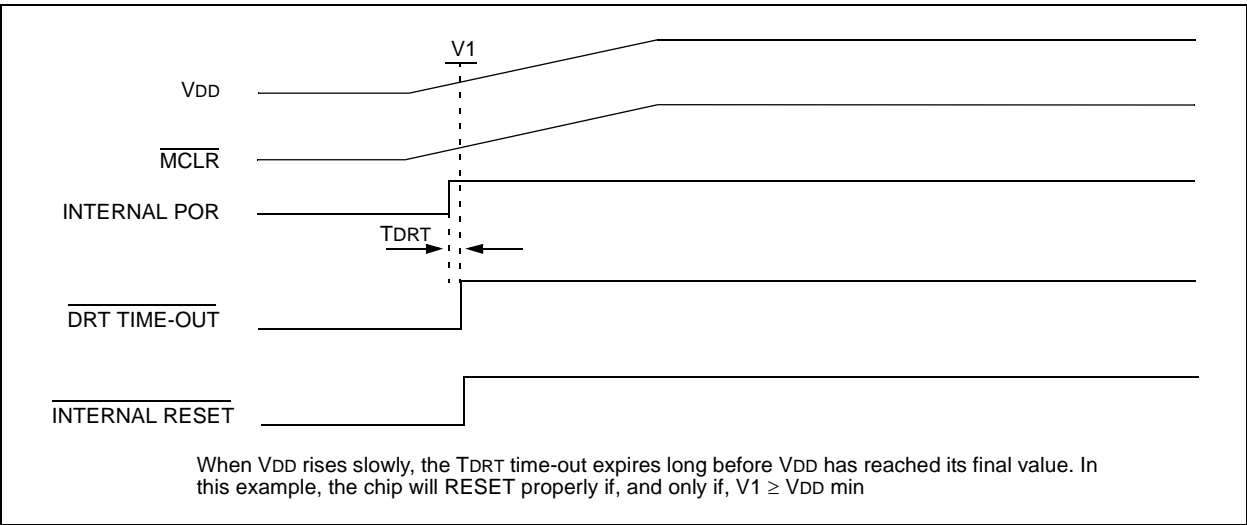
PIC16C5X

6.4 OPTION Register

The OPTION Register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W Register will be transferred to the OPTION Register. A RESET sets the OPTION<5:0> bits.

REGISTER 6-2: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	T0CS	TOSE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7-6: **Unimplemented**: Read as '0'

bit 5: **T0CS**: Timer0 clock source select bit

1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 source edge select bit

1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler assignment bit

1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared x = bit is unknown

6.7 Indirect Data Addressing; INDF and FSR Registers

The INDF Register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 6-1: INDIRECT ADDRESSING

- Register file 08 contains the value 10h
- Register file 09 contains the value 0Ah
- Load the value 08 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (FSR = 09h)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF Register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 6-2.

EXAMPLE 6-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        MOVLW   H'10'   ;initialize pointer
        MOVWF   FSR     ; to RAM
NEXT    CLRF    INDF    ;clear INDF Register
        INCF    FSR,F   ;inc pointer
        BTFSC   FSR,4   ;all done?
        GOTO    NEXT    ;NO, clear next
CONTINUE
        :               ;YES, continue
```

The FSR is either a 5-bit (PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56) or 7-bit (PIC16C57, PIC16CR57, PIC16C58, PIC16CR58) wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56: These do not use banking. FSR<6:5> bits are unimplemented and read as '1's.

PIC16C57, PIC16CR57, PIC16C58, PIC16CR58: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).

FIGURE 6-10: DIRECT/INDIRECT ADDRESSING

Note 1: For register map detail see Section 6.2.

NOTES:

Preliminary
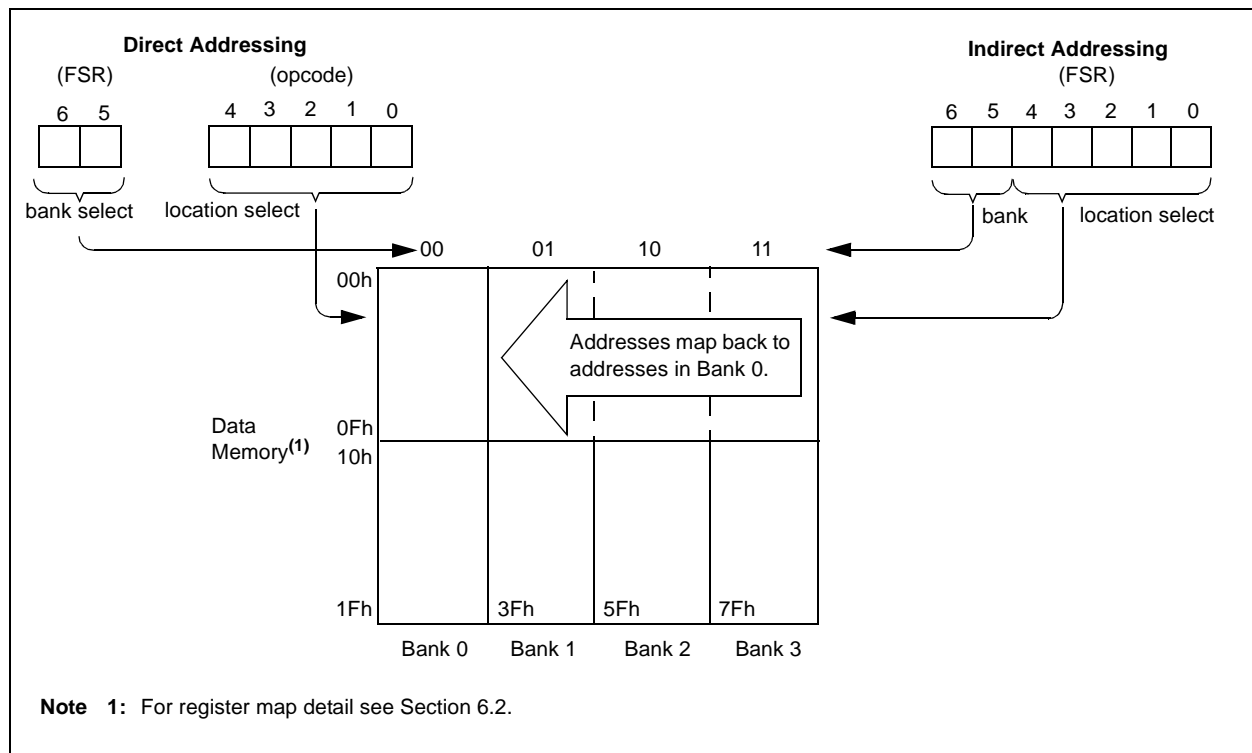
9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

12.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature −40°C ≤ TA ≤ +85°C for industrial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D001	VDD	**Supply Voltage** PIC16C5X-RCI PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-LPI	3.0 3.0 4.5 4.5 2.5	— — — — —	6.25 6.25 5.5 5.5 6.25	V V V V V	
D002	VDR	**RAM Data Retention Voltage**[1]	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current**[2] PIC16C5X-RCI[3] PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-HSI PIC16C5X-LPI	— — — — — —	1.8 1.8 4.8 4.8 9.0 15	3.3 3.3 10 10 20 40	mA mA mA mA mA μA	FOSC = 4 MHz, VDD = 5.5V FOSC = 4 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	IPD	**Power-down Current**[2]	— —	4.0 0.6	14 12	μA μA	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled

*   These parameters are characterized but not tested.

†   Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

    2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

      a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

      b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

    3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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13.6 Timing Diagrams and Specifications

FIGURE 13-2:   EXTERNAL CLOCK TIMING - PIC16CR54A
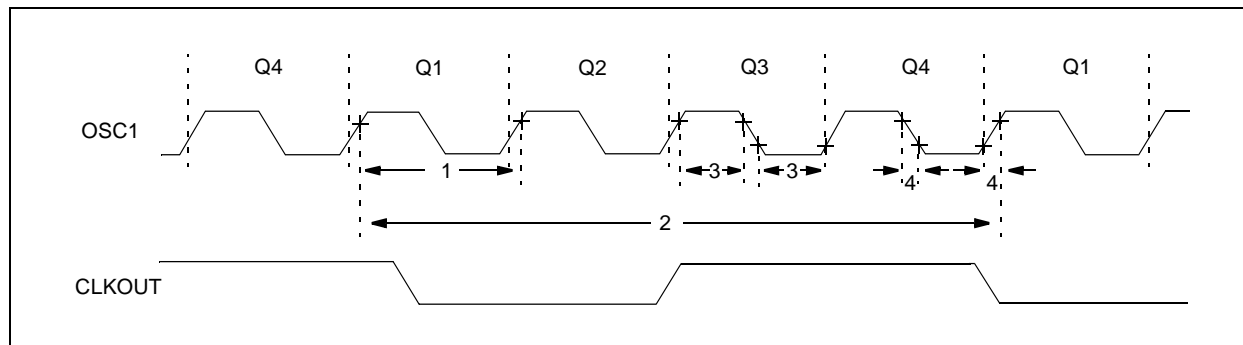
TABLE 13-1:   EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C $\leq$ TA $\leq$ +70°C for commercial −40°C $\leq$ TA $\leq$ +85°C for industrial −40°C $\leq$ TA $\leq$ +125°C for extended					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency[1]	DC	—	4.0	MHz	XT OSC mode
			DC	—	4.0	MHz	HS OSC mode (04)
			DC	—	10	MHz	HS OSC mode (10)
			DC	—	20	MHz	HS OSC mode (20)
			DC	—	200	kHz	LP OSC mode
		Oscillator Frequency[1]	DC	—	4.0	MHz	RC OSC mode
			0.1	—	4.0	MHz	XT OSC mode
			4.0	—	4.0	MHz	HS OSC mode (04)
			4.0	—	10	MHz	HS OSC mode (10)
			4.0	—	20	MHz	HS OSC mode (20)
			5.0	—	200	kHz	LP OSC mode

*   These parameters are characterized but not tested.

†   Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

15.0   ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings[†]

Ambient temperature under bias.. −55°C to +125°C

Storage temperature .... −65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ....0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS}... 0 to +14V

Voltage on all other pins with respect to V_{SS} ....−0.6V to (V_{DD} + 0.6V)

Total power dissipation[1] ....800 mW

Max. current out of V_{SS} pin .... 150 mA

Max. current into V_{DD} pin .... 100 mA

Max. current into an input pin (T0CKI only) .... ±500 µA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})..±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ....±20 mA

Max. output current sunk by any I/O pin .... 25 mA

Max. output current sourced by any I/O pin .... 20 mA

Max. output current sourced by a single I/O port (PORTA or B) .... 50 mA

Max. output current sunk by a single I/O port (PORTA or B) .... 50 mA

Note 1: Power dissipation is calculated as follows: Pdis = V_{DD} x {I_{DD} - $\sum I_{OH}$} + $\sum$ {(V_{DD}-V_{OH}) x I_{OH}} + $\sum$(V_{OL} x I_{OL})

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

18.0   DEVICE CHARACTERIZATION - PIC16LC54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 18-1:   TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE
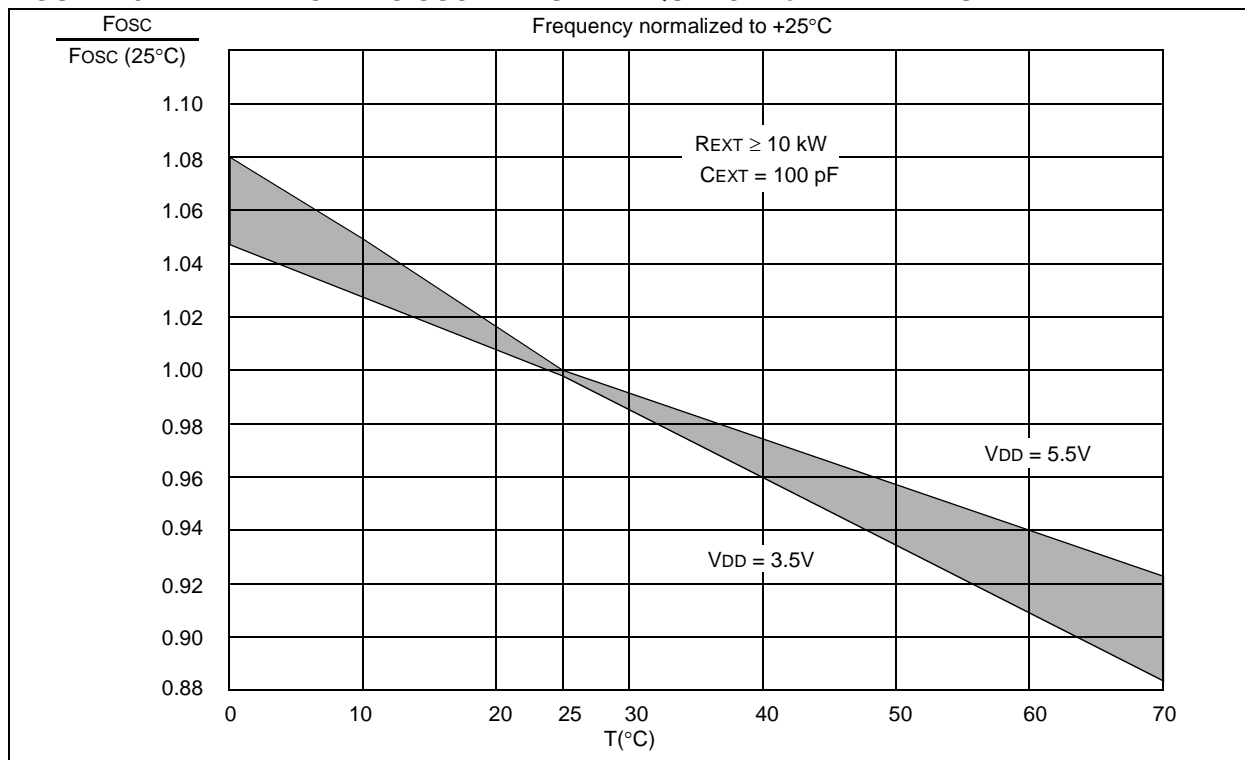
TABLE 18-1:   RC OSCILLATOR FREQUENCIES

CEXT	REXT	Average Fosc @ 5V, 25°C	
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.63 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

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FIGURE 18-2: **TYPICAL RC OSCILLATOR FREQUENCY vs. V$_{DD}$, C$_{EXT}$ = 20 PF, 25°C**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

R=3.3K
R=5K
R=10K
R=100K

V$_{DD}$ (Volts)
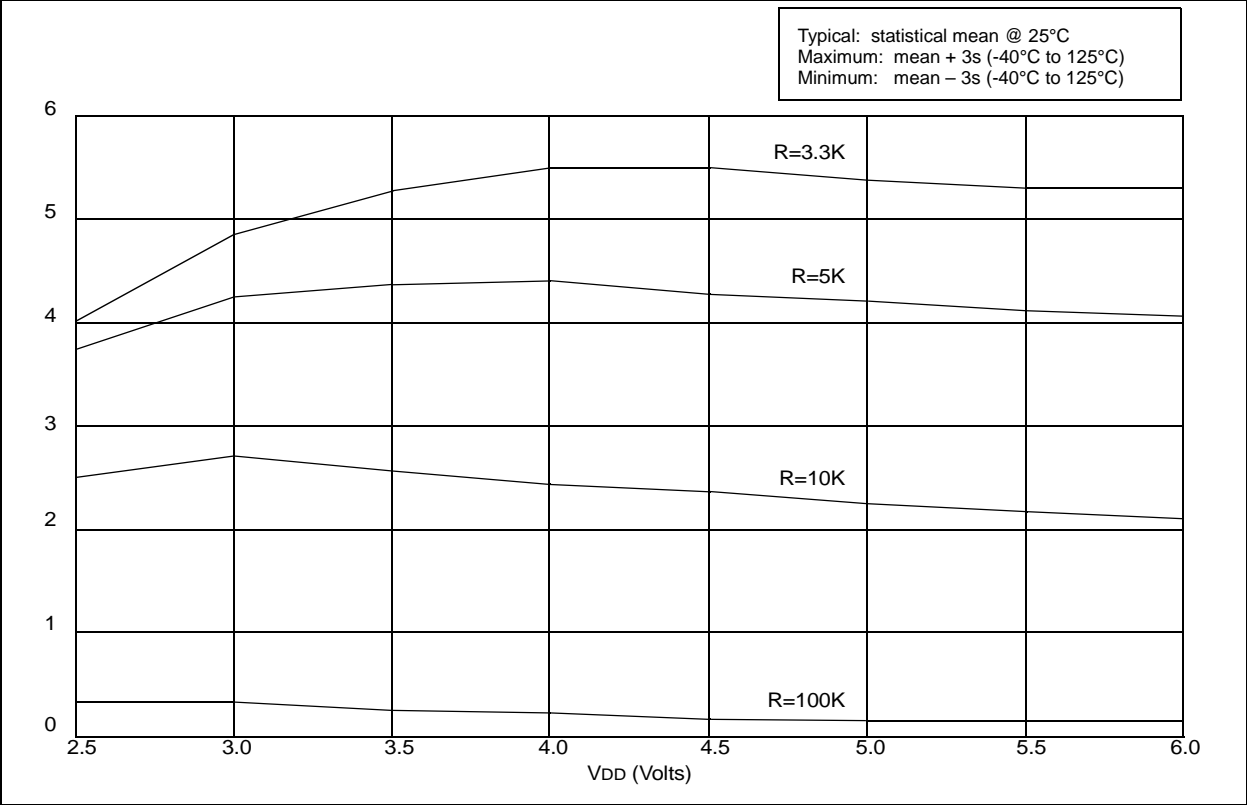
FIGURE 18-3: **TYPICAL RC OSCILLATOR FREQUENCY vs. V$_{DD}$, C$_{EXT}$ = 100 PF, 25°C**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

F$_{OSC}$ (MHz)

R=3.3K
R=5K
R=10K
R=100K

V$_{DD}$ (Volts)

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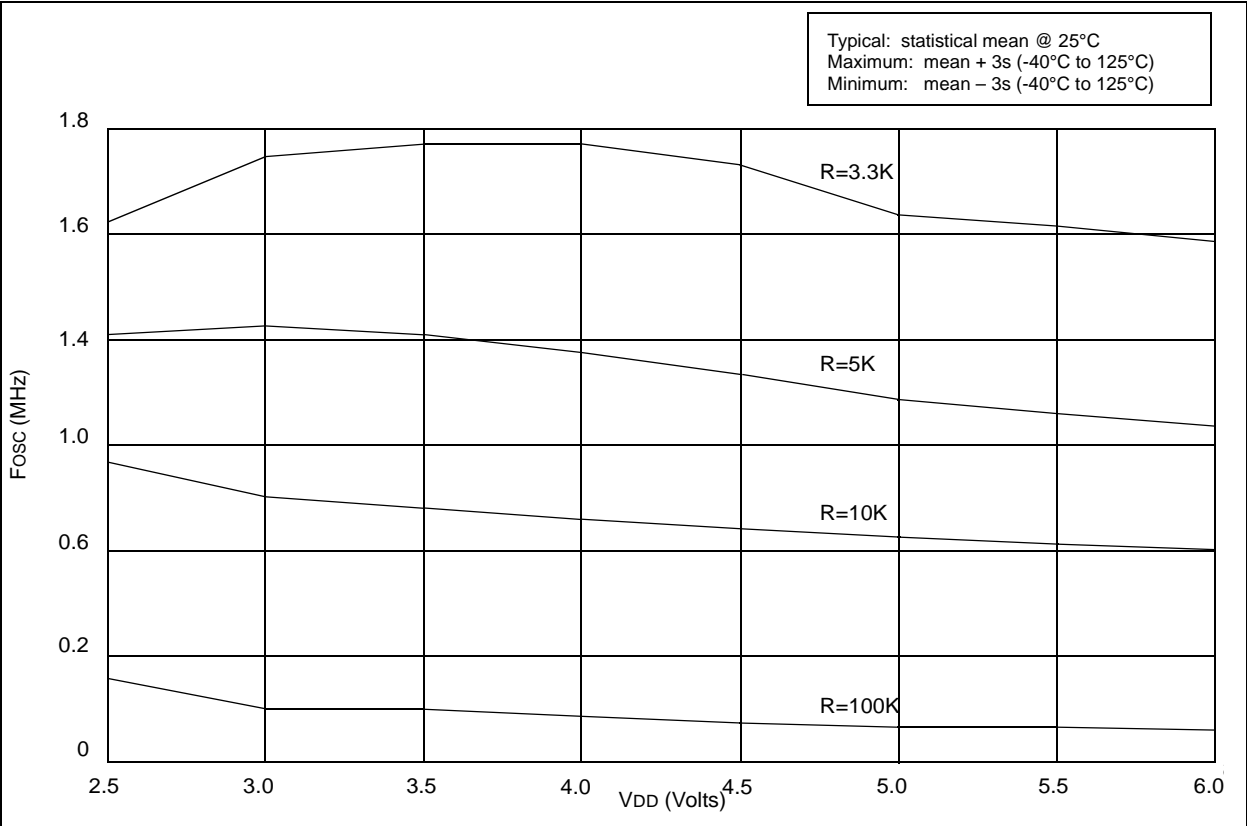
FIGURE 18-6: **TYPICAL I_{PD} vs. V_{DD}, WATCHDOG ENABLED (25°C)**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)
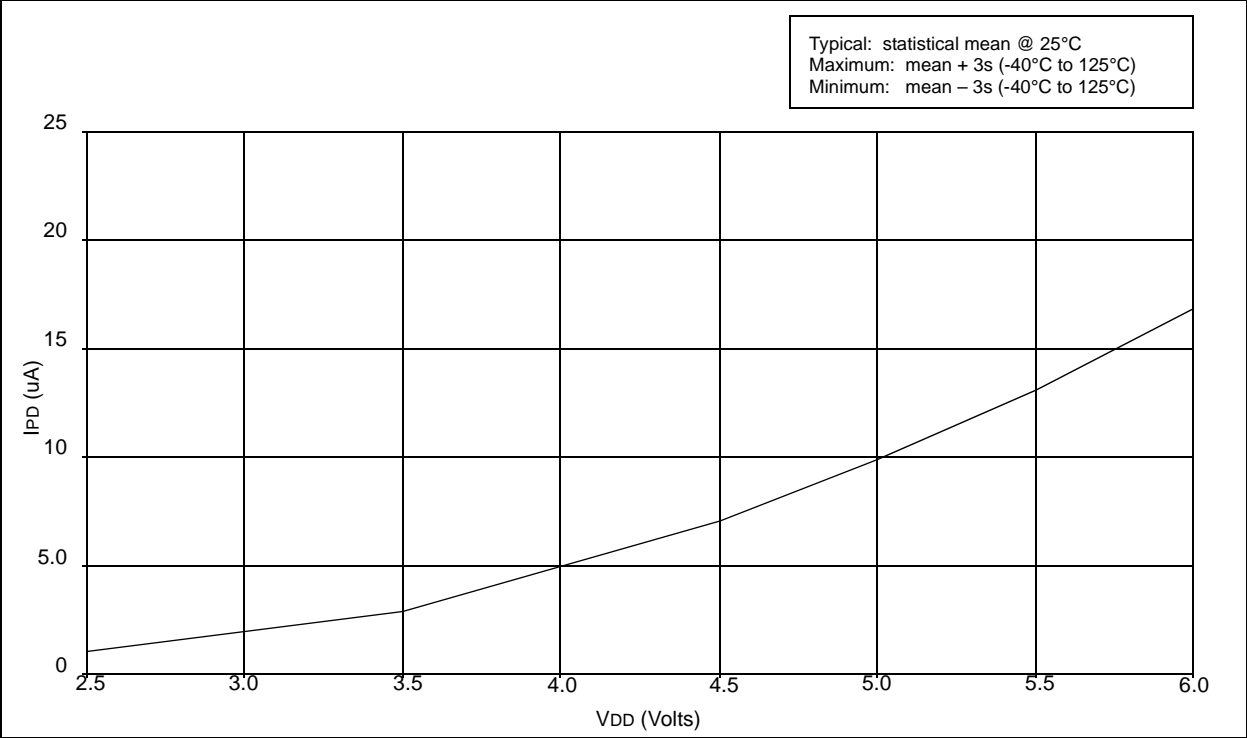
FIGURE 18-7: **TYPICAL I_{PD} vs. V_{DD}, WATCHDOG ENABLED (−40°C, 85°C)**

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Preliminary

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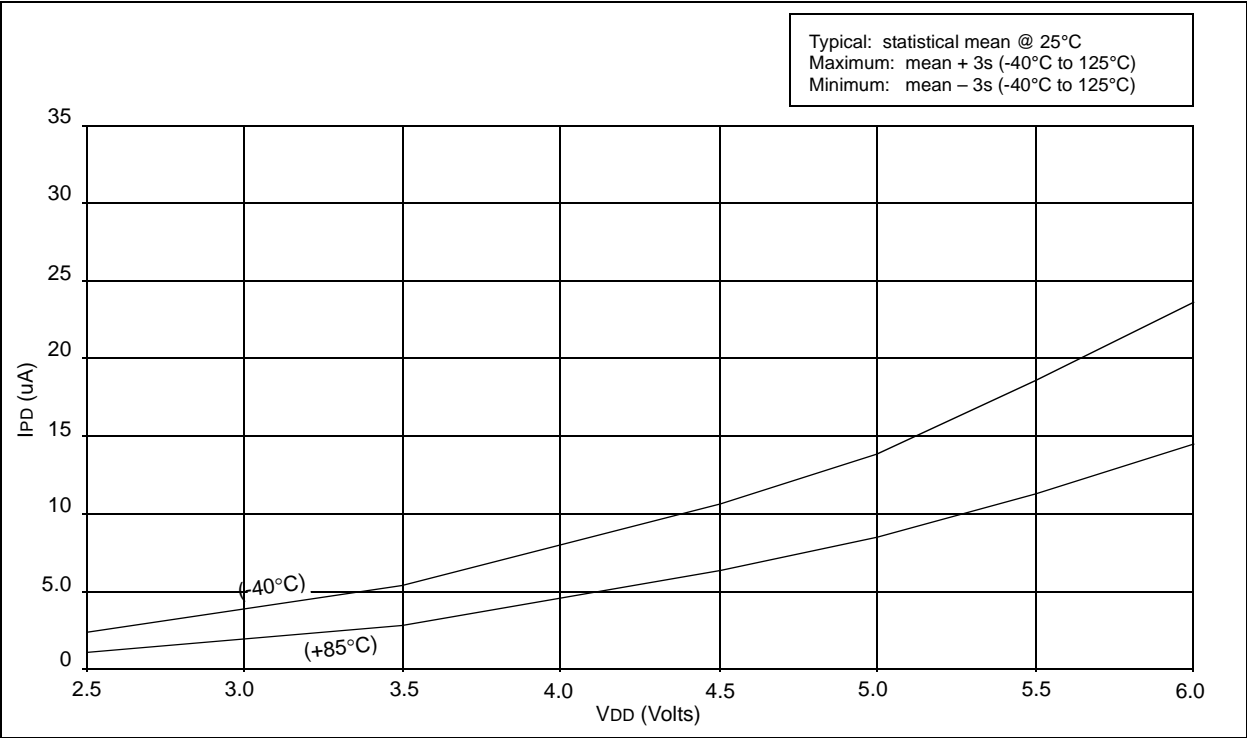
19.0   ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

Absolute Maximum Ratings[†]

Ambient temperature under bias .... −55°C to +125°C

Storage temperature .... −65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +14V

Voltage on all other pins with respect to V_{SS} .... −0.6V to (V_{DD} + 0.6V)

Total power dissipation[1] .... 800 mW

Max. current out of V_{SS} pin .... 150 mA

Max. current into V_{DD} pin .... 100 mA

Max. current into an input pin (T0CKI only) .... ±500 μA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) .... ±20 mA

Max. output current sunk by any I/O pin .... 25 mA

Max. output current sourced by any I/O pin .... 20 mA

Max. output current sourced by a single I/O (Port A, B or C) .... 50 mA

Max. output current sunk by a single I/O (Port A, B or C) .... 50 mA

   Note 1: Power dissipation is calculated as follows: Pdis = V_{DD} x {I_{DD} - $\sum I_{OH}$} + $\sum$ {(V_{DD}-V_{OH}) x I_{OH}} + $\sum$(V_{OL} x I_{OL})

---

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
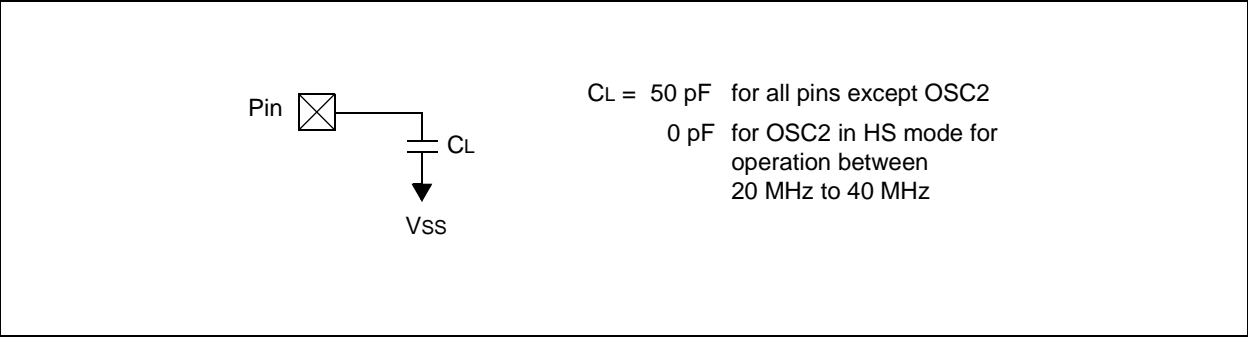

19.3   Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 19-2:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/C55A/C56A/C57C/C58B-40

Pin

C_L

Vss

C_L = 50 pF   for all pins except OSC2

0 pF   for OSC2 in HS mode for operation between 20 MHz to 40 MHz

20.0   DEVICE CHARACTERIZATION - PIC16LC54C 40MHz

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

 "Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

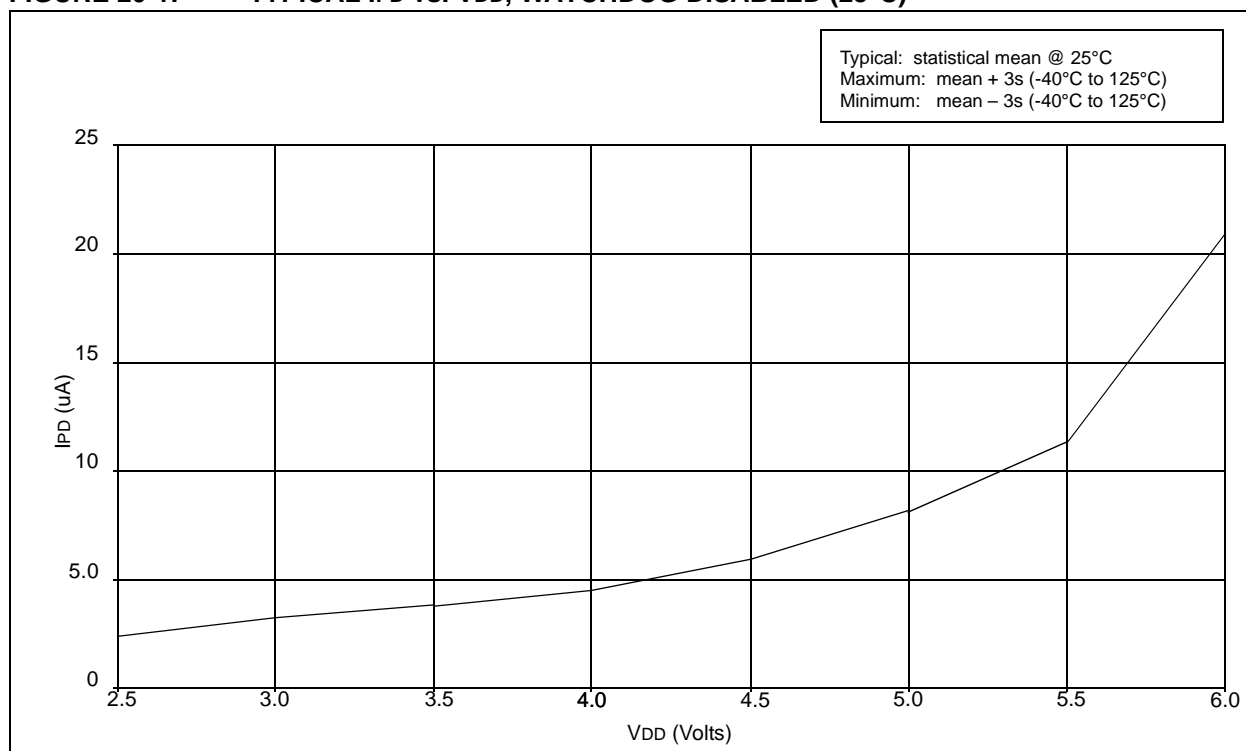**FIGURE 20-1:   TYPICAL I$_{PD}$ vs. V$_{DD}$, WATCHDOG DISABLED (25°C)**
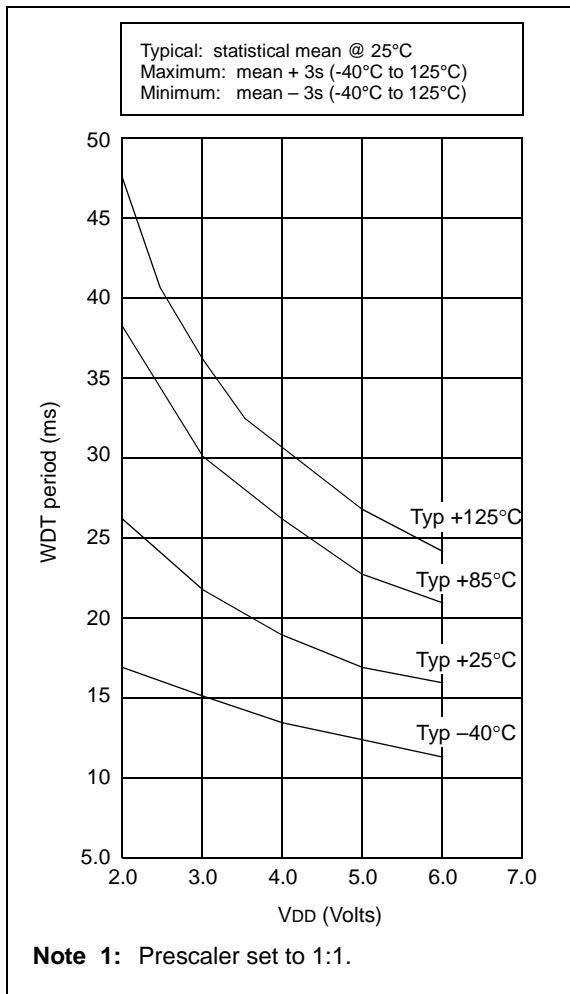
FIGURE 20-7: WDT TIMER TIME-OUT PERIOD vs. VDD[1]

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Typ +125°C
Typ +85°C
Typ +25°C
Typ –40°C

Note 1: Prescaler set to 1:1.

FIGURE 20-8: IOH vs. VOH, VDD = 5 V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Typ +125°C
Typ +85°C
Typ +25°C
Typ –40°C
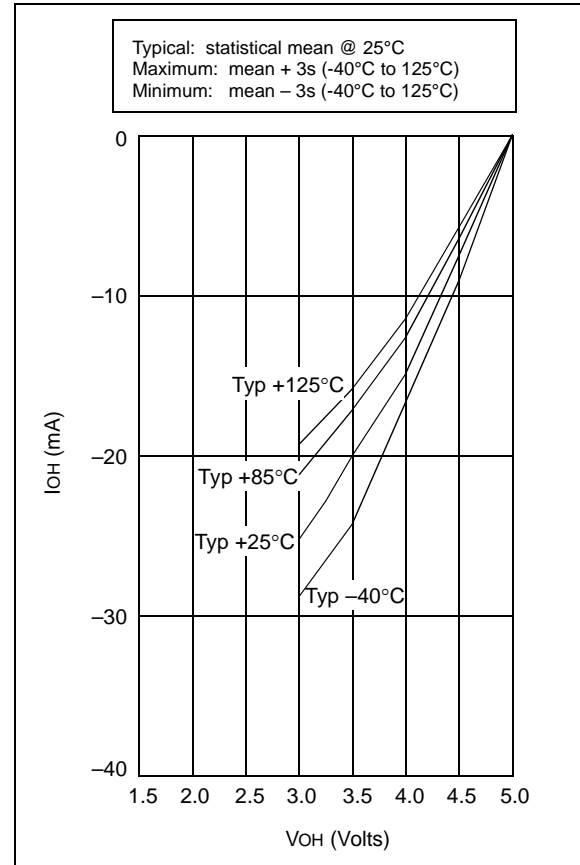
TABLE 20-1:   INPUT CAPACITANCE

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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FIGURE 20-9: IOL vs. VOL, VDD = 5 V

Typical: statistical mean @ 25°C
Maximum: mean + 3s (-40°C to 125°C)
Minimum: mean – 3s (-40°C to 125°C)

Max –40°C

Typ +25°C

Min +85°C

IOL (mA)

VOL (Volts)

Preliminary © 1997-2013 Microchip Technology Inc.
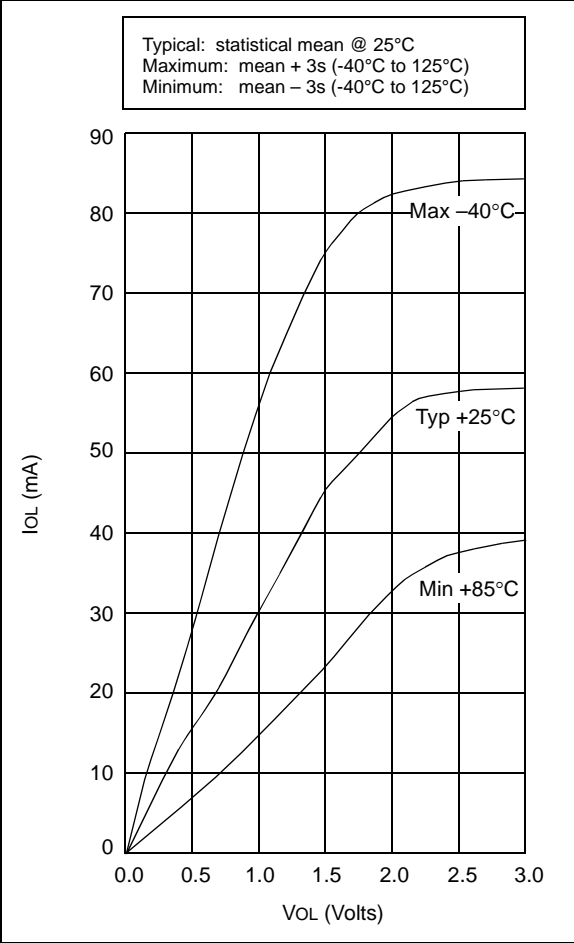
18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
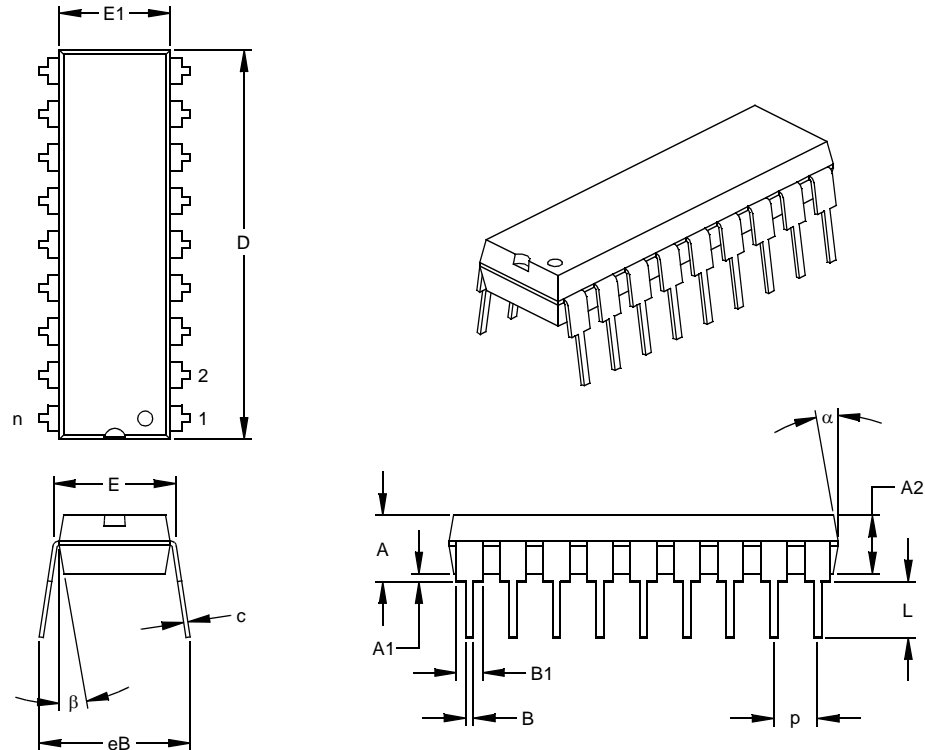
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
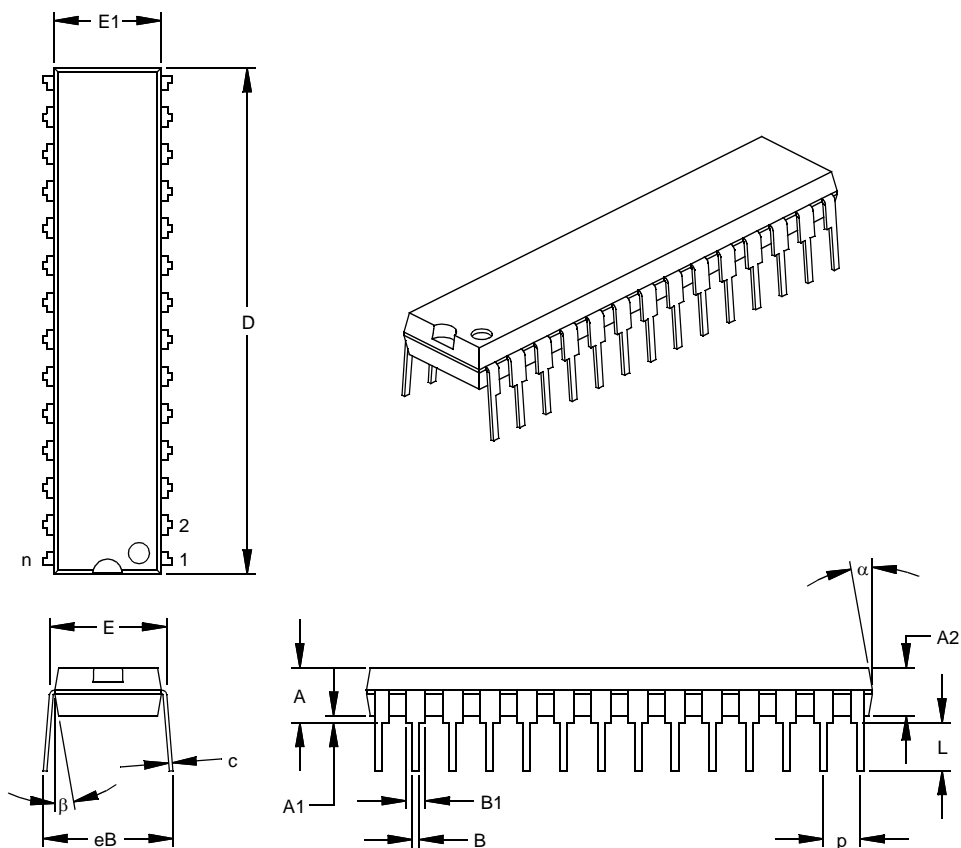JEDEC Equivalent: MS-001
Drawing No. C04-007

PIC16C5X

28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

		Units	INCHES*			MILLIMETERS		
	Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins		n		28			28	
Pitch		p		.100			2.54	
Top to Seating Plane		A	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness		A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane		A1	.015			0.38		
Shoulder to Shoulder Width		E	.300	.310	.325	7.62	7.87	8.26
Molded Package Width		E1	.275	.285	.295	6.99	7.24	7.49
Overall Length		D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane		L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness		c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width		B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width		B	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing §		eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top		α	5	10	15	5	10	15
Mold Draft Angle Bottom		β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-095
Drawing No. C04-070

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PIC16C5X

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change RESET vector to proper value for processor used.
6. Remove any use of the `ADDLW,` `RETURN` and `SUBLW` instructions.
7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

Preliminary