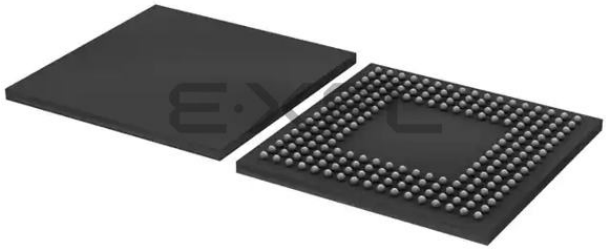

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	160
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	98K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2468fet208-551

- Two independent power domains allow fine tuning of power consumption based on needed features.
- Each peripheral has its own clock divider for further power saving. These dividers help reduce active power by 20 % to 30 %.
- Brownout detect with separate thresholds for interrupt and forced reset.
- On-chip power-on reset.
- On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as the system clock. When used as the CPU clock, does not allow CAN and USB to run.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Boundary scan for simplified board testing.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.

3. Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2468FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC2468FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					External bus	Ethernet	USB OTG/ OHC/ device + 4 kB FIFO	CAN channels	SD/ MMC	GP DMA	ADC channels	DAC channels	Temp range
		Local bus	Ethernet buffer	GP/USB	RTC	Total									
LPC2468FBD208	512	64	16	16	2	98	Full 32-bit	MII/RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C
LPC2468FET208	512	64	16	16	2	98	Full 32-bit	MII/RMII	yes	2	yes	yes	8	1	−40 °C to +85 °C

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
17	P1[5]/ENET_TX_ER/ MCIPWR/PWM0[3]		-		-		-
Row B							
1	P3[2]/D2	2	P3[10]/D10	3	P3[1]/D1	4	P3[0]/D0
5	P1[1]/ENET_TXD1	6	V_{SSIO}	7	P4[30]/$\overline{CS0}$	8	P4[24]/$\overline{OE}$
9	P4[25]/$\overline{WE}$	10	P4[29]/$\overline{BLS3}$/ MAT2[1]/RXD3	11	P1[6]/ENET_TX_CLK/ MCIDAT0/PWM0[4]	12	P0[4]/I2SRX_CLK/RD2/ CAP2[0]
13	$V_{DD(3V3)}$	14	P3[19]/D19/ PWM0[4]/DCD1	15	P4[14]/A14	16	P4[13]/A13
17	P2[0]/PWM1[1]/TXD1/ TRACECLK		-		-		-
Row C							
1	P3[13]/D13	2	TDI	3	RTCK	4	P0[2]/TXD0
5	P3[9]/D9	6	P3[22]/D22/ PCAP0[0]/RI1	7	P1[8]/ENET_CRS_DV/ ENET_CRS	8	P1[10]/ENET_RXD1
9	$V_{DD(3V3)}$	10	P3[21]/D21/ PWM0[6]/DTR1	11	P4[28]/$\overline{BLS2}$/ MAT2[0]/TXD3	12	P0[5]/I2SRX_WS/TD2/ CAP2[1]
13	P0[7]/I2STX_CLK/SCK1 /MAT2[1]	14	P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	15	P3[18]/D18/ PWM0[3]/CTS1	16	P4[12]/A12
17	$V_{DD(3V3)}$		-		-		-
Row D							
1	$\overline{TRST}$	2	P3[28]/D28/ CAP1[1]/PWM1[5]	3	TDO	4	P3[12]/D12
5	P3[11]/D11	6	P0[3]/RXD0	7	$V_{DD(3V3)}$	8	P3[8]/D8
9	P1[2]/ENET_TXD2/ MCICLK/PWM0[1]	10	P1[16]/ENET_MDC	11	$V_{DD(DCDC)(3V3)}$	12	V_{SSCORE}
13	P0[6]/I2SRX_SDA/ SSEL1/MAT2[0]	14	P1[7]/ENET_COL/ MCIDAT1/PWM0[5]	15	P2[2]/PWM1[3]/ CTS1/PIPESTAT1	16	P1[13]/ENET_RX_DV
17	P2[4]/PWM1[5]/ DSR1/TRACESYNC		-		-		-
Row E							
1	P0[26]/AD0[3]/ AOUT/RXD3	2	TCK	3	TMS	4	P3[3]/D3
14	P2[1]/PWM1[2]/RXD1/ PIPESTAT0	15	V_{SSIO}	16	P2[3]/PWM1[4]/ DCD1/PIPESTAT2	17	P2[6]/PCAP1[0]/ RI1/TRACEPKT1
Row F							
1	P0[25]/AD0[2]/ I2SRX_SDA/TXD3	2	P3[4]/D4	3	P3[29]/D29/ MAT1[0]/PWM1[6]	4	DBGEN
14	P4[11]/A11	15	P3[17]/D17/ PWM0[2]/RXD1	16	P2[5]/PWM1[6]/ DTR1/TRACEPKT0	17	P3[16]/D16/ PWM0[1]/TXD1
Row G							
1	P3[5]/D5	2	P0[24]/AD0[1]/ I2SRX_WS/CAP3[1]	3	$V_{DD(3V3)}$	4	V_{DDA}
14	n.c.	15	P4[27]/$\overline{BLS1}$	16	P2[7]/RD2/ RTS1/TRACEPKT2	17	P4[10]/A10

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P0[21]/RI1/ MCIPWR/RD1	118[1]	M16[1]	I/O	**P0[21] —** General purpose digital input/output pin.
			I	**RI1 —** Ring Indicator input for UART1.
			O	**MCIPWR —** Power Supply Enable for external SD/MMC power supply.
			I	**RD1 —** CAN1 receiver input.
P0[22]/RTS1/ MCIDAT0/TD1	116[1]	N17[1]	I/O	**P0[22] —** General purpose digital input/output pin.
			O	**RTS1 —** Request to Send output for UART1.
			I/O	**MCIDAT0 —** Data line 0 for SD/MMC interface.
			O	**TD1 —** CAN1 transmitter output.
P0[23]/AD0[0]/ I2SRX_CLK/ CAP3[0]	18[2]	H1[2]	I/O	**P0[23] —** General purpose digital input/output pin.
			I	**AD0[0] —** A/D converter 0, input 0.
			I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I	**CAP3[0] —** Capture input for Timer 3, channel 0.
P0[24]/AD0[1]/ I2SRX_WS/ CAP3[1]	16[2]	G2[2]	I/O	**P0[24] —** General purpose digital input/output pin.
			I	**AD0[1] —** A/D converter 0, input 1.
			I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			I	**CAP3[1] —** Capture input for Timer 3, channel 1.
P0[25]/AD0[2]/ I2SRX_SDA/ TXD3	14[2]	F1[2]	I/O	**P0[25] —** General purpose digital input/output pin.
			I	**AD0[2] —** A/D converter 0, input 2.
			I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			O	**TXD3 —** Transmitter output for UART3.
P0[26]/AD0[3]/ AOUT/RXD3	12[2][3]	E1[2][3]	I/O	**P0[26] —** General purpose digital input/output pin.
			I	**AD0[3] —** A/D converter 0, input 3.
			O	**AOUT —** D/A converter output.
			I	**RXD3 —** Receiver input for UART3.
P0[27]/SDA0	50[4]	T1[4]	I/O	**P0[27] —** General purpose digital input/output pin.
			I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
P0[28]/SCL0	48[4]	R3[4]	I/O	**P0[28] —** General purpose digital input/output pin.
			I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
P0[29]/USB_D+1	61[5]	U4[5]	I/O	**P0[29] —** General purpose digital input/output pin.
			I/O	**USB_D+1 —** USB port 1 bidirectional D+ line.
P0[30]/USB_D−1	62[5]	R6[5]	I/O	**P0[30] —** General purpose digital input/output pin.
			I/O	**USB_D−1 —** USB port 1 bidirectional D− line.
P0[31]/USB_D+2	51[5]	T2[5]	I/O	**P0[31] —** General purpose digital input/output pin.
			I/O	**USB_D+2 —** USB port 2 bidirectional D+ line.
P1[0] to P1[31]			I/O	**Port 1:** Port 1 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect block.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[24]/ USB_RX_DM1/ PWM1[5]/MOSI0	78[1]	T9[1]	I/O	**P1[24] —** General purpose digital input/output pin.
			I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
			O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
			I/O	**MOSI0 —** Master Out Slave in for SSP0.
P1[25]/ USB_LS1/ USB_HSTEN1/ MAT1[1]	80[1]	T10[1]	I/O	**P1[25] —** General purpose digital input/output pin.
			O	**USB_LS1 —** Low-speed status for USB port 1 (OTG transceiver).
			O	**USB_HSTEN1 —** Host Enabled status for USB port 1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
P1[26]/ USB_SSPND1/ PWM1[6]/ CAP0[0]	82[1]	R10[1]	I/O	**P1[26] —** General purpose digital input/output pin.
			O	**USB_SSPND1 —** USB port 1 Bus Suspend status (OTG transceiver).
			O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/ USB_INT1/ USB_OVRCR1/ CAP0[1]	88[1]	T12[1]	I/O	**P1[27] —** General purpose digital input/output pin.
			I	**USB_INT1 —** USB port 1 OTG transceiver interrupt (OTG transceiver).
			I	**USB_OVRCR1 —** USB port 1 Over-Current status.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/ USB_SCL1/ PCAP1[0]/ MAT0[0]	90[1]	T13[1]	I/O	**P1[28] —** General purpose digital input/output pin.
			I/O	**USB_SCL1 —** USB port 1 I^2C serial clock (OTG transceiver).
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/ USB_SDA1/ PCAP1[1]/ MAT0[1]	92[1]	U14[1]	I/O	**P1[29] —** General purpose digital input/output pin.
			I/O	**USB_SDA1 —** USB port 1 I^2C serial data (OTG transceiver).
			I	**PCAP1[1] —** Capture input for PWM1, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 0.
P1[30]/ USB_PWRD2/ V_{BUS}/AD0[4]	42[2]	P2[2]	I/O	**P1[30] —** General purpose digital input/output pin.
			I	**USB_PWRD2 —** Power Status for USB port 2.
			I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/ USB_OVRCR2/ SCK1/AD0[5]	40[2]	P1[2]	I/O	**P1[31] —** General purpose digital input/output pin.
			I	**USB_OVRCR2 —** Over-Current status for USB port 2.
			I/O	**SCK1 —** Serial Clock for SSP1.
			I	**AD0[5] —** A/D converter 0, input 5.
P2[0] to P2[31]			I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect block.
P2[0]/PWM1[1]/ TXD1/ TRACECLK	154[1]	B17[1]	I/O	**P2[0] —** General purpose digital input/output pin.
			O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
			O	**TXD1 —** Transmitter output for UART1.
			O	**TRACECLK —** Trace Clock.

The Thumb set's 16-bit instruction length allows it to approach higher density compared to standard ARM code while retaining most of the ARM's performance.

7.2 On-chip flash programming memory

The LPC2468 incorporates 512 kB flash memory system. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port (UART0). The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field and firmware upgrades.

The flash memory is 128 bits wide and includes pre-fetching and buffering techniques to allow it to operate at speeds of 72 MHz.

7.3 On-chip SRAM

The LPC2468 includes a SRAM memory of 64 kB reserved for the ARM processor exclusive use. This RAM may be used for code and/or data storage and may be accessed as 8 bits, 16 bits, and 32 bits.

A 16 kB SRAM block serving as a buffer for the Ethernet controller and a 16 kB SRAM associated with the second AHB can be used both for data and code storage. The 2 kB RTC SRAM can be used for data storage only. The RTC SRAM is battery powered and retains the content in the absence of the main power supply.

7.4 Memory map

The LPC2468 memory map incorporates several distinct regions as shown in Table 5 and Figure 4.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (default), boot ROM or SRAM (see Section 7.26.6).

Table 5. LPC2468 memory usage and details

Address range	General use	Address range details and description	
0x0000 0000 to 0x3FFF FFFF	on-chip non-volatile memory and Fast I/O	0x0000 0000 - 0x0007 FFFF	flash memory (512 kB)
		0x3FFF C000 - 0x3FFF FFFF	fast GPIO registers
0x4000 0000 to 0x7FFF FFFF	on-chip RAM	0x4000 0000 - 0x4000 FFFF	RAM (64 kB)
		0x7FE0 0000 - 0x7FE0 3FFF	Ethernet RAM (16 kB)
		0x7FD0 0000 - 0x7FD0 3FFF	USB RAM (16 kB)

- Asynchronous page mode read
- Programmable Wait States
- Bus turnaround delay
- Output enable and write enable delays
- Extended wait

- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control CKE and CLKOUT to SDRAMs
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048, 4096, and 8192 row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.8 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected LPC2468 peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master.

7.8.1 Features

- Two DMA channels. Each channel can support a unidirectional transfer.
- The GPDMA can transfer data between the 16 kB SRAM, external memory, and peripherals such as the SD/MMC, two SSPs, and the I^2S interface.
- Single DMA and burst DMA request signals. Each peripheral connected to the GPDMA can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the GPDMA.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority. Each DMA channel has a specific hardware priority. DMA channel 0 has the highest priority and channel 1 has the lowest priority. If requests from two channels become active at the same time, the channel with the highest priority is serviced first.
- AHB slave DMA programming interface. The GPDMA is programmed by writing to the DMA control registers over the AHB slave interface.

- Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

- Physical interface:
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.11 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC2468 USB interface includes a device, host, and OTG controller. Details on typical USB interfacing solutions can be found in Section 14.1 “Suggested USB interface solutions” on page 69.

7.11.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

7.11.1.1 Features

- Fully compliant with *USB 2.0 Specification (full speed)*.
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, LPC2468 can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with the DMA RAM of 16 kB on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.11.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the *OHCI specification*.

7.18.1 Features

- The MCI interface provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.
- Conforms to *Multimedia Card Specification v2.11*.
- Conforms to *Secure Digital Memory Card Physical Layer Specification, v0.96.*
- Can be used as a multimedia card bus or a secure digital memory card bus host. The SD/MMC can be connected to several multimedia cards or a single secure digital memory card.
- DMA supported through the GPDMA controller.

7.19 I^2C-bus serial I/O controller

The LPC2468 contains three I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial Data Line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus and can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2468 supports bit rates up to 400 kbit/s (Fast I^2C-bus).

7.19.1 Features

- I^2C0 is a standard I^2C compliant bus interface with open-drain pins.
- I^2C1 and I^2C2 use standard I/O pins and do not support powering off of individual devices connected to the same bus lines.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.

7.20 I^2S-bus serial I/O controllers

The I^2S-bus provides a standard communication interface for digital audio applications.

- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must 'release' new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

7.23 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

7.23.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the RTC clock, the Internal RC oscillator (IRC), or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring, for increased reliability.

7.24 RTC and battery RAM

The RTC is a set of counters for measuring time when system power is on, and optionally when power is off. It uses little power in Power-down and Deep power-down modes. On the LPC2468, the RTC can be clocked by a separate 32.768 kHz oscillator or by a programmable prescale divider based on the APB clock. The RTC is powered by its own power supply pin, VBAT, which can be connected to a battery or to the same 3.3 V supply used by the rest of the device.

7.25.4 Power control

The LPC2468 supports a variety of power control features. There are four special modes of processor power reduction: Idle mode, Sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The LPC2468 also implements a separate power domain in order to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small SRAM, referred to as the Battery RAM.

7.25.4.1 Idle mode

In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.25.4.2 Sleep mode

In Sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The 32 kHz RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

The Sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Sleep mode reduces chip power consumption to a very low value. The flash memory is left on in Sleep mode, allowing a very quick wake-up.

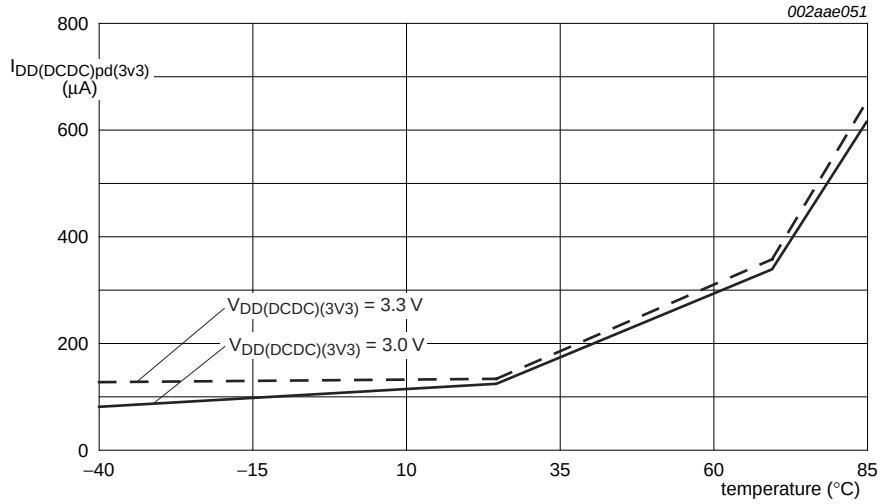
On the wake-up from Sleep mode, if the IRC was used before entering Sleep mode, the code execution and peripherals activities will resume after 4 cycles expire. If the main external oscillator was used, the code execution will resume when 4096 cycles expire.

The customers need to reconfigure the PLL and clock dividers accordingly.

7.25.4.3 Power-down mode

Power-down mode does everything that Sleep mode does, but also turns off the IRC oscillator and the flash memory. This saves more power, but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

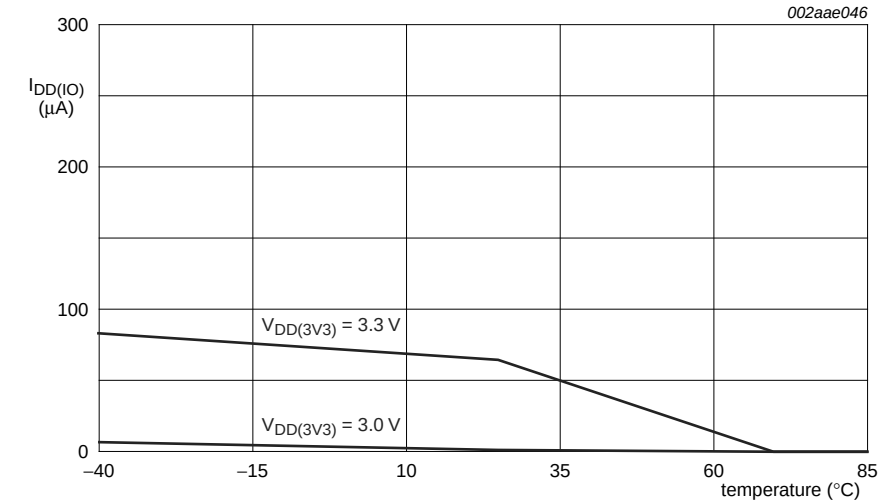
On the wake-up from Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 7. Total DC-to-DC converter supply current $I_{DD(DCDC)pd(3V3)}$ at different temperatures in Power-down mode

10.2 Deep power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 8. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Deep power-down mode

11. Dynamic characteristics

Table 10. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
I^2C-bus pins (P0[27]/SDA0 and P0[28]/SCL0)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns
SSP interface						
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 17	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

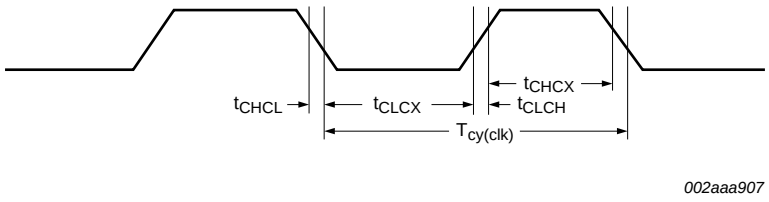


Fig 13. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.6 Dynamic external memory interface

Table 16. Dynamic characteristics: Dynamic external memory interface

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V, EMC Dynamic Read Config Register = 0x0 (RD = 00)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Common							
$t_{d(SV)}$	chip select valid delay time		[1]	-	1.05	1.76	ns
$t_{h(S)}$	chip select hold time		[1]	0.1	1.02	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		[1]	-	1.51	1.95	ns
$t_{h(RAS)}$	row address strobe hold time		[1]	0.5	1.51	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		[1]	-	0.98	1.27	ns
$t_{h(CAS)}$	column address strobe hold time		[1]	0.1	0.97	-	ns
$t_{d(WV)}$	write valid delay time		[1]	-	0.84	1.95	ns
$t_{h(W)}$	write hold time		[1]	0.1	0.84	-	ns
$t_{d(GV)}$	output enable valid delay time		[1]	-	0.95	1.86	ns
$t_{h(G)}$	output enable hold time		[1]	0.1	1	-	ns
$t_{d(AV)}$	address valid delay time		[1]	-	0.87	1.95	ns
$t_{h(A)}$	address hold time		[1]	0.1	0.81	-	ns
Read cycle parameters							
$t_{su(D)}$	data input set-up time		[1]	0.51	2.24	-	ns
$t_{h(D)}$	data input hold time		[1]	0.57	2.41	-	ns
Write cycle parameters							
$t_{d(QV)}$	data output valid delay time		[1]	-	2.65	4.36	ns
$t_{h(Q)}$	data output hold time		[1]	0.49	2.61	-	ns

[1] See Figure 18.

11.7 Timing

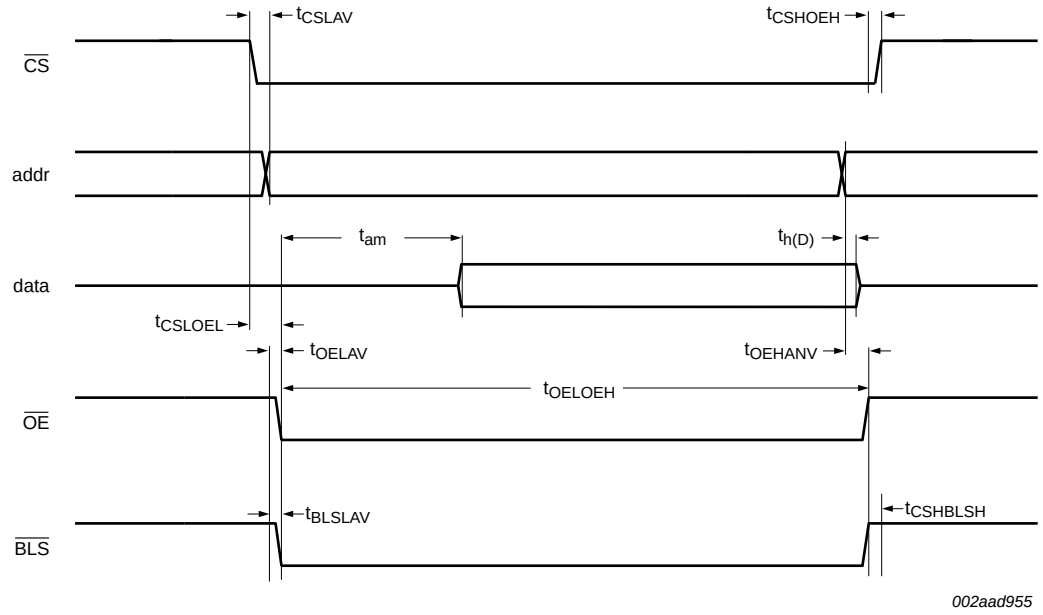


Fig 14. External memory read access

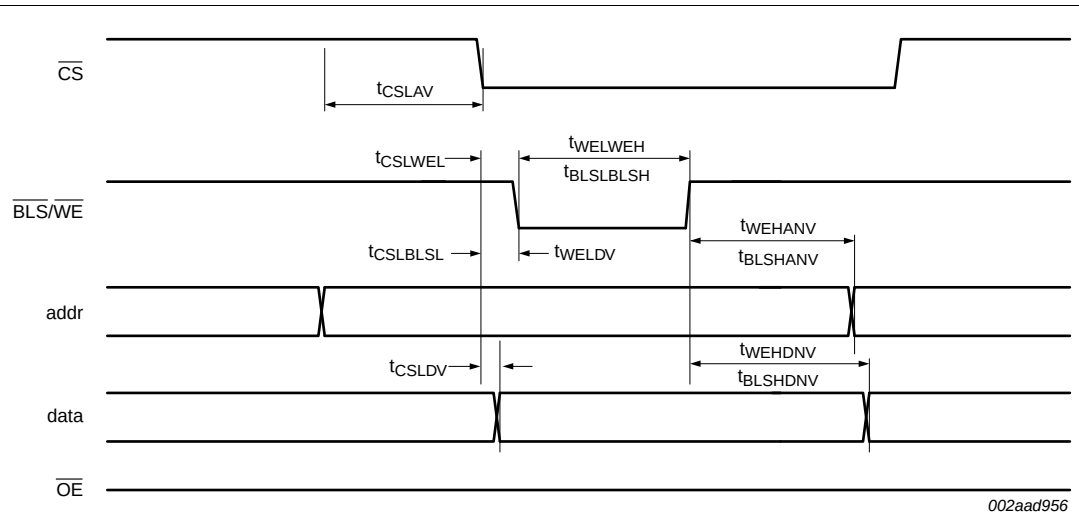


Fig 15. External memory write access

12. ADC electrical characteristics

Table 18. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	-	±2	LSB
E_O	offset error		[1][5]	-	-	±3	LSB
E_G	gain error		[1][6]	-	-	±0.5	%
E_T	absolute error		[1][7]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[8]	-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 19.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 19.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 19.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 19.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 19.

[8] See Figure 20.

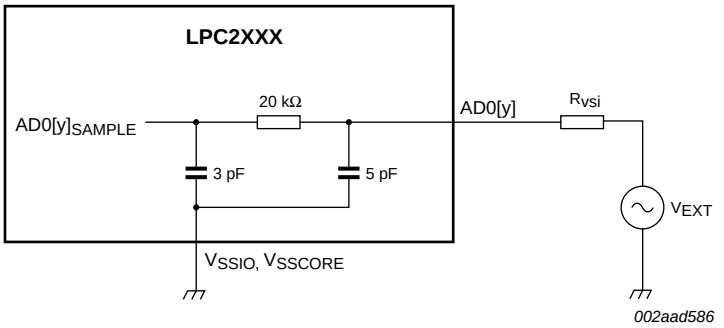


Fig 20. Suggested ADC interface - LPC2468 AD0[y] pin

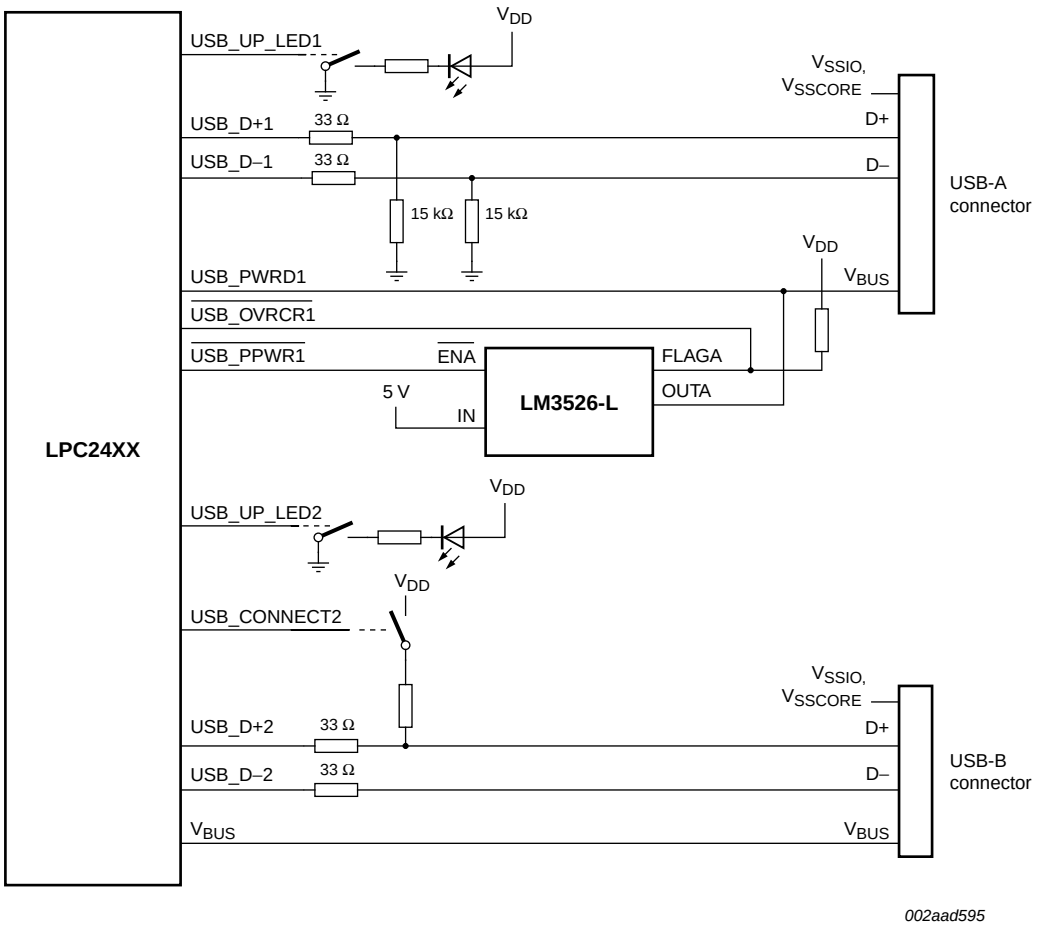


Fig 25. LPC2468 USB OTG port configuration: USB port 2 device, USB port 1 host

14.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1}, C_{X2}, and C_{X3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{X1} and C_{X2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

14.5 Standard I/O pin configuration

Figure 30 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Analog input (for ADC input channels)

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

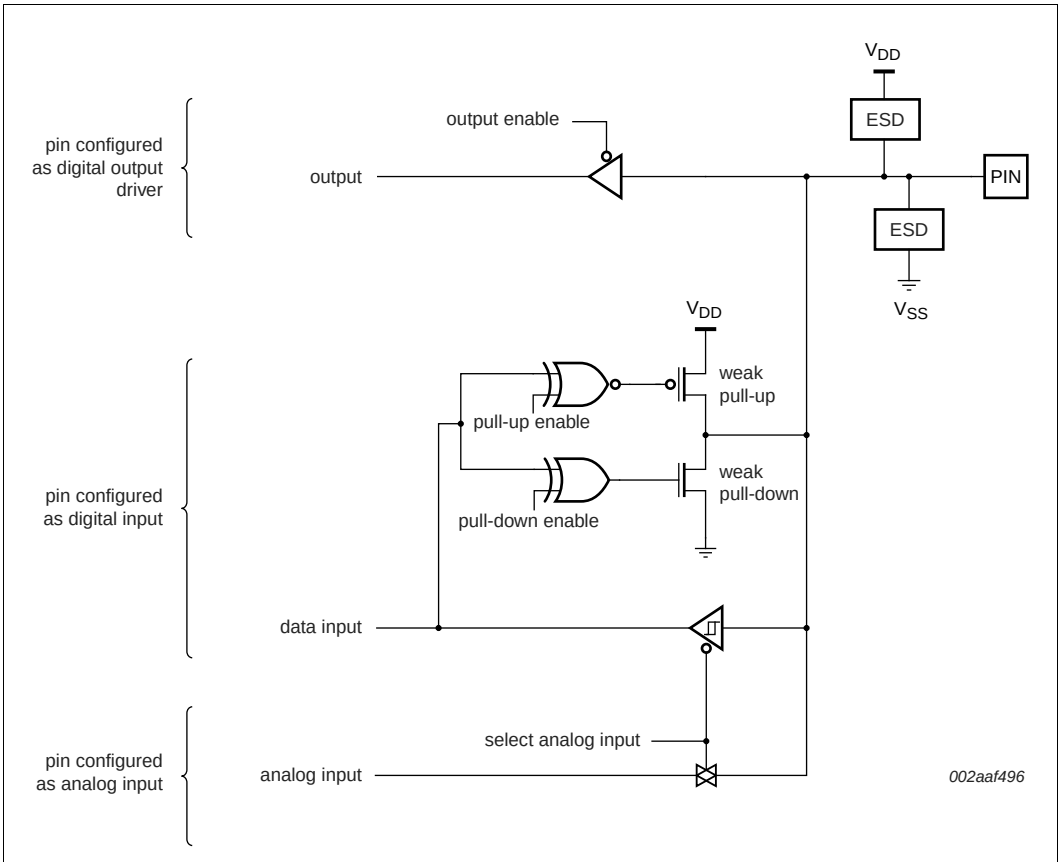
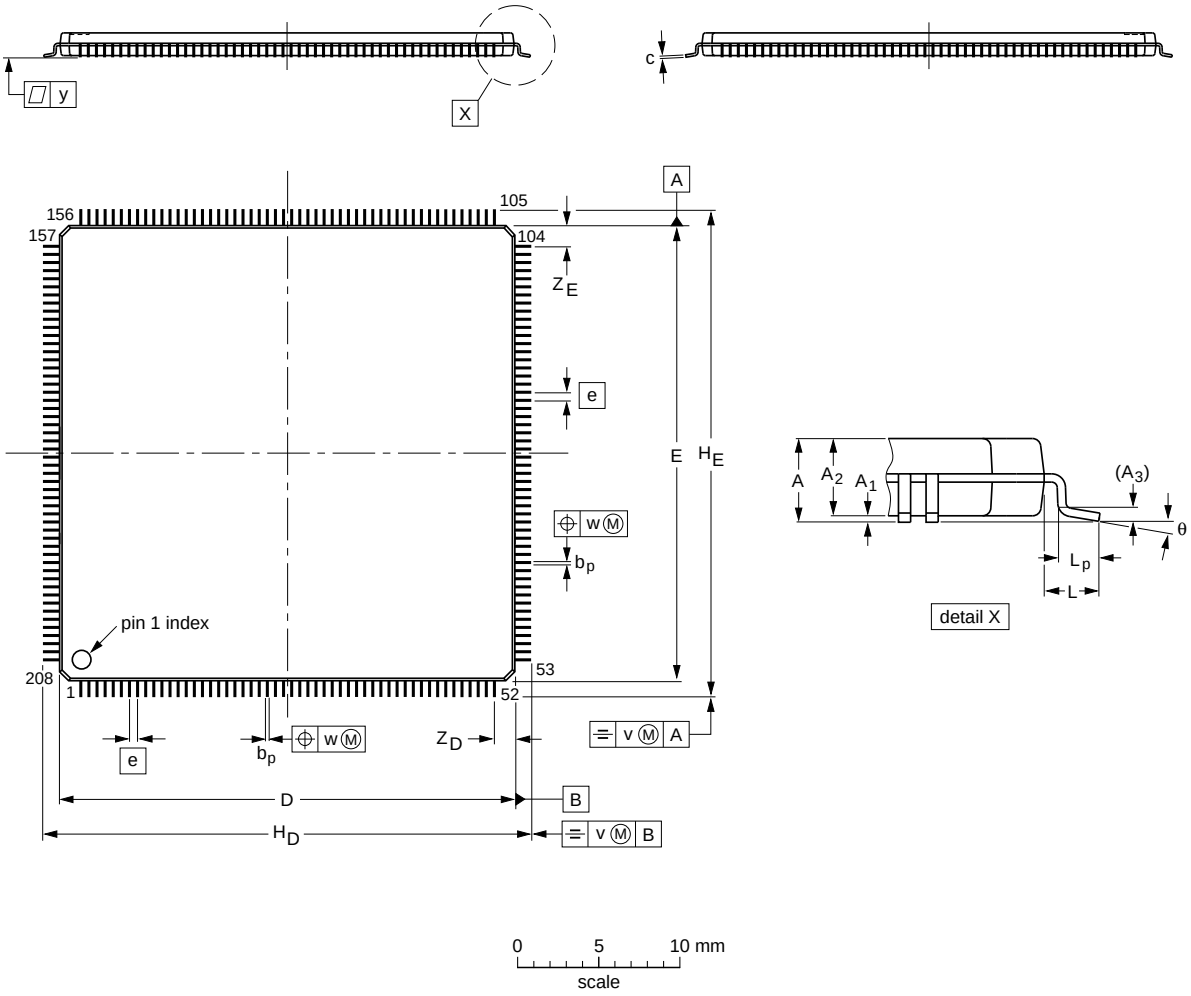


Fig 30. Standard I/O pin configuration with analog input

15. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

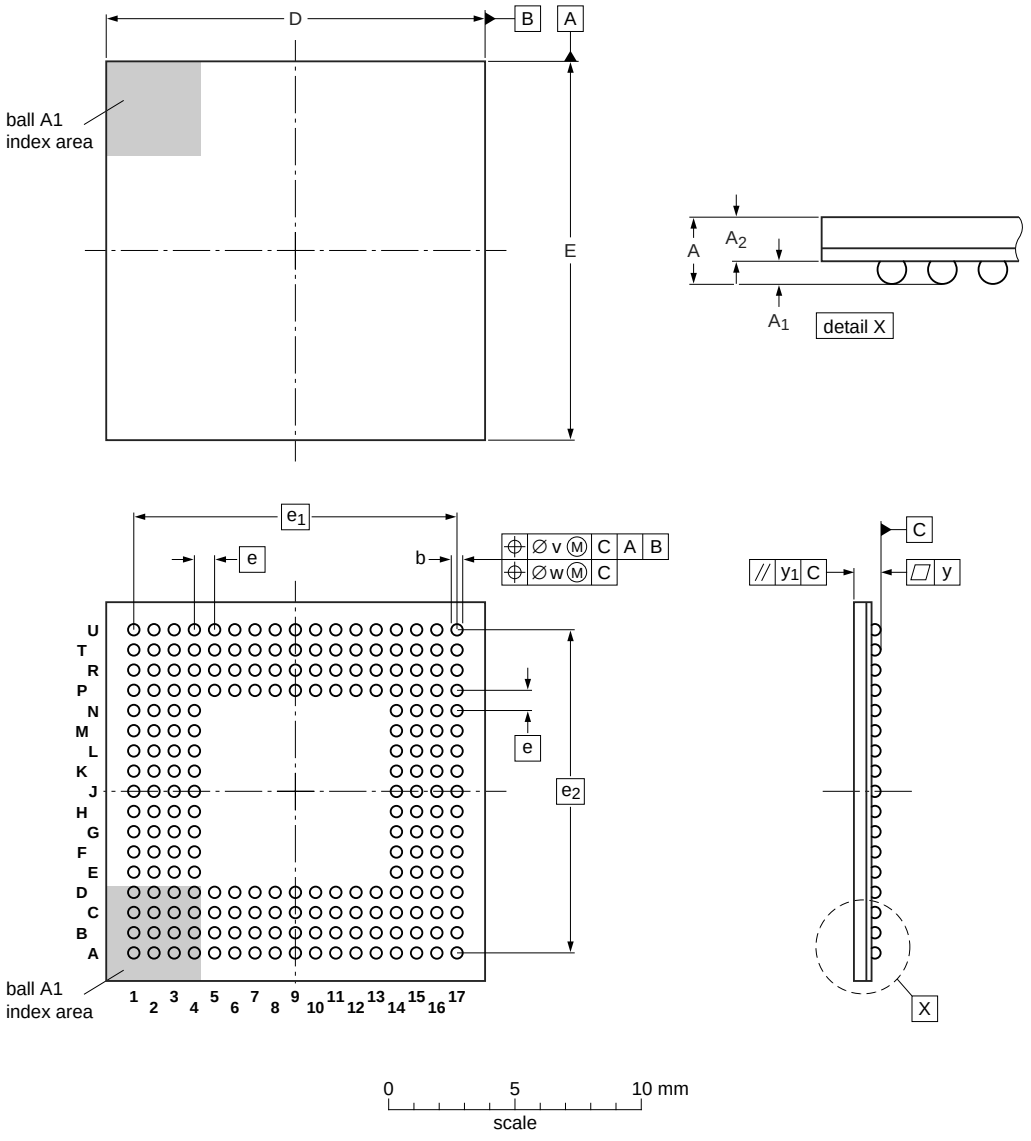
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 32. Package outline SOT459-1 (LQFP208)

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 33. Package outline SOT950-1 (TFBGA208)