E · K Fattice Semiconductor Corporation - <u>LCMXO3L-1300C-5BG256I Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	206
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-1300c-5bg256i

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Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3L/LF devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO3L/LF devices, please see TN1290, Memory Usage Guide for MachXO3 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4				
Number of slices	3	3				
Note: SPB = Single Port RAM_PDPB = Pseudo Dual Port RAM						

ote: SPR = Single Port RAM, PDPR = Pseudo Dual



Figure 2-6. Secondary High Fanout Nets for MachXO3L/LF Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO3L/LF devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO3L/LF sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO3L/LF clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.



Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	0	Primary PLL output clock (with phase shift adjustment)
CLKOS	0	Secondary PLL output clock (with phase shift adjust)
CLKOS2	0	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	0	Secondary PLL output clock3 (with phase shift adjust)
LOCK	0	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed- back signals.
DPHSRC	0	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	0	PLL data bus data output
PLLACK	0	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO3L/LF devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.



Figure 2-8. sysMEM Memory Primitives





If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1290, Memory Usage Guide for MachXO3 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO3L/LF devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO3L/LF devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

All PIO pairs can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these devices have on-chip differential termination and also provide PCI support.



Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-13 shows a block diagram of the input gearbox.



Table 2-11 shows the I/O standards (together with their supply and reference voltages) supported by the MachXO3L/LF devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1280, MachXO3 sysIO Usage Guide.

Table 2-11. Supported Input Standards

		V	CCIO (Ty	р.)	
Input Standard	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V
Single-Ended Interfaces					
LVTTL	Yes				
LVCMOS33	Yes				
LVCMOS25		Yes			
LVCMOS18			Yes		
LVCMOS15				Yes	
LVCMOS12					Yes
PCI	Yes				
Differential Interfaces					
LVDS	Yes	Yes			
BLVDS, MLVDS, LVPECL, RSDS	Yes	Yes			
MIPI ¹	Yes	Yes			
LVTTLD	Yes				
LVCMOS33D	Yes				
LVCMOS25D		Yes			
LVCMOS18D			Yes		

1. These interfaces can be emulated with external resistors in all devices.



Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-13 lists all the available MCLK frequencies.

Table 2-13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133



Figure 2-18. PC Core Block Diagram



Table 2-14 describes the signals interfacing with the I²C cores.

 Table 2-14. PC Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I ² C core. The signal is an output if the I ² C core is in master mode. The signal is an input if the I ² C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO3L/LF device.
i2c_sda	Bi-directional	Bi-directional data line of the l^2C core. The signal is an output when data is transmitted from the l^2C core. The signal is an input when data is received into the l^2C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of l^2C ports in each MachXO3L/LF device.
i2c_irqo	Output	Interrupt request output signal of the I ² C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I ² C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.

Hardened SPI IP Core

Every MachXO3L/LF device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO3L/LF devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface



There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1293, Using Hardened Control Functions in MachXO3 Devices

Figure 2-19. SPI Core Block Diagram



Table 2-15 describes the signals interfacing with the SPI cores.

Table 2-15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	0	Master	SPI master chip-select output
spi_csn[17]	0	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	0	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Con- figuration Logic.
cfg_stdby	0	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.
cfg_wake	0	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.



Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
 - Watchdog timer
 - Clear timer on compare match
 - Fast PWM
 - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

Figure 2-20. Timer/Counter Block Diagram



Table 2-16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and NVCM/Flash spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

Password

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to TN1313, Using Password Security with MachXO3 Devices.

Dual Boot

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1292, MachXO3 Soft Error Detection Usage Guide.

Soft Error Correction

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to TN1292, MachXO3 Soft Error Detection (SED)/Correction (SEC) Usage Guide.



Programming and Erase Supply Current – C/E Devices^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ.⁴	Units
I _{CC}	Core Power Supply	LCMXO3L/LF-1300C 256 Ball Package	22.1	mA
		LCMXO3L/LF-2100C	22.1	mA
		LCMXO3L/LF-2100C 324 Ball Package	26.8	mA
		LCMXO3L/LF-4300C	26.8	mA
		LCMXO3L/LF-4300C 400 Ball Package	33.2	mA
		LCMXO3L/LF-6900C	33.2	mA
		LCMXO3L/LF-9400C	39.6	mA
		LCMXO3L/LF-640E	17.7	mA
		LCMXO3L/LF-1300E	17.7	mA
		LCMXO3L/LF-1300E 256 Ball Package	18.3	mA
		LCMXO3L/LF-2100E	18.3	mA
		LCMXO3L/LF-2100E 324 Ball Package	20.4	mA
		LCMXO3L/LF-4300E	20.4	mA
		LCMXO3L/LF-6900E	23.9	mA
		LCMXO3L/LF-9400E	28.5	mA
I _{CCIO}	Bank Power Supply ⁵ VCCIO = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1289, Power Estimation and Management for MachXO3 Devices.

2. Assumes all inputs are held at $V_{\mbox{\scriptsize CCIO}}$ or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5. $T_J = 25$ °C, power supplies at nominal voltage.

6. Per bank. $V_{CCIO} = 2.5$ V. Does not include pull-up/pull-down.



sysIO Recommended Operating Conditions

		V _{CCIO} (V)			V _{REF} (V)		
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.	
LVCMOS 3.3	3.135	3.3	3.465	—	—	—	
LVCMOS 2.5	2.375	2.5	2.625	—	—	—	
LVCMOS 1.8	1.71	1.8	1.89	—	—	—	
LVCMOS 1.5	1.425	1.5	1.575	—	—	—	
LVCMOS 1.2	1.14	1.2	1.26	—	—	—	
LVTTL	3.135	3.3	3.465	—	—	—	
LVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—	
LVDS33 ^{1, 2}	3.135	3.3	3.465	—	—	—	
LVPECL ¹	3.135	3.3	3.465	—	—	—	
BLVDS ¹	2.375	2.5	2.625	—	—	—	
MIPI ³	2.375	2.5	2.625	—	—	—	
MIPI_LP ³	1.14	1.2	1.26	—	—	—	
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4	
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05	
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05	
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9	
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9	
LVCMOS12R334	3.135	3.3	3.6	0.45	0.6	0.75	
LVCMOS12R254	2.375	2.5	2.625	0.45	0.6	0.75	
LVCMOS10R33 ⁴	3.135	3.3	3.6	0.35	0.5	0.65	
LVCMOS10R25 ^₄	2.375	2.5	2.625	0.35	0.5	0.65	

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. For the dedicated LVDS buffers.

3. Requires the addition of external resistors.

4. Supported only for inputs and BIDIs for -6 speed grade devices.



MIPI D-PHY Emulation

MachXO3L/LF devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed IOs use the LVDS25E buffer and Low Power IOs use the LVCMOS buffers. The scheme shown in Figure 3-4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3-5 is one possible solution for MIPI D-PHY Transmitter implementation.

Figure 3-4. MIPI D-PHY Input Using External Resistors



Table 3-4. MIPI DC Conditions¹

	Description	Min.	Тур.	Max.	Units
Receiver	·				
External Terminatio	n				
RT	1% external resistor with VCCIO=2.5 V		50	—	Ohms
	1% external resistor with VCCIO=3.3 V	—	50	—	Ohms
High Speed					
VCCIO	VCCIO of the Bank with LVDS Emulated input buffer	—	2.5	—	V
	VCCIO of the Bank with LVDS Emulated input buffer	—	3.3	—	V
VCMRX	Common-mode voltage HS receive mode	150	200	250	mV
VIDTH	Differential input high threshold	—	—	100	mV
VIDTL	Differential input low threshold	-100	—	—	mV
VIHHS	Single-ended input high voltage		_	300	mV
VILHS	Single-ended input low voltage	100	—	—	mV
ZID	Differential input impedance	80	100	120	Ohms



Table 3-5. MIPI D-PHY Output DC Conditions¹

	Description	Min.	Тур.	Max.	Units
Transmitter	· · ·			•	•
External Termination	on				
RL	1% external resistor with VCCIO = 2.5 V	1% external resistor with VCCIO = 2.5 V —			Ohms
	1% external resistor with VCCIO = 3.3 V	_	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	_	330	_	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	_	464	—	Ohms
High Speed	· ·				
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	_	2.5	_	V
	VCCIO of the Bank with LVDS Emulated output buffer	_	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage		—	360	V
ZOS	Single ended output impedance		50	_	Ohms
ΔZOS	Single ended output impedance mismatch		—	10	%
Low Power	· · · ·				
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	_	1.2	_	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	-50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

1. Over Recommended Operating Conditions



sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS)		1.5625	400	MHz
f _{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f _{VCO}	PLL VCO Frequency		200	800	MHz
f _{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteri	stics	•			
t _{DT}	Output Clock Duty Cycle	Without duty trim selected ³	45	55	%
t _{DT_TRIM} ⁷	Edge Duty Trim Accuracy		-75	75	%
t _{PH} ⁴	Output Phase Accuracy		-6	6	%
	Output Cleak Pariad littar	f _{OUT} > 100 MHz	—	150	ps p-p
		f _{OUT} < 100 MHz	—	0.007	UIPP
		f _{OUT} > 100 MHz	—	180	ps p-p
		f _{OUT} < 100 MHz	—	0.009	UIPP
+ 1.8		f _{PFD} > 100 MHz	—	160	ps p-p
^I OPJIT ¹	Output Clock Phase Jitter	f _{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Pariod litter (Fractional N)	f _{OUT} > 100 MHz	—	230	ps p-p
	Output Clock Period Jitter (Fractional-N)	f _{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter	f _{OUT} > 100 MHz	—	230	ps p-p
(Fractional-N)		f _{OUT} < 100 MHz	—	0.12	UIPP
t _{SPO}	Static Phase Offset	Divider ratio = integer	-120	120	ps
t _W	Output Clock Pulse Width	At 90% or 10% ³	0.9	—	ns
tLOCK ^{2, 5}	PLL Lock-in Time		—	15	ms
t _{UNLOCK}	PLL Unlock Time		—	50	ns
. 6	Innut Clask Daviad Littar	f _{PFD} ≥ 20 MHz	—	1,000	ps p-p
'IPJIT		f _{PFD} < 20 MHz	—	0.02	UIPP
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t _{STABLE} ⁵	STANDBY High to PLL Stable		—	15	ms
t _{RST}	RST/RESETM Pulse Width		1	—	ns
t _{RSTREC}	RST Recovery Time		1	—	ns
t _{RST DIV}	RESETC/D Pulse Width		10	—	ns
t _{RSTREC} DIV	RESETC/D Recovery Time		1	—	ns
t _{ROTATE-SETUP}	PHASESTEP Setup Time		10	—	ns
t _{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

Over Recommended Operating Conditions

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide for more details.

5. At minimum $\rm f_{PFD}$ As the $\rm f_{PFD}$ increases the time will decrease to approximately 60% the value listed.

6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.

7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.

8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.



	MachXO3L/LF-2100						
	WLCSP49	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	
General Purpose IO per Bank		•	•				
Bank 0	19	24	50	71	50	71	
Bank 1	0	26	52	62	52	68	
Bank 2	13	26	52	72	52	72	
Bank 3	0	7	16	22	16	24	
Bank 4	0	7	16	14	16	16	
Bank 5	6	10	20	27	20	28	
Total General Purpose Single Ended IO	38	100	206	268	206	279	
Differential IO per Bank							
Bank 0	10	12	25	36	25	36	
Bank 1	0	13	26	30	26	34	
Bank 2	6	13	26	36	26	36	
Bank 3	0	3	8	10	8	12	
Bank 4	0	3	8	6	8	8	
Bank 5	3	5	10	13	10	14	
Total General Purpose Differential IO	19	49	103	131	103	140	
Dual Function IO	25	33	33	37	33	37	
Number 7:1 or 8:1 Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18	
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18	
High-speed Differential Outputs							
Bank 0	5	7	14	18	14	18	
VCCIO Pins		•	•				
Bank 0	2	1	4	4	4	4	
Bank 1	0	1	3	4	4	4	
Bank 2	1	1	4	4	4	4	
Bank 3	0	1	2	2	1	2	
Bank 4	0	1	2	2	2	2	
Bank 5	1	1	2	2	1	2	
VCC	2	4	8	8	8	10	
GND	4	10	24	16	24	16	
NC	0	0	0	13	1	0	
Reserved for Configuration	1	1	1	1	1	1	
Total Count of Bonded Pins	49	121	256	324	256	324	



	MachXO3L/LF-9400C					
	CSFBGA256	CABGA256	CABGA400	CABGA484		
General Purpose IO per Bank	•					
Bank 0	50	50	83	95		
Bank 1	52	52	84	96		
Bank 2	52	52	84	96		
Bank 3	16	16	28	36		
Bank 4	16	16	24	24		
Bank 5	20	20	32	36		
Total General Purpose Single Ended IO	206	206	335	383		
Differential IO per Bank	·		•			
Bank 0	25	25	42	48		
Bank 1	26	26	42	48		
Bank 2	26	26	42	48		
Bank 3	8	8	14	18		
Bank 4	8	8	12	12		
Bank 5	10	10	16	18		
Total General Purpose Differential IO	103	103	168	192		
Dual Function IO	37	37	37	45		
Number 7:1 or 8:1 Gearboxes	•					
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	20	22	24		
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	20	22	24		
High-speed Differential Outputs	•					
Bank 0	20	20	21	24		
VCCIO Pins	·		•			
Bank 0	4	4	5	9		
Bank 1	3	4	5	9		
Bank 2	4	4	5	9		
Bank 3	2	1	2	3		
Bank 4	2	2	2	3		
Bank 5	2	1	2	3		
VCC	8	8	10	12		
GND	24	24	33	52		
NC	0	1	0	0		
Reserved for Configuration	1	1	1	1		
Total Count of Bonded Pins	256	256	400	484		



MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-640E-5MG121I	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-1300E-5MG1211	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-1300E-6MG1211	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-1300C-5BG256C	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-6BG256C	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-5BG256I	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-1300C-6BG256I	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-2100E-6MG1211	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND