# E · K Fattice Semiconductor Corporation - <u>LCMXO3L-1300C-6BG256I Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	206
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-1300c-6bg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the  $t_{I,OCK}$  parameter has been satisfied.

The MachXO3L/LF also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO3L/LF PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t<sub>LOCK</sub> parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.



### Figure 2-7. PLL Diagram

Table 2-4 provides signal descriptions of the PLL block.

Table 2-4	. PLL	Signal	Descriptions
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Port Name	I/O	Description	
CLKI	Ι	Input clock to PLL	
LKFB         I         Feedback clock			
PHASESEL[1:0]	Ι	I Select which output is affected by Dynamic Phase adjustment ports	
PHASEDIR I Dynamic Phase adjustment direction		Dynamic Phase adjustment direction	
PHASESTEP	Ι	Dynamic Phase step – toggle shifts VCO phase adjust by one step.	



Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE <sup>1</sup>	Output Clock Enable	Active High
RST	Reset	Active High
BE <sup>1</sup>	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	
DI	Data In	_
DO	Data Out	_
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	
FF	FIFO RAM Full Flag	_
AEF	FIFO RAM Almost Empty Flag	_
EF	FIFO RAM Empty Flag	_
RPRST	FIFO RAM Read Pointer Reset	

### Table 2-6. EBR Signal Descriptions

1. Optional signals.

2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port clock, CSR is the read port clock.

The EBR memory supports three forms of write behavior for single or dual port operation:

- 1. **Normal** Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
- 3. Read-Before-Write When new data is being written, the old contents of the address appears at the output.

### **FIFO Configuration**

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

### Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2 <sup>N</sup> -1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset



state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

### Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

### Figure 2-9. Memory Core Reset



For further information on the sysMEM EBR block, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

### EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

### Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram

Reset	
Clock	
Clock	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f<sub>MAX</sub> (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.



Figure 2-11. Group of Four Programmable I/O Cells





### PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Pin Name	I/О Туре	Description	
CE	Input	Clock Enable	
D	Input	Pin input from sysIO buffer.	
INDD	Output	Register bypassed input.	
INCK	Output	Clock input	
Q0	Output	DDR positive edge input	
Q1	Output	Registered input/DDR negative edge input	
D0	Input	Output signal from the core (SDR and DDR)	
D1	Input	Output signal from the core (DDR)	
TD	Input	Tri-state signal from the core	
Q	Output	Data output signals to sysIO Buffer	
TQ	Output	Tri-state output signals to sysIO Buffer	
SCLK	Input	System clock for input and output/tri-state blocks.	
RST	Input	Local set reset signal	

### Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

### Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.



### Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and NVCM/Flash spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

### Password

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to TN1313, Using Password Security with MachXO3 Devices.

### **Dual Boot**

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

### Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1292, MachXO3 Soft Error Detection Usage Guide.

### Soft Error Correction

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND\_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to TN1292, MachXO3 Soft Error Detection (SED)/Correction (SEC) Usage Guide.



## MachXO3 Family Data Sheet DC and Switching Characteristics

#### February 2017

#### Advance Data Sheet DS1047

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	MachXO3L/LF E (1.2 V)	MachXO3L/LF C (2.5 V/3.3 V)
Supply Voltage V <sub>CC</sub>	$\ldots$ .–0.5 V to 1.32 V $\ldots$ $\ldots$	–0.5 V to 3.75 V
Output Supply Voltage V <sub>CCIO</sub>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied <sup>4, 5</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied <sup>4</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T <sub>1</sub> )	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

4. Overshoot and undershoot of -2 V to (V<sub>IHMAX</sub> + 2) volts is permitted for a duration of <20 ns.

5. The dual function  $I^2C$  pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

### **Recommended Operating Conditions**<sup>1</sup>

Symbol	Parameter		Max.	Units
$V_{a}$ $a^{1}$	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
VCC	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V <sub>CCIO</sub> <sup>1, 2, 3</sup>	I/O Driver Supply Voltage		3.465	V
t <sub>JCOM</sub>	COM Junction Temperature Commercial Operation		85	°C
t <sub>JIND</sub>	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if V<sub>CCIO</sub> and V<sub>CC</sub> are both the same voltage, they must also be the same supply.

2. See recommended voltages by I/O standard in subsequent table.

3. V<sub>CCIO</sub> pins of unused I/O banks should be connected to the V<sub>CC</sub> power supply on boards.

### Power Supply Ramp Rates<sup>1</sup>

	iyp.	wax.	Units
t <sub>RAMP</sub> Power supply ramp rates for all power supplies. 0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

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### sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

### LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V <sub>INP</sub> , V <sub>INM</sub>	Input Voltage	V <sub>CCIO</sub> = 3.3 V	0	_	2.605	V
		V <sub>CCIO</sub> = 2.5 V	0	_	2.05	V
V <sub>THD</sub>	Differential Input Threshold		±100	_		mV
V <sub>CM</sub>	Input Common Mode Voltage	V <sub>CCIO</sub> = 3.3 V	0.05	_	2.6	V
		V <sub>CCIO</sub> = 2.5 V	0.05	_	2.0	V
I <sub>IN</sub>	Input current	Power on	_	_	±10	μA
V <sub>OH</sub>	Output high voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	_	1.375	_	V
V <sub>OL</sub>	Output low voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	0.90	1.025	_	V
V <sub>OD</sub>	Output voltage differential	(V <sub>OP</sub> - V <sub>OM</sub> ), R <sub>T</sub> = 100 Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in V <sub>OD</sub> between high and low		_	_	50	mV
V <sub>OS</sub>	Output voltage offset	(V <sub>OP</sub> - V <sub>OM</sub> )/2, R <sub>T</sub> = 100 Ohm	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in V <sub>OS</sub> between H and L		—	—	50	mV
IOSD	Output short circuit current	V <sub>OD</sub> = 0 V driver outputs shorted	_	_	24	mA

### **Over Recommended Operating Conditions**



### LVPECL

The MachXO3L/LF family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

### Figure 3-3. Differential LVPECL



### Table 3-3. LVPECL DC Conditions<sup>1</sup>

Symbol	Description	Nominal	Units
Z <sub>OUT</sub>	Output impedance	20	Ohms
R <sub>S</sub>	Driver series resistor	93	Ohms
R <sub>P</sub>	Driver parallel resistor	196	Ohms
R <sub>T</sub>	Receiver termination	100	Ohms
V <sub>OH</sub>	Output high voltage	2.05	V
V <sub>OL</sub>	Output low voltage	1.25	V
V <sub>OD</sub>	Output differential voltage	0.80	V
V <sub>CM</sub>	Output common mode voltage	1.65	V
Z <sub>BACK</sub>	Back impedance	100.5	Ohms
I <sub>DC</sub>	DC output current	12.11	mA

### **Over Recommended Operating Conditions**

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.



### MIPI D-PHY Emulation

MachXO3L/LF devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed IOs use the LVDS25E buffer and Low Power IOs use the LVCMOS buffers. The scheme shown in Figure 3-4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3-5 is one possible solution for MIPI D-PHY Transmitter implementation.

### Figure 3-4. MIPI D-PHY Input Using External Resistors



Table 3-4. MIPI DC Conditions<sup>1</sup>

	Description	Min.	Тур.	Max.	Units
Receiver	·				
External Terminatio	n				
RT	1% external resistor with VCCIO=2.5 V		50	—	Ohms
	1% external resistor with VCCIO=3.3 V	—	50	—	Ohms
High Speed					
VCCIO	VCCIO of the Bank with LVDS Emulated input buffer	—	2.5	—	V
	VCCIO of the Bank with LVDS Emulated input buffer	—	3.3	—	V
VCMRX	Common-mode voltage HS receive mode	150	200	250	mV
VIDTH	Differential input high threshold	—	—	100	mV
VIDTL	Differential input low threshold	-100	—	—	mV
VIHHS	Single-ended input high voltage		_	300	mV
VILHS	Single-ended input low voltage	100	—	—	mV
ZID	Differential input impedance	80	100	120	Ohms



### Table 3-5. MIPI D-PHY Output DC Conditions<sup>1</sup>

	Description	Min.	Тур.	Max.	Units
Transmitter	· · ·			•	
External Termination	on				
RL	1% external resistor with VCCIO = 2.5 V		50		Ohms
	1% external resistor with VCCIO = 3.3 V	—	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	_	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	_	464	—	Ohms
High Speed	· ·				
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	_	2.5	_	V
	VCCIO of the Bank with LVDS Emulated output buffer	_	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage	_	—	360	V
ZOS	Single ended output impedance		50	_	Ohms
ΔZOS	Single ended output impedance mismatch		—	10	%
Low Power	· · · ·				
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	_	1.2	_	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	-50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

1. Over Recommended Operating Conditions



### Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
MIPI	450	MHz
LVDS25	400	MHz
LVDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz



### DC and Switching Characteristics MachXO3 Family Data Sheet

			-6		-5		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
		MachXO3L/LF-1300	2.87		3.18		ns
		MachXO3L/LF-2100	2.87		3.18	—	ns
t <sub>SU_DELPLL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-4300	2.96		3.28		ns
		MachXO3L/LF-6900	3.05		3.35		ns
		MachXO3L/LF-9400	3.06		3.37		ns
		MachXO3L/LF-1300	-0.83		-0.83		ns
	Clock to Data Hold - PIO Input Register with	MachXO3L/LF-2100	-0.83		-0.83		ns
t <sub>H_DELPLL</sub>		MachXO3L/LF-4300	-0.87		-0.87		ns
		MachXO3L/LF-6900	-0.91		-0.91	—	ns
		MachXO3L/LF-9400	-0.93	—	-0.93		ns



			_	6	I _	5	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
MIPI D-PHY	Inputs with Clock and Data Centered at F	Pin Using PCLK Pin for Clo	ck Input	-			<u> </u>
GDDRX4_R	K.ECLK.Centered <sup>10, 11, 12</sup>		1	1	1	1	T
t <sub>SU</sub> <sup>15</sup>	Input Data Setup Before ECLK		0.200		0.200	—	UI
t <sub>HO</sub> <sup>15</sup>	Input Data Hold After ECLK	All MachXO3L/LE	0.200	—	0.200	—	UI
f <sub>DATA</sub> <sup>14</sup>	MIPI D-PHY Input Data Speed	devices, bottom side only		900	—	900	Mbps
f <sub>DDRX4</sub> <sup>14</sup>	MIPI D-PHY ECLK Frequency		—	450	—	450	MHz
f <sub>SCLK</sub> <sup>14</sup>	SCLK Frequency		_	112.5	-	112.5	MHz
Generic DD	R Outputs with Clock and Data Aligned at	Pin Using PCLK Pin for Clo	ck Input	– GDDF	RX1_TX.	SCLK.A	ligned <sup>8</sup>
t <sub>DIA</sub>	Output Data Invalid After CLK Output		—	0.520	—	0.550	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	All MachXO3L/LF		0.520	—	0.550	ns
f <sub>DATA</sub>	DDRX1 Output Data Speed	all sides		300	—	250	Mbps
f <sub>DDRX1</sub>	DDRX1 SCLK frequency			150	—	125	MHz
Generic DDF	Outputs with Clock and Data Centered at	Pin Using PCLK Pin for Clo	ck Input	– GDDR	X1_TX.9	SCLK.Ce	entered <sup>8</sup>
t <sub>DVB</sub>	Output Data Valid Before CLK Output		1.210		1.510	—	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output	All MachXO3L/LF	1.210		1.510	—	ns
f <sub>DATA</sub>	DDRX1 Output Data Speed	devices,	_	300	—	250	Mbps
f <sub>DDRX1</sub>	DDRX1 SCLK Frequency (minimum limited by PLL)	— all sides	_	150	_	125	MHz
Generic DDF	X2 Outputs with Clock and Data Aligned a	at Pin Using PCLK Pin for Clo	ock Inpu	t – GDD	RX2_TX	ECLK.A	
t <sub>DIA</sub>	Output Data Invalid After CLK Output		<u> </u>	0.200	—	0.215	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	_		0.200	_	0.215	ns
f <sub>DATA</sub>	DDRX2 Serial Output Data Speed	MachXO3L/LF devices,		664	_	554	Mbps
foogy2	DDRX2 ECLK frequency	top side only		332	_	277	MHz
fsci k	SCLK Frequency			166	_	139	MHz
Generic DD	RX2 Outputs with Clock and Data Center	ed at Pin Using PCLK Pin fo	or Clock	Input –			
GDDRX2_T	(.ECLK.Centered <sup>8, 9</sup>	0		•			
t <sub>DVB</sub>	Output Data Valid Before CLK Output		0.535	—	0.670	—	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output		0.535	—	0.670	—	ns
f <sub>DATA</sub>	DDRX2 Serial Output Data Speed	MachXO3L/LF devices,		664	—	554	Mbps
f <sub>DDRX2</sub>	DDRX2 ECLK Frequency (minimum limited by PLL)	top side only	_	332	—	277	MHz
f <sub>SCLK</sub>	SCLK Frequency			166	—	139	MHz
Generic DD GDDRX4_TX	RX4 Outputs with Clock and Data Aligned	d at Pin Using PCLK Pin for	Clock I	nput –			
t <sub>DIA</sub>	Output Data Invalid After CLK Output		_	0.200	_	0.215	ns
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	7		0.200	_	0.215	ns
f <sub>DATA</sub>	DDRX4 Serial Output Data Speed	MachXO3L/LF devices,	_	800	_	630	Mbps
f <sub>DDBX4</sub>	DDRX4 ECLK Frequency		<u> </u>	400	_	315	MHz
fscik	SCLK Frequency	{ }	<u> </u>	100		79	MHz



### Figure 3-6. Receiver GDDR71\_RX. Waveforms



Figure 3-7. Transmitter GDDR71\_TX. Waveforms





### I<sup>2</sup>C Port Timing Specifications<sup>1, 2</sup>

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCL clock frequency		400	kHz

1. MachXO3L/LF supports the following modes:

• Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)

• Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)

2. Refer to the  $I^2C$  specification for timing requirements.

### SPI Port Timing Specifications<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCK clock frequency		45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

### **Switching Test Conditions**

Figure 3-9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

### Figure 3-9. Output Test Load, LVTTL and LVCMOS Standards



Table 3-6. Test Fixture Required Components	, Non-Terminated Interfaces
---	-----------------------------

Test Condition	R1	CL	Timing Ref.	VT
			LVTTL, LVCMOS 3.3 = 1.5 V	_
	×	0pF	LVCMOS 2.5 = $V_{CCIO}/2$	_
LVTTL and LVCMOS settings (L -> H, H -> L)			LVCMOS 1.8 = $V_{CCIO}/2$	
			LVCMOS 1.5 = $V_{CCIO}/2$	_
			LVCMOS 1.2 = $V_{CCIO}/2$	_
LVTTL and LVCMOS 3.3 (Z -> H)	-		1.5	V <sub>OL</sub>
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V <sub>OH</sub>
Other LVCMOS (Z -> H)	188	0nE	V <sub>CCIO</sub> /2	V <sub>OL</sub>
Other LVCMOS (Z -> L)	100	орі	V <sub>CCIO</sub> /2	V <sub>OH</sub>
LVTTL + LVCMOS (H -> Z)			V <sub>OH</sub> - 0.15	V <sub>OL</sub>
LVTTL + LVCMOS (L -> Z)	1		V <sub>OL</sub> - 0.15	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.



# MachXO3 Family Data Sheet Pinout Information

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### **Signal Descriptions**

Signal Name	I/O	Descriptions		
General Purpose				
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).		
		[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.		
		[A/B/C/D] indicates the PIO within the group to which the pad is connected.		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.		
		During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.		
NC	—	No connect.		
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.		
VCC	_	$V_{CC}$ – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.		
VCCIOx	_	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.		
PLL and Clock Functi	ons (Us	ed as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	_	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.		
[LOC]_GPLL[T, C]_FB	_	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.		
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.		
Test and Programmin	<b>g</b> (Dual f	function pins used for test access port and during sysCONFIG™)		
TMS	Ι	Test Mode Select input pin, used to control the 1149.1 state machine.		
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.		
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.		
TDO	0	Output pin – Test Data output pin used to shift data out of the device using 1149.1.		
		Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:		
JTAGENB	I	If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.		
		If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.		
		For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.		

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			MachXO3	L/LF-2100		
	WLCSP49	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324
General Purpose IO per Bank		•	•			
Bank 0	19	24	50	71	50	71
Bank 1	0	26	52	62	52	68
Bank 2	13	26	52	72	52	72
Bank 3	0	7	16	22	16	24
Bank 4	0	7	16	14	16	16
Bank 5	6	10	20	27	20	28
Total General Purpose Single Ended IO	38	100	206	268	206	279
Differential IO per Bank						
Bank 0	10	12	25	36	25	36
Bank 1	0	13	26	30	26	34
Bank 2	6	13	26	36	26	36
Bank 3	0	3	8	10	8	12
Bank 4	0	3	8	6	8	8
Bank 5	3	5	10	13	10	14
Total General Purpose Differential IO	19	49	103	131	103	140
Dual Function IO	25	33	33	37	33	37
Number 7:1 or 8:1 Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18
High-speed Differential Outputs						
Bank 0	5	7	14	18	14	18
VCCIO Pins		•	•			
Bank 0	2	1	4	4	4	4
Bank 1	0	1	3	4	4	4
Bank 2	1	1	4	4	4	4
Bank 3	0	1	2	2	1	2
Bank 4	0	1	2	2	2	2
Bank 5	1	1	2	2	1	2
VCC	2	4	8	8	8	10
GND	4	10	24	16	24	16
NC	0	0	0	13	1	0
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	49	121	256	324	256	324



	MachXO3L/LF-4300								
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400		
General Purpose IO per Bank									
Bank 0	29	24	50	71	50	71	83		
Bank 1	0	26	52	62	52	68	84		
Bank 2	20	26	52	72	52	72	84		
Bank 3	7	7	16	22	16	24	28		
Bank 4	0	7	16	14	16	16	24		
Bank 5	7	10	20	27	20	28	32		
Total General Purpose Single Ended IO	63	100	206	268	206	279	335		
Differential IO per Bank									
Bank 0	15	12	25	36	25	36	42		
Bank 1	0	13	26	30	26	34	42		
Bank 2	10	13	26	36	26	36	42		
Bank 3	3	3	8	10	8	12	14		
Bank 4	0	3	8	6	8	8	12		
Bank 5	3	5	10	13	10	14	16		
Total General Purpose Differential IO	31	49	103	131	103	140	168		
Dual Function IO	25	37	37	37	37	37	37		
Number 7:1 or 8:1 Gearboxes									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21		
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21		
High-speed Differential Outputs									
Bank 0	10	7	18	18	18	18	21		
VCCIO Pins									
Bank 0	3	1	4	4	4	4	5		
Bank 1	0	1	3	4	4	4	5		
Bank 2	2	1	4	4	4	4	5		
Bank 3	1	1	2	2	1	2	2		
Bank 4	0	1	2	2	2	2	2		
Bank 5	1	1	2	2	1	2	2		
VCC	4	4	8	8	8	10	10		
GND	6	10	24	16	24	16	33		
NC	0	0	0	13	1	0	0		
Reserved for Configuration	1	1	1	1	1	1	1		
Total Count of Bonded Pins	81	121	256	324	256	324	400		



# MachXO3 Family Data Sheet Revision History

### February 2017

Advance Data Sheet DS1047

Date	Version	Section	Change Summary
February 2017	1.8	Architecture	Updated Supported Standards section. Corrected "MDVS" to "MLDVS" in Table 2-11, Supported Input Standards.
		DC and Switching Characteristics	Updated ESD Performance section. Added reference to the MachXO2 Product Family Qualification Summary document.
			Updated Static Supply Current – C/E Devices section. Added footnote 7.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. — Populated values for MachXO3L/LF-9400. — Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, corrected "t <sub>DVB</sub> " to "t <sub>DIB</sub> " and "t <sub>DVA</sub> " to "t <sub>DIA</sub> " and revised their descriptions. — Added Figure 3-6, Receiver GDDR71_RX Waveforms and Figure 3-7, Transmitter GDDR71_TX Waveforms.
		Pinout Information	Updated the Pin Information Summary section. Added MachXO3L/LF- 9600C packages.
May 2016	1.7	DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Modified I/O Tri-state Volt- age Applied and Dedicated Input Voltage Applied footnotes.
			Updated sysIO Recommended Operating Conditions section. — Added standards. — Added V <sub>REF</sub> (V) — Added footnote 4.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Added I/O standards.
		Ordering Information	Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.

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