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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	121-VFBGA, CSPBGA
Supplier Device Package	121-CSFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-1300e-5mg121i

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# MachXO3 Family Data Sheet Introduction

#### January 2016

#### **Features**

#### Solutions

- Smallest footprint, lowest power, high data throughput bridging solutions for mobile applications
- Optimized footprint, logic density, IO count, IO performance devices for IO management and logic applications
- High IO/logic, lowest cost/IO, high IO devices for IO expansion applications

#### ■ Flexible Architecture

- Logic Density ranging from 640 to 9.4K LUT4
- High IO to LUT ratio with up to 384 IO pins

#### Advanced Packaging

- 0.4 mm pitch: 1K to 4K densities in very small footprint WLCSP (2.5 mm x 2.5 mm to 3.8 mm x 3.8 mm) with 28 to 63 IOs
- 0.5 mm pitch: 640 to 6.9K LUT densities in 6 mm x 6 mm to 10 mm x 10 mm BGA packages with up to 281 IOs
- 0.8 mm pitch: 1K to 9.4K densities with up to 384 IOs in BGA packages

#### Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRx2, DDRx4

#### High Performance, Flexible I/O Buffer

- Programmable sysIO<sup>™</sup> buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - LVDS, Bus-LVDS, MLVDS, LVPECL
  - MIPI D-PHY Emulated
  - Schmitt trigger inputs, up to 0.5 V hysteresis
- Ideal for IO bridging applications
- I/Os support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

#### ■ Flexible On-Chip Clocking

- · Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
  - Wide input frequency range (7 MHz to 400 MHz)
- Non-volatile, Multi-time Programmable
  - Instant-on
    - Powers up in microseconds
    - · Optional dual boot with external SPI memory
    - Single-chip, secure solution
    - Programmable through JTAG, SPI or I<sup>2</sup>C
    - MachXO3L includes multi-time programmable NVCM
    - MachXO3LF infinitely reconfigurable Flash

       Supports background programming of non-volatile memory

#### TransFR Reconfiguration

In-field logic update while IO holds the system state

#### Enhanced System Level Support

- On-chip hardened functions: SPI, I<sup>2</sup>C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

#### Applications

- Consumer Electronics
- Compute and Storage
- Wireless Communications
- Industrial Control Systems
- Automotive System

#### Low Cost Migration Path

- Migration from the Flash based MachXO3LF to the NVCM based MachXO3L
- · Pin compatible and equivalent timing

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#### Advance Data Sheet DS1047



## **PFU Blocks**

The core of the MachXO3L/LF device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

#### Figure 2-3. PFU Block Diagram



#### Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

#### Table 2-1. Resources and Modes Available per Slice

	PFU Block			
Slice	Resources	Modes		
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM		

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.



Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE <sup>1</sup>	Output Clock Enable	Active High
RST	Reset	Active High
BE <sup>1</sup>	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	
DI	Data In	_
DO	Data Out	_
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	
FF	FIFO RAM Full Flag	_
AEF	FIFO RAM Almost Empty Flag	_
EF	FIFO RAM Empty Flag	_
RPRST	FIFO RAM Read Pointer Reset	_

#### Table 2-6. EBR Signal Descriptions

1. Optional signals.

2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port clock, CSR is the read port clock.

The EBR memory supports three forms of write behavior for single or dual port operation:

- 1. **Normal** Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
- 3. Read-Before-Write When new data is being written, the old contents of the address appears at the output.

#### **FIFO Configuration**

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

#### Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2 <sup>N</sup> -1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset



Figure 2-11. Group of Four Programmable I/O Cells





#### Figure 2-13. Input Gearbox



More information on the input gearbox is available in TN1281, Implementing High-Speed Interfaces with MachXO3 Devices.



## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO3L/LF devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) input buffers are powered using I/O supply voltage ( $V_{CCIO}$ ). Each sysIO bank has its own  $V_{CCIO}$ .

MachXO3L/LF devices contain three types of sysIO buffer pairs.

#### 1. Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential input buffers.

#### 2. Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after  $V_{CC}$  and  $V_{CCIO}$  are at valid operating levels and the device has been configured.

#### 3. Top sysIO Buffer Pairs

The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two singleended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver.

#### Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$  and  $V_{CCIO0}$  have reached  $V_{PORUP}$  level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pulldown to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to  $V_{CCIO}$  as the default functionality). The I/O pins will maintain the blank configuration until  $V_{CC}$  and  $V_{CCIO}$  (for I/O banks containing configuration I/Os) have reached  $V_{PORUP}$  levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

There are various ways a user can ensure that there are no spurious signals on critical outputs as the device powers up. These are discussed in more detail in TN1280, MachXO3 sysIO Usage Guide.

#### **Supported Standards**

The MachXO3L/LF sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO3L/LF devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO3L/LF devices. PCI support is provided in the bottom bank of the MachXO3L/LF devices. Table 2-11 summarizes the I/O characteristics of the MachXO3L/LF PLDs.



#### Table 2-12. Supported Output Standards

Output Standard	V <sub>CCIO</sub> (Typ.)			
Single-Ended Interfaces				
LVTTL	3.3			
LVCMOS33	3.3			
LVCMOS25	2.5			
LVCMOS18	1.8			
LVCMOS15	1.5			
LVCMOS12	1.2			
LVCMOS33, Open Drain	_			
LVCMOS25, Open Drain	_			
LVCMOS18, Open Drain	—			
LVCMOS15, Open Drain	_			
LVCMOS12, Open Drain	_			
PCI33	3.3			
Differential Interfaces				
LVDS <sup>1</sup>	2.5, 3.3			
BLVDS, MLVDS, RSDS 1	2.5			
LVPECL <sup>1</sup>	3.3			
MIPI <sup>1</sup>	2.5			
LVTTLD	3.3			
LVCMOS33D	3.3			
LVCMOS25D	2.5			
LVCMOS18D	1.8			

1. These interfaces can be emulated with external resistors in all devices.

#### sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO3L/LF-1300 in the 256 Ball packages and the MachXO3L/LF-2100 and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO3L/LF-1300 and lower density devices have four banks (one bank per side). Figures 2-15 and 2-16 show the sysIO banks and their associated supplies for all devices.



## **Embedded Hardened IP Functions**

All MachXO3L/LF devices provide embedded hardened functions such as SPI, I<sup>2</sup>C and Timer/Counter. MachXO3LF devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-17.

#### Figure 2-17. Embedded Function Block Interface



#### Hardened I<sup>2</sup>C IP Core

Every MachXO3L/LF device contains two  $I^2C$  IP cores. These are the primary and secondary  $I^2C$  IP cores. Either of the two cores can be configured either as an  $I^2C$  master or as an  $I^2C$  slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the  $I^2C$  bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an  $I^2C$  Master. The  $I^2C$  cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface



#### Figure 2-18. PC Core Block Diagram



Table 2-14 describes the signals interfacing with the I<sup>2</sup>C cores.

 Table 2-14. PC Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I <sup>2</sup> C core. The signal is an output if the I <sup>2</sup> C core is in master mode. The signal is an input if the I <sup>2</sup> C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I <sup>2</sup> C ports in each MachXO3L/LF device.
i2c_sda	Bi-directional	Bi-directional data line of the $l^2C$ core. The signal is an output when data is transmitted from the $l^2C$ core. The signal is an input when data is received into the $l^2C$ core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of $l^2C$ ports in each MachXO3L/LF device.
i2c_irqo	Output	Interrupt request output signal of the I <sup>2</sup> C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I <sup>2</sup> C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, $I^2C$ Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, $I^2C$ Tab.

#### Hardened SPI IP Core

Every MachXO3L/LF device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO3L/LF devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface



## TraceID

Each MachXO3L/LF device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I<sup>2</sup>C, or JTAG interfaces.

## **Density Shifting**

The MachXO3L/LF family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO3 migration files.



## **DC Electrical Characteristics**

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
		Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)			+175	μΑ
Iս., հա <sup>1, 4</sup>	Input or I/O Leakage	Clamp OFF and $V_{IN} = V_{CCIO}$	-10	—	10	μΑ
		Clamp OFF and V <sub>CCIO</sub> - 0.97 V < V <sub>IN</sub> < V <sub>CCIO</sub>	-175	_	—	μA
		Clamp OFF and 0 V < $V_{IN}$ < $V_{CCIO}$ - 0.97 V	_		10	μΑ
		Clamp OFF and V <sub>IN</sub> = GND	_		10	μΑ
		Clamp ON and 0 V < $V_{IN}$ < $V_{CCIO}$			10	μΑ
I <sub>PU</sub>	I/O Active Pull-up Current	0 < V <sub>IN</sub> < 0.7 V <sub>CCIO</sub>	-30		-309	μΑ
I <sub>PD</sub>	I/O Active Pull-down Current	V <sub>IL</sub> (MAX) < V <sub>IN</sub> < V <sub>CCIO</sub>	30	—	305	μA
I <sub>BHLS</sub>	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I <sub>BHHS</sub>	Bus Hold High sustaining current	V <sub>IN</sub> = 0.7V <sub>CCIO</sub>	-30	_	_	μΑ
I <sub>BHLO</sub>	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	_	—	305	μΑ
І <sub>внно</sub>	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	_	_	-309	μΑ
V <sub>BHT</sub> <sup>3</sup>	Bus Hold Trip Points			—	V <sub>IH</sub> (MIN)	V
C1	I/O Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)$	3	5	9	pf
C2	Dedicated Input Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)$	3	5.5	7	pf
		V <sub>CCIO</sub> = 3.3 V, Hysteresis = Large	_	450	—	mV
		V <sub>CCIO</sub> = 2.5 V, Hysteresis = Large		250	—	mV
V <sub>HYST</sub>		V <sub>CCIO</sub> = 1.8 V, Hysteresis = Large		125	—	mV
	Hysteresis for Schmitt	V <sub>CCIO</sub> = 1.5 V, Hysteresis = Large	_	100	—	mV
	Trigger Inputs⁵	V <sub>CCIO</sub> = 3.3 V, Hysteresis = Small	_	250	—	mV
		V <sub>CCIO</sub> = 2.5 V, Hysteresis = Small	_	150	—	mV
		V <sub>CCIO</sub> = 1.8 V, Hysteresis = Small	—	60	—	mV
		V <sub>CCIO</sub> = 1.5 V, Hysteresis = Small	_	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T<sub>A</sub> 25 °C, f = 1.0 MHz.

3. Please refer to V<sub>IL</sub> and V<sub>IH</sub> in the sysIO Single-Ended DC Electrical Characteristics table of this document.

 When V<sub>IH</sub> is higher than V<sub>CCIO</sub>, a transient current typically of 30 ns in duration or less with a peak current of 6mA can occur on the high-tolow transition. For true LVDS output pins in MachXO3L/LF devices, V<sub>IH</sub> must be less than or equal to V<sub>CCIO</sub>.

5. With bus keeper circuit turned on. For more details, refer to TN1280, MachXO3 sysIO Usage Guide.



# Programming and Erase Supply Current – C/E Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ.⁴	Units
I <sub>CC</sub>	Core Power Supply	LCMXO3L/LF-1300C 256 Ball Package	22.1	mA
		LCMXO3L/LF-2100C	22.1	mA
		LCMXO3L/LF-2100C 324 Ball Package	26.8	mA
		LCMXO3L/LF-4300C	26.8	mA
		LCMXO3L/LF-4300C 400 Ball Package	33.2	mA
		LCMXO3L/LF-6900C	33.2	mA
		LCMXO3L/LF-9400C	39.6	mA
		LCMXO3L/LF-640E	17.7	mA
		LCMXO3L/LF-1300E	17.7	mA
		LCMXO3L/LF-1300E 256 Ball Package	18.3	mA
		LCMXO3L/LF-2100E	18.3	mA
		LCMXO3L/LF-2100E 324 Ball Package	20.4	mA
		LCMXO3L/LF-4300E	20.4	mA
		LCMXO3L/LF-6900E	23.9	mA
		LCMXO3L/LF-9400E	28.5	mA
I <sub>CCIO</sub>	Bank Power Supply <sup>5</sup> VCCIO = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1289, Power Estimation and Management for MachXO3 Devices.

2. Assumes all inputs are held at  $V_{\mbox{\scriptsize CCIO}}$  or GND and all outputs are tri-stated.

3. Typical user pattern.

4. JTAG programming is at 25 MHz.

5.  $T_J = 25$  °C, power supplies at nominal voltage.

6. Per bank.  $V_{CCIO} = 2.5$  V. Does not include pull-up/pull-down.



# sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

### LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V V	Input Voltage	V <sub>CCIO</sub> = 3.3 V	0	_	2.605	V
VINP VINM		V <sub>CCIO</sub> = 2.5 V	0	_	2.05	V
V <sub>THD</sub>	Differential Input Threshold		±100	_		mV
V	Input Common Mode Voltage	V <sub>CCIO</sub> = 3.3 V	0.05	_	2.6	V
VCM	Input Common Mode Voltage	V <sub>CCIO</sub> = 2.5 V	0.05	_	2.0	V
I <sub>IN</sub>	Input current	Power on	_	_	±10	μA
V <sub>OH</sub>	Output high voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	_	1.375	_	V
V <sub>OL</sub>	Output low voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	0.90	1.025	_	V
V <sub>OD</sub>	Output voltage differential	(V <sub>OP</sub> - V <sub>OM</sub> ), R <sub>T</sub> = 100 Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in V <sub>OD</sub> between high and low		_	_	50	mV
V <sub>OS</sub>	Output voltage offset	(V <sub>OP</sub> - V <sub>OM</sub> )/2, R <sub>T</sub> = 100 Ohm	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in V <sub>OS</sub> between H and L		—	—	50	mV
IOSD	Output short circuit current	V <sub>OD</sub> = 0 V driver outputs shorted	_	_	24	mA

#### **Over Recommended Operating Conditions**



## Typical Building Block Function Performance – C/E Devices<sup>1</sup>

#### Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

#### **Register-to-Register Performance**

Function	–6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

 The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

## **Derating Logic Timing**

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.



			-6		_5			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units	
MIPI D-PHY	Inputs with Clock and Data Centered at F	Pin Using PCLK Pin for Clo	ck Input	-			<u> </u>	
GDDRX4_R	K.ECLK.Centered <sup>10, 11, 12</sup>		1	1	1	1	T	
t <sub>SU</sub> <sup>15</sup>	Input Data Setup Before ECLK		0.200		0.200	—	UI	
t <sub>HO</sub> <sup>15</sup>	Input Data Hold After ECLK	All MachXO3L/LE	0.200	—	0.200	—	UI	
f <sub>DATA</sub> <sup>14</sup>	MIPI D-PHY Input Data Speed	devices, bottom side only		900	—	900	Mbps	
f <sub>DDRX4</sub> <sup>14</sup>	MIPI D-PHY ECLK Frequency		—	450	—	450	MHz	
f <sub>SCLK</sub> <sup>14</sup>	SCLK Frequency		_	112.5	-	112.5	MHz	
Generic DD	R Outputs with Clock and Data Aligned at	Pin Using PCLK Pin for Clo	ck Input	– GDDF	RX1_TX.	SCLK.A	ligned <sup>8</sup>	
t <sub>DIA</sub>	Output Data Invalid After CLK Output		—	0.520	—	0.550	ns	
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	All MachXO3L/LF		0.520	—	0.550	ns	
f <sub>DATA</sub>	DDRX1 Output Data Speed	all sides		300	—	250	Mbps	
f <sub>DDRX1</sub>	DDRX1 SCLK frequency			150	—	125	MHz	
Generic DDF	Outputs with Clock and Data Centered at	Pin Using PCLK Pin for Clo	ck Input	– GDDR	X1_TX.9	SCLK.Ce	entered <sup>8</sup>	
t <sub>DVB</sub>	Output Data Valid Before CLK Output		1.210		1.510	—	ns	
t <sub>DVA</sub>	Output Data Valid After CLK Output	All MachXO3L/LF	1.210		1.510	—	ns	
f <sub>DATA</sub>	DDRX1 Output Data Speed	devices,	_	300	—	250	Mbps	
f <sub>DDRX1</sub>	DDRX1 SCLK Frequency (minimum limited by PLL)	— all sides	_	150	_	125	MHz	
Generic DDF	X2 Outputs with Clock and Data Aligned a	at Pin Using PCLK Pin for Clo	ock Inpu	t – GDD	RX2_TX	ECLK.A		
t <sub>DIA</sub>	Output Data Invalid After CLK Output		<u> </u>	0.200	—	0.215	ns	
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	_		0.200	_	0.215	ns	
f <sub>DATA</sub>	DDRX2 Serial Output Data Speed	MachXO3L/LF devices,		664	_	554	Mbps	
foogy2	DDRX2 ECLK frequency	top side only		332	_	277	MHz	
fsci k	SCLK Frequency			166	_	139	MHz	
Generic DD	RX2 Outputs with Clock and Data Center	ed at Pin Using PCLK Pin fo	or Clock	Input –			<u> </u>	
GDDRX2_T	K.ECLK.Centered <sup>8,9</sup>	0		•				
t <sub>DVB</sub>	Output Data Valid Before CLK Output		0.535	—	0.670	—	ns	
t <sub>DVA</sub>	Output Data Valid After CLK Output		0.535	—	0.670	—	ns	
f <sub>DATA</sub>	DDRX2 Serial Output Data Speed	MachXO3L/LF devices,		664	—	554	Mbps	
f <sub>DDRX2</sub>	DDRX2 ECLK Frequency (minimum limited by PLL)	top side only	_	332	—	277	MHz	
f <sub>SCLK</sub>	SCLK Frequency			166	—	139	MHz	
Generic DD GDDRX4_TX	RX4 Outputs with Clock and Data Aligned	d at Pin Using PCLK Pin for	Clock I	nput –				
t <sub>DIA</sub>	Output Data Invalid After CLK Output		_	0.200	—	0.215	ns	
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	7		0.200	_	0.215	ns	
f <sub>DATA</sub>	DDRX4 Serial Output Data Speed	MachXO3L/LF devices,	_	800	_	630	Mbps	
f <sub>DDBX4</sub>	DDRX4 ECLK Frequency		<b> </b>	400	_	315	MHz	
fscik	SCLK Frequency		<u> </u>	100		79	MHz	



# I<sup>2</sup>C Port Timing Specifications<sup>1, 2</sup>

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCL clock frequency		400	kHz

1. MachXO3L/LF supports the following modes:

• Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)

• Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)

2. Refer to the  $I^2C$  specification for timing requirements.

# SPI Port Timing Specifications<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCK clock frequency		45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

## **Switching Test Conditions**

Figure 3-9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

#### Figure 3-9. Output Test Load, LVTTL and LVCMOS Standards



Table 3-6. Test Fixture Required Components	, Non-Terminated Interfaces
---------------------------------------------	-----------------------------

Test Condition	R1	CL	Timing Ref.	VT
			LVTTL, LVCMOS 3.3 = 1.5 V	_
			LVCMOS 2.5 = $V_{CCIO}/2$	_
LVTTL and LVCMOS settings (L -> H, H -> L)	$\infty$	0pF	LVCMOS 1.8 = $V_{CCIO}/2$	
			LVCMOS 1.5 = $V_{CCIO}/2$	_
			LVCMOS 1.2 = $V_{CCIO}/2$	_
LVTTL and LVCMOS 3.3 (Z -> H)			1.5	V <sub>OL</sub>
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V <sub>OH</sub>
Other LVCMOS (Z -> H)	188	0nE	V <sub>CCIO</sub> /2	V <sub>OL</sub>
Other LVCMOS (Z -> L) LVTTL + LVCMOS (H -> Z)	100	орі	V <sub>CCIO</sub> /2	V <sub>OH</sub>
			V <sub>OH</sub> - 0.15	V <sub>OL</sub>
LVTTL + LVCMOS (L -> Z)			V <sub>OL</sub> - 0.15	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.



	MachXO3L/LF-4300							
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400	
General Purpose IO per Bank								
Bank 0	29	24	50	71	50	71	83	
Bank 1	0	26	52	62	52	68	84	
Bank 2	20	26	52	72	52	72	84	
Bank 3	7	7	16	22	16	24	28	
Bank 4	0	7	16	14	16	16	24	
Bank 5	7	10	20	27	20	28	32	
Total General Purpose Single Ended IO	63	100	206	268	206	279	335	
Differential IO per Bank								
Bank 0	15	12	25	36	25	36	42	
Bank 1	0	13	26	30	26	34	42	
Bank 2	10	13	26	36	26	36	42	
Bank 3	3	3	8	10	8	12	14	
Bank 4	0	3	8	6	8	8	12	
Bank 5	3	5	10	13	10	14	16	
Total General Purpose Differential IO	31	49	103	131	103	140	168	
Dual Function IO	25	37	37	37	37	37	37	
Number 7:1 or 8:1 Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21	
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21	
High-speed Differential Outputs								
Bank 0	10	7	18	18	18	18	21	
VCCIO Pins								
Bank 0	3	1	4	4	4	4	5	
Bank 1	0	1	3	4	4	4	5	
Bank 2	2	1	4	4	4	4	5	
Bank 3	1	1	2	2	1	2	2	
Bank 4	0	1	2	2	2	2	2	
Bank 5	1	1	2	2	1	2	2	
VCC	4	4	8	8	8	10	10	
GND	6	10	24	16	24	16	33	
NC	0	0	0	13	1	0	0	
Reserved for Configuration	1	1	1	1	1	1	1	
Total Count of Bonded Pins	81	121	256	324	256	324	400	



Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
				1		
Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND



# MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-5MG1211	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND
Part Number	l IITe	Supply Voltage	Sneed	Package	abea I	Tomn

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-5MG121I	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-6MG121I	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300C-5BG256C	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-6BG256C	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-5BG256I	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-1300C-6BG256I	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-6MG121I	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND



Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	СОМ
LCMXO3LF-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	СОМ
LCMXO3LF-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	СОМ
LCMXO3LF-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND
	T		<b></b>	1	1	1
Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3LF-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND