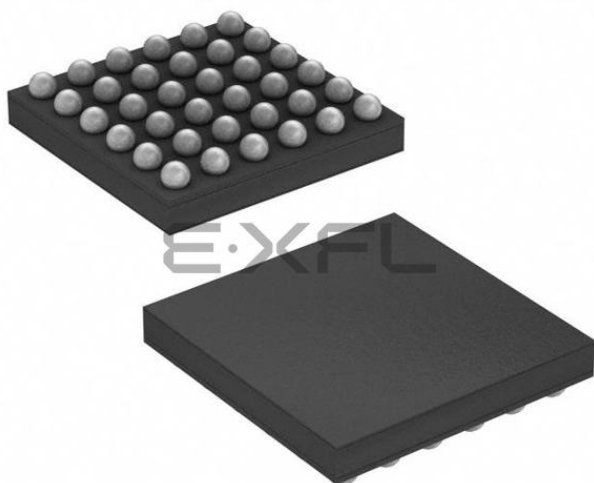




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

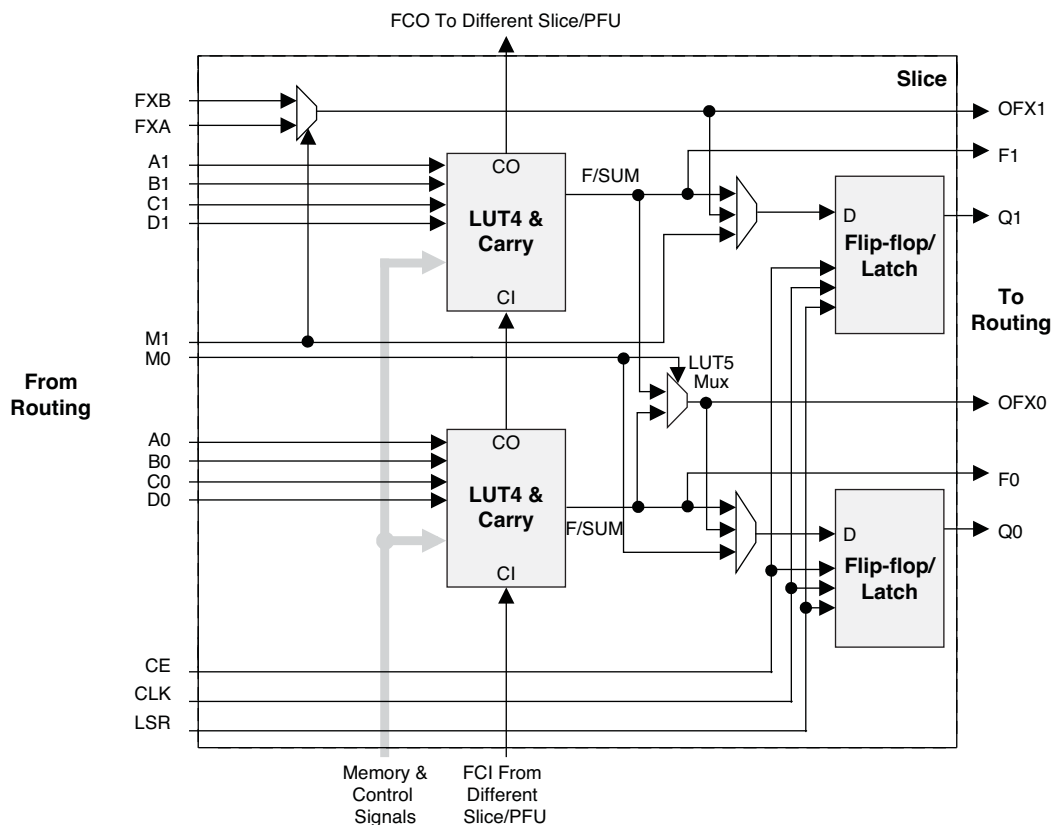
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	28
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP (2.54x2.59)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-1300e-5uwg36itr50

Figure 2-4. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3L/LF devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO3L/LF devices, please see TN1290, [Memory Usage Guide for MachXO3 Devices](#).

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1290, [Memory Usage Guide for MachXO3 Devices](#).

Routing

There are many resources provided in the MachXO3L/LF devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO3L/LF device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO3L/LF architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO3L/LF devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3L/LF devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3L/LF External Switching Characteristics table.

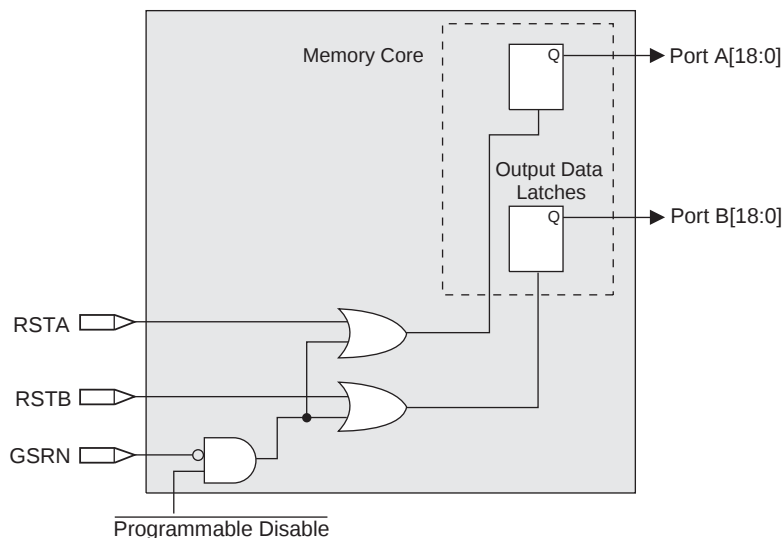
Primary clock signals for the MachXO3L/LF-1300 and larger devices are generated from eight 27:1 muxes. The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sys-CLOCK PLL outputs.

state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-9. Memory Core Reset

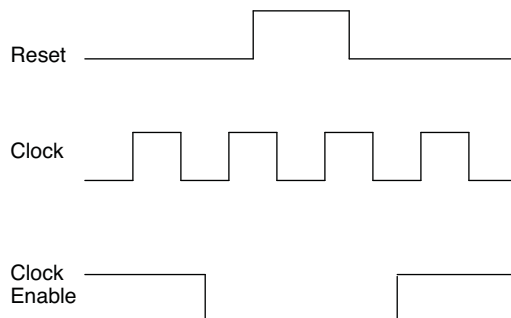


For further information on the sysMEM EBR block, please refer to TN1290, [Memory Usage Guide for MachXO3 Devices](#).

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/t_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.



MachXO3 Family Data Sheet

DC and Switching Characteristics

February 2017

Advance Data Sheet DS1047

Absolute Maximum Ratings^{1, 2, 3}

	MachXO3L/LF E (1.2 V)	MachXO3L/LF C (2.5 V/3.3 V)
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied ^{4, 5}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied ⁴	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.
5. The dual function I²C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V_{CC}^1	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
$V_{CCIO}^{1, 2, 3}$	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates¹

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

Power-On-Reset Voltage Levels^{1, 2, 3, 4, 5}

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for C devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Hot Socketing Specifications^{1, 2, 3}

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	μA

1. Insensitive to sequence of V_{CC} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO} .
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .

ESD Performance

Please refer to the [MachXO2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,4}$	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH} (MAX)$	—	—	+175	μA
		Clamp OFF and $V_{IN} = V_{CCIO}$	-10	—	10	μA
		Clamp OFF and $V_{CCIO} - 0.97 V < V_{IN} < V_{CCIO}$	-175	—	—	μA
		Clamp OFF and $0 V < V_{IN} < V_{CCIO} - 0.97 V$	—	—	10	μA
		Clamp OFF and $V_{IN} = GND$	—	—	10	μA
		Clamp ON and $0 V < V_{IN} < V_{CCIO}$	—	—	10	μA
I_{PU}	I/O Active Pull-up Current	$0 < V_{IN} < 0.7 V_{CCIO}$	-30	—	-309	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) < V_{IN} < V_{CCIO}$	30	—	305	μA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	305	μA
I_{BHHO}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-309	μA
V_{BHT}^3	Bus Hold Trip Points		$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{IH} (MAX)$	3	5	9	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 \text{ to } V_{IH} (MAX)$	3	5.5	7	pf
V_{HYST}	Hysteresis for Schmitt Trigger Inputs ⁵	$V_{CCIO} = 3.3 V, \text{Hysteresis} = \text{Large}$	—	450	—	mV
		$V_{CCIO} = 2.5 V, \text{Hysteresis} = \text{Large}$	—	250	—	mV
		$V_{CCIO} = 1.8 V, \text{Hysteresis} = \text{Large}$	—	125	—	mV
		$V_{CCIO} = 1.5 V, \text{Hysteresis} = \text{Large}$	—	100	—	mV
		$V_{CCIO} = 3.3 V, \text{Hysteresis} = \text{Small}$	—	250	—	mV
		$V_{CCIO} = 2.5 V, \text{Hysteresis} = \text{Small}$	—	150	—	mV
		$V_{CCIO} = 1.8 V, \text{Hysteresis} = \text{Small}$	—	60	—	mV
		$V_{CCIO} = 1.5 V, \text{Hysteresis} = \text{Small}$	—	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A = 25^\circ C$, $f = 1.0 \text{ MHz}$.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO} , a transient current typically of 30 ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For true LVDS output pins in MachXO3L/LF devices, V_{IH} must be less than or equal to V_{CCIO} .
5. With bus keeper circuit turned on. For more details, refer to TN1280, [MachXO3 sysIO Usage Guide](#).

sysIO Recommended Operating Conditions

Standard	V _{CCIO} (V)			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3	3.135	3.3	3.465	—	—	—
LVC MOS 2.5	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—
LVDS33 ^{1, 2}	3.135	3.3	3.465	—	—	—
LVPECL ¹	3.135	3.3	3.465	—	—	—
BLVDS ¹	2.375	2.5	2.625	—	—	—
MIPI ³	2.375	2.5	2.625	—	—	—
MIPI_LP ³	1.14	1.2	1.26	—	—	—
LVC MOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVC MOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVC MOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVC MOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVC MOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVC MOS12R33 ⁴	3.135	3.3	3.6	0.45	0.6	0.75
LVC MOS12R25 ⁴	2.375	2.5	2.625	0.45	0.6	0.75
LVC MOS10R33 ⁴	3.135	3.3	3.6	0.35	0.5	0.65
LVC MOS10R25 ⁴	2.375	2.5	2.625	0.35	0.5	0.65

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. For the dedicated LVDS buffers.

3. Requires the addition of external resistors.

4. Supported only for inputs and BIDs for -6 speed grade devices.

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP} V_{INM}	Input Voltage	$V_{CCIO} = 3.3\text{ V}$	0	—	2.605	V
		$V_{CCIO} = 2.5\text{ V}$	0	—	2.05	V
V_{THD}	Differential Input Threshold		± 100	—		mV
V_{CM}	Input Common Mode Voltage	$V_{CCIO} = 3.3\text{ V}$	0.05	—	2.6	V
		$V_{CCIO} = 2.5\text{ V}$	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	± 10	μA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	$R_T = 100\text{ Ohm}$	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	$R_T = 100\text{ Ohm}$	0.90	1.025	—	V
V_{OD}	Output voltage differential	$(V_{OP} - V_{OM})$, $R_T = 100\text{ Ohm}$	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	$(V_{OP} - V_{OM})/2$, $R_T = 100\text{ Ohm}$	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	$V_{OD} = 0\text{ V}$ driver outputs shorted	—	—	24	mA

LVDS Emulation

MachXO3L/LF devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)

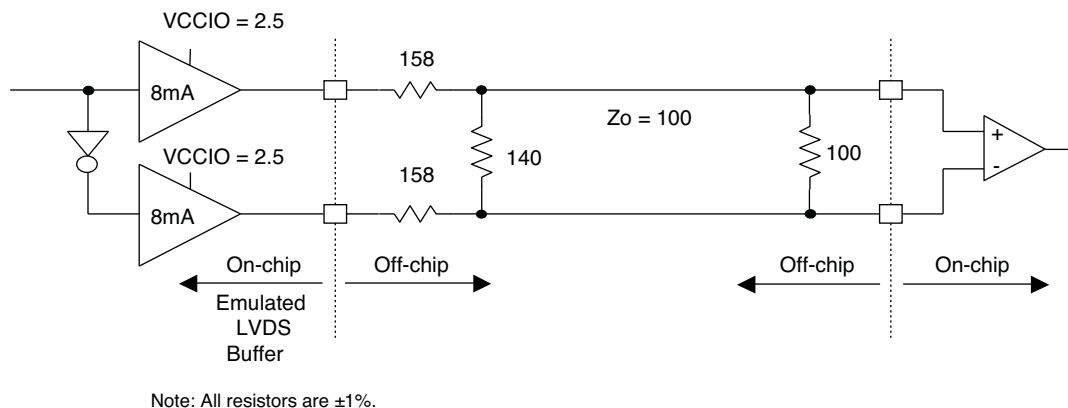


Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

MIPI D-PHY Emulation

MachXO3L/LF devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed IOs use the LVDS25E buffer and Low Power IOs use the LVC MOS buffers. The scheme shown in Figure 3-4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3-5 is one possible solution for MIPI D-PHY Transmitter implementation.

Figure 3-4. MIPI D-PHY Input Using External Resistors

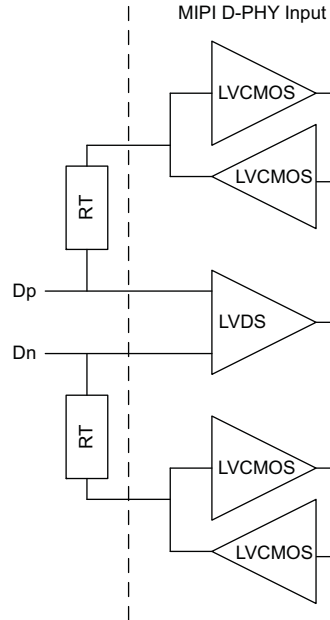


Table 3-4. MIPI DC Conditions¹

	Description	Min.	Typ.	Max.	Units
Receiver					
External Termination					
RT	1% external resistor with VCCIO=2.5 V	—	50	—	Ohms
	1% external resistor with VCCIO=3.3 V	—	50	—	Ohms
High Speed					
VCCIO	VCCIO of the Bank with LVDS Emulated input buffer	—	2.5	—	V
	VCCIO of the Bank with LVDS Emulated input buffer	—	3.3	—	V
VCMRX	Common-mode voltage HS receive mode	150	200	250	mV
VIDTH	Differential input high threshold	—	—	100	mV
VIDTL	Differential input low threshold	-100	—	—	mV
VIHHS	Single-ended input high voltage	—	—	300	mV
VILHS	Single-ended input low voltage	100	—	—	mV
ZID	Differential input impedance	80	100	120	Ohms

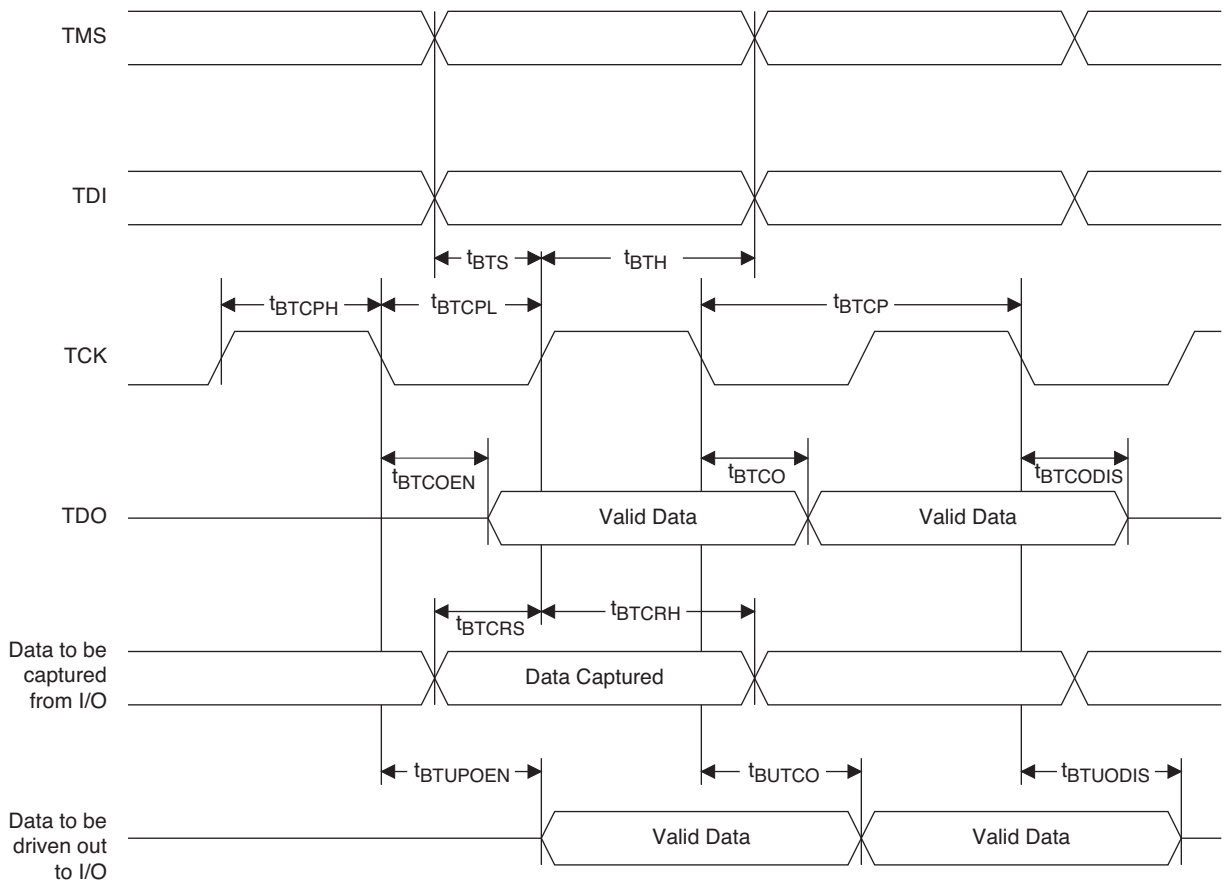
Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	2.87	—	3.18	—	ns
		MachXO3L/LF-2100	2.87	—	3.18	—	ns
		MachXO3L/LF-4300	2.96	—	3.28	—	ns
		MachXO3L/LF-6900	3.05	—	3.35	—	ns
		MachXO3L/LF-9400	3.06	—	3.37	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L/LF-1300	-0.83	—	-0.83	—	ns
		MachXO3L/LF-2100	-0.83	—	-0.83	—	ns
		MachXO3L/LF-4300	-0.87	—	-0.87	—	ns
		MachXO3L/LF-6900	-0.91	—	-0.91	—	ns
		MachXO3L/LF-9400	-0.93	—	-0.93	—	ns

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
MIPI D-PHY Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDR4_RX.ECLK.Centered ^{10, 11, 12}							
t _{SU} ¹⁵	Input Data Setup Before ECLK	All MachXO3L/LF devices, bottom side only	0.200	—	0.200	—	UI
t _{HO} ¹⁵	Input Data Hold After ECLK		0.200	—	0.200	—	UI
f _{DATA} ¹⁴	MIPI D-PHY Input Data Speed		—	900	—	900	Mbps
f _{DDR4} ¹⁴	MIPI D-PHY ECLK Frequency		—	450	—	450	MHz
f _{SCLK} ¹⁴	SCLK Frequency		—	112.5	—	112.5	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Aligned ⁸							
t _{DIA}	Output Data Invalid After CLK Output	All MachXO3L/LF devices, all sides	—	0.520	—	0.550	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	Mbps
f _{DDR1}	DDR1 SCLK frequency		—	150	—	125	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Centered ⁸							
t _{DVB}	Output Data Valid Before CLK Output	All MachXO3L/LF devices, all sides	1.210	—	1.510	—	ns
t _{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	Mbps
f _{DDR1}	DDR1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	MHz
Generic DDR2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Aligned ⁸							
t _{DIA}	Output Data Invalid After CLK Output	MachXO3L/LF devices, top side only	—	0.200	—	0.215	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	Mbps
f _{DDR2}	DDR2 ECLK frequency		—	332	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Centered ^{8, 9}							
t _{DVB}	Output Data Valid Before CLK Output	MachXO3L/LF devices, top side only	0.535	—	0.670	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	Mbps
f _{DDR2}	DDR2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_TX.ECLK.Aligned ^{8, 9}							
t _{DIA}	Output Data Invalid After CLK Output	MachXO3L/LF devices, top side only	—	0.200	—	0.215	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f _{DATA}	DDR4 Serial Output Data Speed		—	800	—	630	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	400	—	315	MHz
f _{SCLK}	SCLK Frequency		—	100	—	79	MHz

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-8. JTAG Port Timing Waveforms



Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I ² C clock input and master I ² C clock output.
SDA	I/O	Slave I ² C data input and master I ² C data output.

Pin Information Summary

	MachXO3L/LF-640	MachXO3L/LF-1300			
	CSFBGA121	WLCSP36	CSFBGA121	CSFBGA256	CABGA256
General Purpose IO per Bank					
Bank 0	24	15	24	50	50
Bank 1	26	0	26	52	52
Bank 2	26	9	26	52	52
Bank 3	24	4	24	16	16
Bank 4	0	0	0	16	16
Bank 5	0	0	0	20	20
Total General Purpose Single Ended IO	100	28	100	206	206
Differential IO per Bank					
Bank 0	12	8	12	25	25
Bank 1	13	0	13	26	26
Bank 2	13	4	13	26	26
Bank 3	11	2	11	8	8
Bank 4	0	0	0	8	8
Bank 5	0	0	0	10	10
Total General Purpose Differential IO	49	14	49	103	103
Dual Function IO	33	25	33	33	33
Number 7:1 or 8:1 Gearboxes					
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	7	3	7	14	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	7	2	7	14	14
High-speed Differential Outputs					
Bank 0	7	3	7	14	14
VCCIO Pins					
Bank 0	1	1	1	4	4
Bank 1	1	0	1	3	4
Bank 2	1	1	1	4	4
Bank 3	3	1	3	2	1
Bank 4	0	0	0	2	2
Bank 5	0	0	0	2	1
VCC	4	2	4	8	8
GND	10	2	10	24	24
NC	0	0	0	0	1
Reserved for Configuration	1	1	1	1	1
Total Count of Bonded Pins	121	36	121	256	256

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3L-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3LF-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND

Date	Version	Section	Change Summary
April 2016	1.6	Introduction	Updated Features section. — Revised logic density range and IO to LUT ratio under Flexible Architecture. — Revised 0.8 mm pitch information under Advanced Packaging. — Added MachXO3L-9400/MachXO3LF-9400 information to Table 1-1, MachXO3L/LF Family Selection Guide.
			Updated Introduction section. — Changed density from 6900 to 9400 LUTs. — Changed caBGA packaging to 19 x 19 mm.
		Architecture	Updated Architecture Overview section. — Changed statement to “All logic density devices in this family...” — Updated Figure 2-2 heading and notes.
			Updated sysCLOCK Phase Locked Loops (PLLs) section. — Changed statement to “All MachXO3L/LF devices have one or more sysCLOCK PLL.”
			Updated Programmable I/O Cells (PIC) section. — Changed statement to “All PIO pairs can implement differential receivers.”
			Updated sysIO Buffer Banks section. Updated Figure 2-5 heading.
			Updated Device Configuration section. Added Password and Soft Error Correction.
		DC and Switching Characteristics	Updated Static Supply Current – C/E Devices section. Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices.
			Updated Programming and Erase Supply Current – C/E Devices section. — Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices. — Changed LCMXO3L/LF-640E and LCMXO3L/LF-1300E Typ. values.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. Added MachXO3L/LF-9400 devices.
			Updated NVCM/Flash Download Time section. Added LCMXO3L/LF-9400C device.
			Updated sysCONFIG Port Timing Specifications section. — Added LCMXO3L/LF-9400C device. — Changed t_{INITL} units to from ns to us. — Changed $t_{DPPINIT}$ and $t_{DPPDONE}$ Max. values are per PCN#03A-16.
		Pinout Information	Updated Pin Information Summary section. Added LCMXO3L/LF-9400C device.
		Ordering Information	Updated MachXO3 Part Number Description section. — Added 9400 = 9400 LUTs. — Added BG484 package.
			Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.