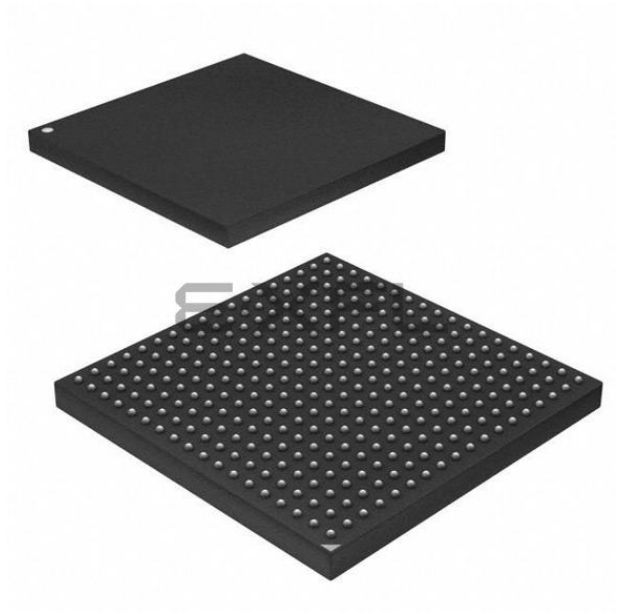

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	279
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	324-LFBGA
Supplier Device Package	324-CABGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-2100c-5bg324i

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode
In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode
Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  — A greater-than-or-equal-to B
  — A not-equal-to B
  — A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3L/LF devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO3L/LF devices, please see TN1290, Memory Usage Guide for MachXO3 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO3L/LF also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO3L/LF PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.

Figure 2-7. PLL Diagram

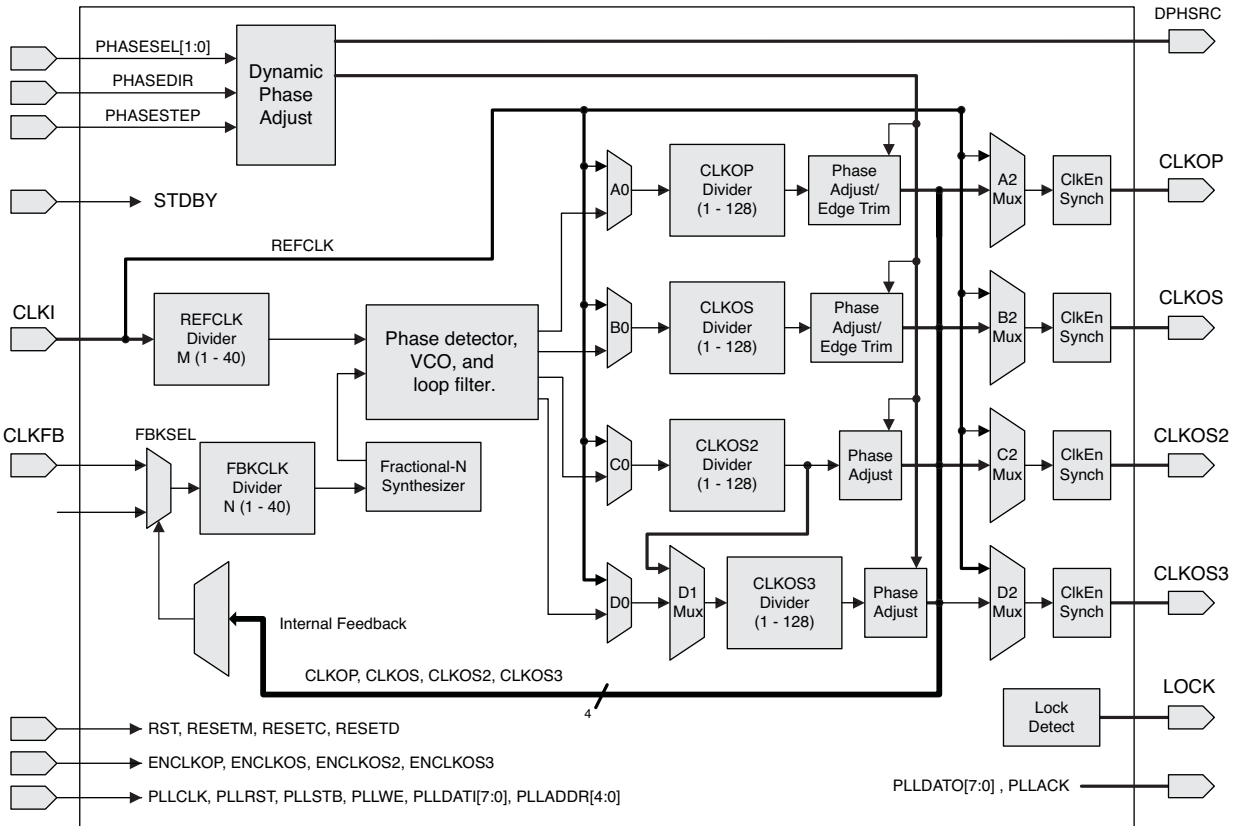


Table 2-4 provides signal descriptions of the PLL block.

Table 2-4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1290, Memory Usage Guide for MachXO3 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO3L/LF devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO3L/LF devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

All PIO pairs can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these devices have on-chip differential termination and also provide PCI support.

PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2-8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

Table 2-11 shows the I/O standards (together with their supply and reference voltages) supported by the MachXO3L/LF devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1280, MachXO3 sysIO Usage Guide.

Table 2-11. Supported Input Standards

	VCCIO (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5 V**	**1.2 V**
Single-Ended Interfaces					
LVTTL	Yes				
LVCMOS33	Yes				
LVCMOS25		Yes			
LVCMOS18			Yes		
LVCMOS15				Yes	
LVCMOS12					Yes
PCI	Yes				
Differential Interfaces					
LVDS	Yes	Yes			
BLVDS, MLVDS, LVPECL, RSDS	Yes	Yes			
MIPI[1]	Yes	Yes			
LVTTLD	Yes				
LVCMOS33D	Yes				
LVCMOS25D		Yes			
LVCMOS18D			Yes		

1. These interfaces can be emulated with external resistors in all devices.

Figure 2-15. MachXO3L/LF-1300 in 256 Ball Packages, MachXO3L/LF-2100, MachXO3L/LF-4300, MachXO3L/LF-6900 and MachXO3L/LF-9400 Banks

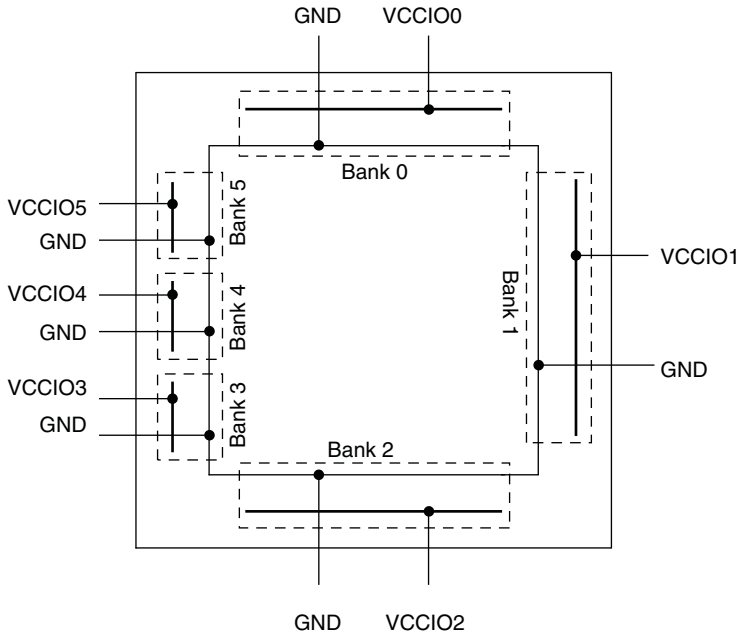
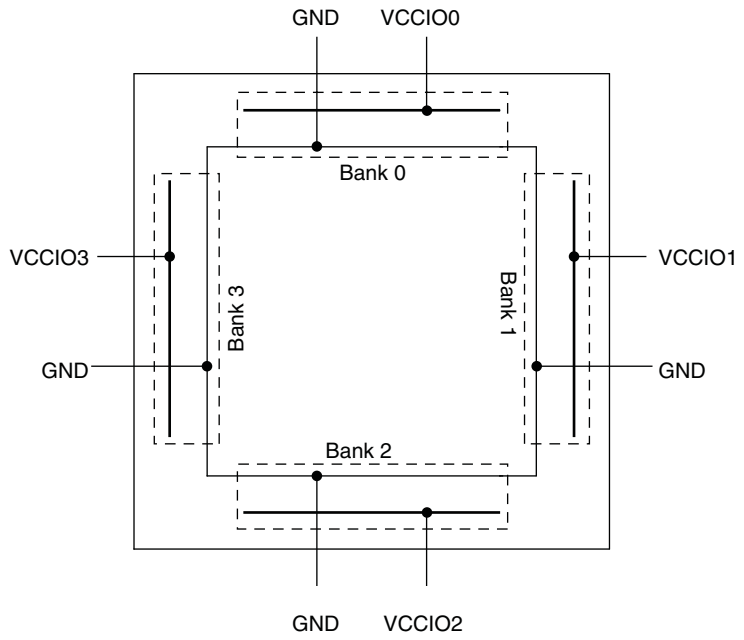


Figure 2-16. MachXO3L/LF-640 and MachXO3L/LF-1300 Banks



There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1293, Using Hardened Control Functions in MachXO3 Devices

Figure 2-19. SPI Core Block Diagram

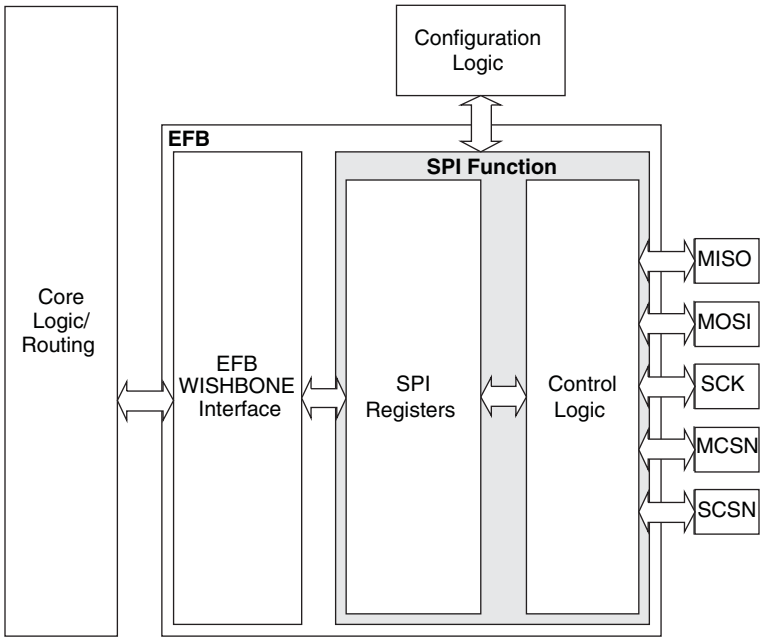


Table 2-15 describes the signals interfacing with the SPI cores.

Table 2-15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Configuration Logic.
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

Table 2-17. MachXO3L/LF Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1289, Power Estimation and Management for MachXO3 Devices.

Power On Reset

MachXO3L/LF devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration NVCM/Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For “E” devices without voltage regulators, V_{CCINT} is the same as the V_{CC} supply voltage. For “C” devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as NVCM/Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration. Note that for “C” devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once an “E” device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a mini-mal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.

Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

1. Internal NVCM/Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, MachXO3 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)
TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

Programming and Erase Supply Current – C/E Devices[1, 2, 3, 4]

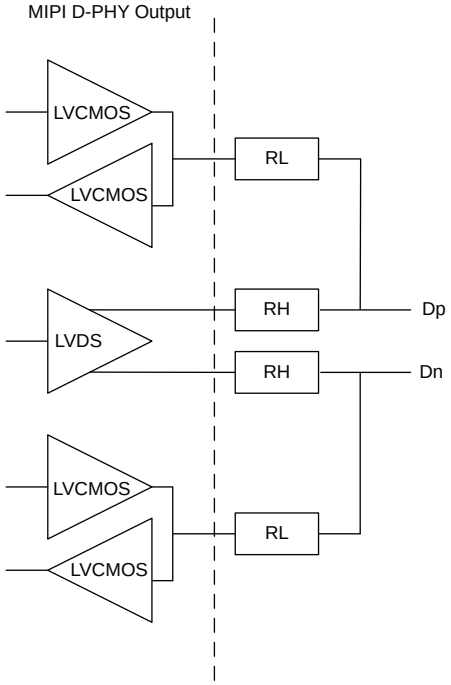
Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO3L/LF-1300C 256 Ball Package	22.1	mA
		LCMXO3L/LF-2100C	22.1	mA
		LCMXO3L/LF-2100C 324 Ball Package	26.8	mA
		LCMXO3L/LF-4300C	26.8	mA
		LCMXO3L/LF-4300C 400 Ball Package	33.2	mA
		LCMXO3L/LF-6900C	33.2	mA
		LCMXO3L/LF-9400C	39.6	mA
		LCMXO3L/LF-640E	17.7	mA
		LCMXO3L/LF-1300E	17.7	mA
		LCMXO3L/LF-1300E 256 Ball Package	18.3	mA
		LCMXO3L/LF-2100E	18.3	mA
		LCMXO3L/LF-2100E 324 Ball Package	20.4	mA
		LCMXO3L/LF-4300E	20.4	mA
		LCMXO3L/LF-6900E	23.9	mA
		LCMXO3L/LF-9400E	28.5	mA
I_{CCIO}	Bank Power Supply[5] VCCIO = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1289, Power Estimation and Management for MachXO3 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

	Description	Min.	Typ.	Max.	Units
Low Power					
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer		1.2		V
VIH	Logic 1 input voltage	—	—	0.88	V
VIL	Logic 0 input voltage, not in ULP State	0.55	—	—	V
VHYST	Input hysteresis	25	—	—	mV

1. Over Recommended Operating Conditions

Figure 3-5. MIPI D-PHY Output Using External Resistors



Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[8, 9]							
t_{DVA}	Input Data Valid After CLK	All MachXO3L/LF devices, all sides	—	0.317	—	0.344	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[8, 9]							
t_{SU}	Input Data Setup Before CLK	All MachXO3L/LF devices, all sides	0.566	—	0.560	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—		Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[8, 9]							
t_{DVA}	Input Data Valid After CLK	MachXO3L/LF devices, bottom side only	—	0.316	—	0.342	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[8, 9]							
t_{SU}	Input Data Setup Before CLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[8]							
t_{DVA}	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.307	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK		0.782	—	0.699	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[8]							
t_{SU}	Input Data Setup Before ECLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9]							
t_{DVA}	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.290	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
MIPI D-PHY Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Centered[10, 11, 12]							
t_{SU}[15]	Input Data Setup Before ECLK	All MachXO3L/LF devices, bottom side only	0.200	—	0.200	—	UI
t_{HO}[15]	Input Data Hold After ECLK		0.200	—	0.200	—	UI
f_{DATA}[14]	MIPI D-PHY Input Data Speed		—	900	—	900	Mbps
f_{DDRX4}[14]	MIPI D-PHY ECLK Frequency		—	450	—	450	MHz
f_{SCLK}[14]	SCLK Frequency		—	112.5	—	112.5	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	All MachXO3L/LF devices, all sides	—	0.520	—	0.550	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[8]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3L/LF devices, all sides	1.210	—	1.510	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	MHz
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[8]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3L/LF devices, top side only	—	0.200	—	0.215	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[8, 9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3L/LF devices, top side only	0.535	—	0.670	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[8, 9]							
t_{DIA}	Output Data Invalid After CLK Output	MachXO3L/LF devices, top side only	—	0.200	—	0.215	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz

Figure 3-6. Receiver GDDR71_RX. Waveforms

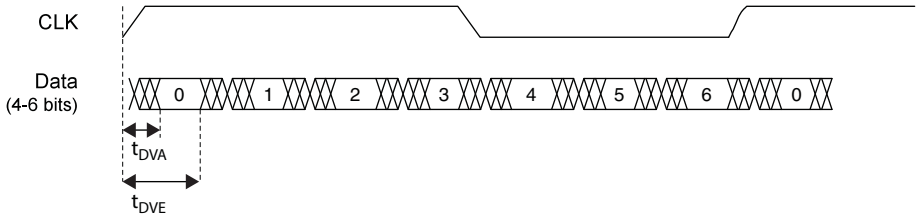
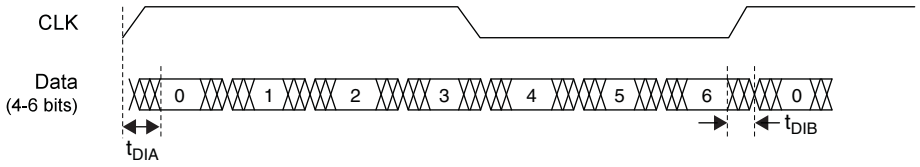


Figure 3-7. Transmitter GDDR71_TX. Waveforms



sysCLOCK PLL Timing

Over Recommended Operating Conditions

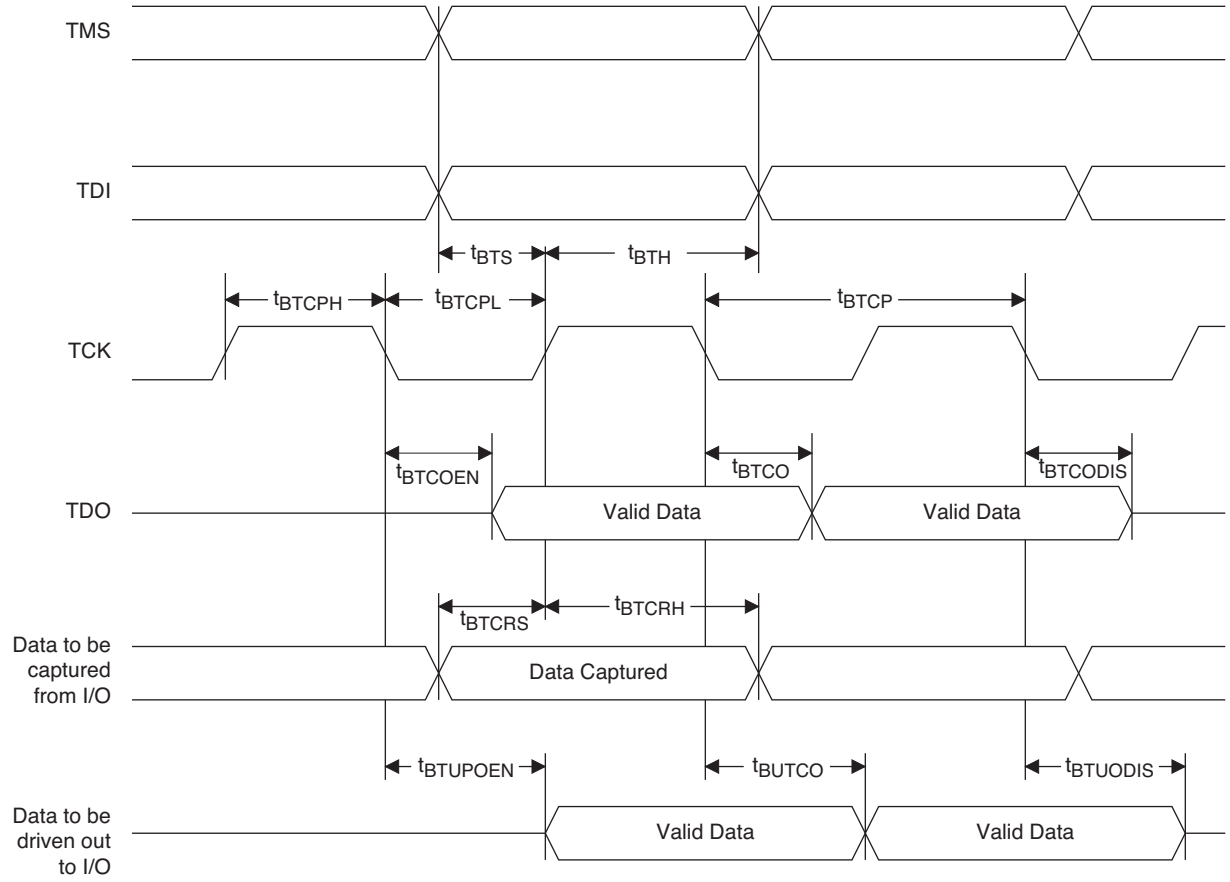
Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy		–75	75	%
t_{PH}[4]	Output Phase Accuracy		–6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	150	ps p-p
		f_{OUT} < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100 MHz	—	180	ps p-p
		f_{OUT} < 100 MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100 MHz	—	160	ps p-p
		f_{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_{W}	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq$ 20 MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-8. JTAG Port Timing Waveforms



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Modes					
t_{PRGM}	PROGRAMN low pulse accept		55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	25	ns
t_{INITL}	INITN low time	LCMXO3L/LF-640/ LCMXO3L/LF-1300	—	55	us
		LCMXO3L/LF-1300 256-Ball Package/ LCMXO3L/LF-2100	—	70	us
		LCMXO3L/LF-2100 324-Ball Package/ LCMXO3-4300	—	105	us
		LCMXO3L/LF-4300 400-Ball Package/ LCMXO3-6900	—	130	us
		LCMXO3L/LF-9400C	—	175	us
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	150	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	120	ns
Slave SPI					
f_{MAX}	CCLK clock frequency		—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	ns
t_{STSU}	CCLK setup time		2	—	ns
t_{STH}	CCLK hold time		0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	10	ns
t_{STOZ}	CCLK falling edge to valid disable		—	10	ns
t_{STOV}	CCLK falling edge to valid enable		—	10	ns
t_{SCS}	Chip select high time		25	—	ns
t_{SCSS}	Chip select setup time		3	—	ns
t_{SCSH}	Chip select hold time		3	—	ns
Master SPI					
f_{MAX}	MCLK clock frequency		—	133	MHz
t_{MCLKH}	MCLK clock pulse width high		3.75	—	ns
t_{MCLKL}	MCLK clock pulse width low		3.75	—	ns
t_{STSU}	MCLK setup time		5	—	ns
t_{STH}	MCLK hold time		1	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	us

	MachXO3L/LF-2100					
	WLCSP49	**CSFBGA121**	**CSFBGA256**	**CSFBGA324**	**CABGA256**	**CABGA324**
General Purpose IO per Bank						
Bank 0	19	24	50	71	50	71
Bank 1	0	26	52	62	52	68
Bank 2	13	26	52	72	52	72
Bank 3	0	7	16	22	16	24
Bank 4	0	7	16	14	16	16
Bank 5	6	10	20	27	20	28
Total General Purpose Single Ended IO	38	100	206	268	206	279
Differential IO per Bank						
Bank 0	10	12	25	36	25	36
Bank 1	0	13	26	30	26	34
Bank 2	6	13	26	36	26	36
Bank 3	0	3	8	10	8	12
Bank 4	0	3	8	6	8	8
Bank 5	3	5	10	13	10	14
Total General Purpose Differential IO	19	49	103	131	103	140
Dual Function IO	25	33	33	37	33	37
Number 7:1 or 8:1 Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18
High-speed Differential Outputs						
Bank 0	5	7	14	18	14	18
VCCIO Pins						
Bank 0	2	1	4	4	4	4
Bank 1	0	1	3	4	4	4
Bank 2	1	1	4	4	4	4
Bank 3	0	1	2	2	1	2
Bank 4	0	1	2	2	2	2
Bank 5	1	1	2	2	1	2
VCC	2	4	8	8	8	10
GND	4	10	24	16	24	16
NC	0	0	0	13	1	0
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	**49**	**121**	**256**	**324**	**256**	**324**

	MachXO3L/LF-4300						
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank							
Bank 0	29	24	50	71	50	71	83
Bank 1	0	26	52	62	52	68	84
Bank 2	20	26	52	72	52	72	84
Bank 3	7	7	16	22	16	24	28
Bank 4	0	7	16	14	16	16	24
Bank 5	7	10	20	27	20	28	32
Total General Purpose Single Ended IO	63	100	206	268	206	279	335
Differential IO per Bank							
Bank 0	15	12	25	36	25	36	42
Bank 1	0	13	26	30	26	34	42
Bank 2	10	13	26	36	26	36	42
Bank 3	3	3	8	10	8	12	14
Bank 4	0	3	8	6	8	8	12
Bank 5	3	5	10	13	10	14	16
Total General Purpose Differential IO	31	49	103	131	103	140	168
Dual Function IO	25	37	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21
High-speed Differential Outputs							
Bank 0	10	7	18	18	18	18	21
VCCIO Pins							
Bank 0	3	1	4	4	4	4	5
Bank 1	0	1	3	4	4	4	5
Bank 2	2	1	4	4	4	4	5
Bank 3	1	1	2	2	1	2	2
Bank 4	0	1	2	2	2	2	2
Bank 5	1	1	2	2	1	2	2
VCC	4	4	8	8	8	10	10
GND	6	10	24	16	24	16	33
NC	0	0	0	13	1	0	0
Reserved for Configuration	1	1	1	1	1	1	1
Total Count of Bonded Pins	**81**	**121**	**256**	**324**	**256**	**324**	**400**

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND