# Evy Eartice Semiconductor Corporation - <u>LCMXO3L-2100C-6BG324C Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	279
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-LFBGA
Supplier Device Package	324-CABGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-2100c-6bg324c

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### Table 1-1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900	9400
Distributed RAM (kbits)		5	10	16	34	54	73
EBR SRAM (I	kbits)	64	64	74	92	240	432
Number of PLLs		1	1	1	2	2	2
Hardened	l <sup>2</sup> C	2	2	2	2	2	2
Functions:	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY S	Support	Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Pr NVCM	ogrammable	MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400
Packages				ΙΟ			
36-ball WLCS (2.5 mm x 2.5	6P <sup>1</sup> 6 mm, 0.4 mm)		28				
49-ball WLCS (3.2 mm x 3.2	P <sup>1</sup> mm, 0.4 mm)			38			
81-ball WLCS (3.8 mm x 3.8	P <sup>1</sup> mm, 0.4 mm)				63		
121-ball csfB0 (6 mm x 6 mm	GA <sup>1</sup> n, 0.5 mm)	100	100	100	100		
256-ball csfB (9 mm x 9 mn	GA <sup>1</sup> n, 0.5 mm)		206	206	206	206	206
324-ball csfB (10 mm x 10	GA <sup>1</sup> mm, 0.5 mm)		2	268	268	281	
256-ball caBC (14 mm x 14 i	àA² mm, 0.8 mm)		206	206	206	206	206
324-ball caBC (15 mm x 15 i	àA² mm, 0.8 mm)			279	279	279	
400-ball caB0 (17 mm x 17 i	àA² mm, 0.8 mm)				335	335	335
484-ball caBC (19 mm x 19	3A² mm, 0.8 mm)						384

1. Package is only available for E=1.2 V devices.

2. Package is only available for C=2.5 V/3.3 V devices.

### Introduction

MachXO3<sup>™</sup> device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs



## MachXO3 Family Data Sheet Architecture

#### February 2017

Advance Data Sheet DS1047

### **Architecture Overview**

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK<sup>™</sup> PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.





Notes:

MachXO3L/LF-640 is similar to MachXO3L/LF-1300. MachXO3L/LF-640 has a lower LUT count.

MachXO3L devices have NVCM, MachXO3LF devices have Flash.

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state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

#### Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

#### Figure 2-9. Memory Core Reset



For further information on the sysMEM EBR block, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

#### EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

#### Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram

Reset	
Clock	
Clock	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f<sub>MAX</sub> (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.



### Figure 2-13. Input Gearbox



More information on the input gearbox is available in TN1281, Implementing High-Speed Interfaces with MachXO3 Devices.



### Table 2-12. Supported Output Standards

Output Standard	V <sub>CCIO</sub> (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	_
LVCMOS25, Open Drain	_
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	_
LVCMOS12, Open Drain	_
PCI33	3.3
Differential Interfaces	
LVDS <sup>1</sup>	2.5, 3.3
BLVDS, MLVDS, RSDS 1	2.5
LVPECL <sup>1</sup>	3.3
MIPI <sup>1</sup>	2.5
LVTTLD	3.3
LVCMOS33D	3.3
LVCMOS25D	2.5
LVCMOS18D	1.8

1. These interfaces can be emulated with external resistors in all devices.

### sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO3L/LF-1300 in the 256 Ball packages and the MachXO3L/LF-2100 and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO3L/LF-1300 and lower density devices have four banks (one bank per side). Figures 2-15 and 2-16 show the sysIO banks and their associated supplies for all devices.



### Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

### **On-chip Oscillator**

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-13 lists all the available MCLK frequencies.

### Table 2-13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133



### Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - Watchdog timer
  - Clear timer on compare match
  - Fast PWM
  - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

### Figure 2-20. Timer/Counter Block Diagram



Table 2-16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



For more details on these embedded functions, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

### **User Flash Memory (UFM)**

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

### **Standby Mode and Power Saving Options**

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V V<sub>CC</sub> and 3.3 V V<sub>CC</sub> while the E devices operate at 1.2 V V<sub>CC</sub>.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I<sup>2</sup>C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned "off" or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.



### **Configuration and Testing**

This section describes the configuration and testing features of the MachXO3L/LF family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with  $V_{CCIO}$  Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

### **Device Configuration**

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

- 1. Internal NVCM/Flash Download
- 2. JTAG
- 3. Standard Serial Peripheral Interface (Master SPI mode) interface to boot PROM memory
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, MachXO3 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/ LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.



## MachXO3 Family Data Sheet DC and Switching Characteristics

#### February 2017

#### Advance Data Sheet DS1047

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

	MachXO3L/LF E (1.2 V)	MachXO3L/LF C (2.5 V/3.3 V)
Supply Voltage V <sub>CC</sub>	$\ldots$ .–0.5 V to 1.32 V $\ldots$ $\ldots$	–0.5 V to 3.75 V
Output Supply Voltage V <sub>CCIO</sub>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied <sup>4, 5</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied <sup>4</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T <sub>1</sub> )	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

4. Overshoot and undershoot of -2 V to (V<sub>IHMAX</sub> + 2) volts is permitted for a duration of <20 ns.

5. The dual function  $I^2C$  pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

### **Recommended Operating Conditions**<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
V <sub>CC</sub> <sup>1</sup>	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V <sub>CCIO</sub> <sup>1, 2, 3</sup>	I/O Driver Supply Voltage	1.14	3.465	V
t <sub>JCOM</sub>	Junction Temperature Commercial Operation	0	85	°C
t <sub>JIND</sub>	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if V<sub>CCIO</sub> and V<sub>CC</sub> are both the same voltage, they must also be the same supply.

2. See recommended voltages by I/O standard in subsequent table.

3. V<sub>CCIO</sub> pins of unused I/O banks should be connected to the V<sub>CC</sub> power supply on boards.

### Power Supply Ramp Rates<sup>1</sup>

	iyp.	wax.	Units
t <sub>RAMP</sub> Power supply ramp rates for all power supplies. 0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

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### Table 3-5. MIPI D-PHY Output DC Conditions<sup>1</sup>

	Description	Min.	Тур.	Max.	Units
Transmitter	· · ·			•	
External Termination	on				
RL	1% external resistor with VCCIO = 2.5 V		50		Ohms
	1% external resistor with VCCIO = 3.3 V	—	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	_	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	_	464	—	Ohms
High Speed	· ·				·
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	_	2.5	_	V
	VCCIO of the Bank with LVDS Emulated output buffer	_	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage	_	—	360	V
ZOS	Single ended output impedance		50	_	Ohms
ΔZOS	Single ended output impedance mismatch		—	10	%
Low Power	· · · ·				
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	_	1.2	_	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	-50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

1. Over Recommended Operating Conditions



### Figure 3-6. Receiver GDDR71\_RX. Waveforms



Figure 3-7. Transmitter GDDR71\_TX. Waveforms





### NVCM/Flash Download Time<sup>1, 2</sup>

Symbol	Parameter	Device	Тур.	Units
t <sub>REFRESH</sub>	POR to Device I/O Active	LCMXO3L/LF-640	1.9	ms
		LCMXO3L/LF-1300	1.9	ms
		LCMXO3L/LF-1300 256-Ball Package	1.4	ms
		LCMXO3L/LF-2100	1.4	ms
		LCMXO3L/LF-2100 324-Ball Package	2.4	ms
		LCMXO3L/LF-4300	2.4	ms
		LCMXO3L/LF-4300 400-Ball Package	3.8	ms
		LCMXO3L/LF-6900	3.8	ms
		LCMXO3L/LF-9400C	5.2	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.



	MachXO3L/LF-2100					
	WLCSP49	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324
General Purpose IO per Bank		•	•			
Bank 0	19	24	50	71	50	71
Bank 1	0	26	52	62	52	68
Bank 2	13	26	52	72	52	72
Bank 3	0	7	16	22	16	24
Bank 4	0	7	16	14	16	16
Bank 5	6	10	20	27	20	28
Total General Purpose Single Ended IO	38	100	206	268	206	279
Differential IO per Bank						
Bank 0	10	12	25	36	25	36
Bank 1	0	13	26	30	26	34
Bank 2	6	13	26	36	26	36
Bank 3	0	3	8	10	8	12
Bank 4	0	3	8	6	8	8
Bank 5	3	5	10	13	10	14
Total General Purpose Differential IO	19	49	103	131	103	140
Dual Function IO	25	33	33	37	33	37
Number 7:1 or 8:1 Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18
High-speed Differential Outputs						
Bank 0	5	7	14	18	14	18
VCCIO Pins		•	•			
Bank 0	2	1	4	4	4	4
Bank 1	0	1	3	4	4	4
Bank 2	1	1	4	4	4	4
Bank 3	0	1	2	2	1	2
Bank 4	0	1	2	2	2	2
Bank 5	1	1	2	2	1	2
VCC	2	4	8	8	8	10
GND	4	10	24	16	24	16
NC	0	0	0	13	1	0
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	49	121	256	324	256	324



# MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-640E-5MG121I	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-1300E-5MG1211	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-1300E-6MG1211	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-1300C-5BG256C	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-6BG256C	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-5BG256I	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-1300C-6BG256I	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-2100E-6MG1211	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND



LCMXO3L-9400C-6BG484I

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND
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Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-5BG4001	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND

2.5 V/3.3 V

6

Halogen-Free caBGA

484

IND

9400



# MachXO3 Family Data Sheet Revision History

#### February 2017

Advance Data Sheet DS1047

Date	Version	Section	Change Summary
February 2017	ebruary 2017 1.8 Architecture	Architecture	Updated Supported Standards section. Corrected "MDVS" to "MLDVS" in Table 2-11, Supported Input Standards.
		DC and Switching Characteristics	Updated ESD Performance section. Added reference to the MachXO2 Product Family Qualification Summary document.
			Updated Static Supply Current – C/E Devices section. Added footnote 7.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. — Populated values for MachXO3L/LF-9400. — Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, corrected "t <sub>DVB</sub> " to "t <sub>DIB</sub> " and "t <sub>DVA</sub> " to "t <sub>DIA</sub> " and revised their descriptions. — Added Figure 3-6, Receiver GDDR71_RX Waveforms and Figure 3-7, Transmitter GDDR71_TX Waveforms.
		Pinout Information	Updated the Pin Information Summary section. Added MachXO3L/LF- 9600C packages.
May 2016	1.7	DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Modified I/O Tri-state Volt- age Applied and Dedicated Input Voltage Applied footnotes.
			Updated sysIO Recommended Operating Conditions section. — Added standards. — Added V <sub>REF</sub> (V) — Added footnote 4.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Added I/O standards.
		Ordering Information	Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.

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Date	Version	Section	Change Summary
April 2016	1.6	Introduction	Updated Features section. — Revised logic density range and IO to LUT ratio under Flexible Archi- tecture. — Revised 0.8 mm pitch information under Advanced Packaging. — Added MachXO3L-9400/MachXO3LF-9400 information to Table 1-1, MachXO3L/LF Family Selection Guide.
			Updated Introduction section. — Changed density from 6900 to 9400 LUTs. — Changed caBGA packaging to 19 x 19 mm.
		Architecture	Updated Architecture Overview section. — Changed statement to "All logic density devices in this family" — Updated Figure 2-2 heading and notes.
			Updated sysCLOCK Phase Locked Loops (PLLs) section. — Changed statement to "All MachXO3L/LF devices have one or more sysCLOCK PLL."
			Updated Programmable I/O Cells (PIC) section. — Changed statement to "All PIO pairs can implement differential receivers."
			Updated sysIO Buffer Banks section. Updated Figure 2-5 heading.
			Updated Device Configuration section. Added Password and Soft Error Correction.
		DC and Switching Characteristics	Updated Static Supply Current – C/E Devices section. Added LCMXO3L/ LF-9400C and LCMXO3L/LF-9400E devices.
		Updated Programming and Erase Supply Current – C/E Devices section. — Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices. — Changed LCMXO3L/LF-640E and LCMXO3L/LF-1300E Typ. values.	
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. Added MachXO3L/LF-9400 devices.
			Updated NVCM/Flash Download Time section. Added LCMXO3L/LF- 9400C device.
			Updated sysCONFIG Port Timing Specifications section. — Added LCMXO3L/LF-9400C device. — Changed t <sub>INITL</sub> units to from ns to us. — Changed t <sub>DPPINIT</sub> and t <sub>DPPDONE</sub> Max. values are per PCN#03A-16.
		Pinout Information	Updated Pin Information Summary section. Added LCMXO3L/LF-9400C device.
Orderin	Ordering Information	Updated MachXO3 Part Number Description section. — Added 9400 = 9400 LUTs. — Added BG484 package.	
			Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.



Date	Version	Section	Change Summary
September 2015	1.5	DC and Switching Characteristics	Updated the MIPI D-PHY Emulation section. Revised Table 3-5, MIPI D- PHY Output DC Conditions. — Revised RL Typ. value. — Revised RH description and values.
			Updated the Maximum sysIO Buffer Performance section. Revised MIPI Max. Speed value.
			Updated the MachXO3L/LF External Switching Characteristics – C/E Devices section. Added footnotes 14 and 15.
August 2015	1.4	Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.
		Ordering Information	Updated the top side markings section to indicate the use of LMXO3LF for the LCMXO3LF device.
March 2015	1.3	All	General update. Added MachXO3LF devices.
October 2014	1.2	Introduction	Updated Table 1-1, MachXO3L Family Selection Guide. Revised XO3L- 2100 and XO3L-4300 IO for 324-ball csfBGA package.
		Architecture	Updated the Dual Boot section. Corrected information on where the pri- mary bitstream and the golden image must reside.
		Pinout Information	Updated the Pin Information Summary section.
			Changed General Purpose IO Bank 5 values for MachXO3L-2100 and MachXO3L-4300 CSFBGA 324 package.
			Changed Number 7:1 or 8:1 Gearboxes for MachXO3L-640 and MachXO3L-1300.
			Removed DQS Groups (Bank 1) section.
			Changed VCCIO Pins Bank 1 values for MachXO3L-1300, MachXO3L- 2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.
			Changed GND values for MachXO3L-1300, MachXO3L-2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.
			Changed NC values for MachXO3L-2100 and MachXO3L-4300 CSF- BGA 324 package.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	1.1	DC and Switching Characteristics	Updated the Static Supply Current – C/E Devices section. Added devices.
			Updated the Programming and Erase Supply Current – C/E Device section. Added devices.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Revised footnote 4.
			Added the NVCM Download Time section.
			Updated the Typical Building Block Function Performance – C/E Devices section. Added information to footnote.
		Pinout Information	Updated the Pin Information Summary section.
		Ordering Information	Updated the MachXO3L Part Number Description section. Added packages.
			Updated the Ordering Information section. General update.





Date	Version	Section	Change Summary
June 2014	1.0	—	Product name/trademark adjustment.
		Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Changed fcCSP packages to csfBGA. Adjusted 121-ball csfBGA arrow.
			Introduction section general update.
		Architecture	General update.
		DC and Switching Characteristics	Updated sysIO Recommended Operating Conditions section. Removed V <sub>REF</sub> (V) column. Added standards.
			Updated Maximum sysIO Buffer Performance section. Added MIPI I/O standard.
			Updated MIPI D-PHY Emulation section. Changed Low Speed to Low Power. Updated Table 3-4, MIPI DC Conditions.
			Updated Table 3-5, MIPI D-PHY Output DC Conditions.
			Updated Maximum sysIO Buffer Performance section.
			Updated MachXO3L External Switching Characteristics – C/E Device section.
May 2014	00.3	Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Moved 121-ball fcCSP arrow.
			General update of Introduction section.
		Architecture	General update.
		Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
		Ordering Information	Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
			Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers.
February 2014	00.2	DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.
	00.1	_	Initial release.