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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	121-VFBGA, CSPBGA
Supplier Device Package	121-CSFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-2100e-5mg121i

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MachXO3 Family Data Sheet Architecture

February 2017

Advance Data Sheet DS1047

Architecture Overview

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK[™] PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.





Notes:

MachXO3L/LF-640 is similar to MachXO3L/LF-1300. MachXO3L/LF-640 has a lower LUT count.

MachXO3L devices have NVCM, MachXO3LF devices have Flash.

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PFU Blocks

The core of the MachXO3L/LF device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Block Diagram



Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

	PFU Block			
Slice	Resources	Modes		
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM		

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.



ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

Routing

There are many resources provided in the MachXO3L/LF devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO3L/LF device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO3L/LF architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO3L/LF devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3L/LF devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3L/LF External Switching Characteristics table.

Primary clock signals for the MachXO3L/LF-1300 and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sys-CLOCK PLL outputs.



Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-13 lists all the available MCLK frequencies.

Table 2-13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133



Figure 2-18. PC Core Block Diagram



Table 2-14 describes the signals interfacing with the I²C cores.

 Table 2-14. PC Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I ² C core. The signal is an output if the I ² C core is in master mode. The signal is an input if the I ² C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO3L/LF device.
i2c_sda	Bi-directional	Bi-directional data line of the l^2C core. The signal is an output when data is transmitted from the l^2C core. The signal is an input when data is received into the l^2C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of l^2C ports in each MachXO3L/LF device.
i2c_irqo	Output	Interrupt request output signal of the I ² C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I ² C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.

Hardened SPI IP Core

Every MachXO3L/LF device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO3L/LF devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface



Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
 - Watchdog timer
 - Clear timer on compare match
 - Fast PWM
 - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

Figure 2-20. Timer/Counter Block Diagram



Table 2-16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and NVCM/Flash spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

Password

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to TN1313, Using Password Security with MachXO3 Devices.

Dual Boot

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1292, MachXO3 Soft Error Detection Usage Guide.

Soft Error Correction

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to TN1292, MachXO3 Soft Error Detection (SED)/Correction (SEC) Usage Guide.



DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
		Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)			+175	μΑ
		Clamp OFF and $V_{IN} = V_{CCIO}$	-10	—	10	μΑ
I _{IL} , I _{IH} ^{1, 4}	Input or I/O Leakage	Clamp OFF and V _{CCIO} - 0.97 V < V _{IN} < V _{CCIO}	-175	_	—	μA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} - 0.97 V	_		10	μΑ
		Clamp OFF and V _{IN} = GND	_		10	μΑ
		Clamp ON and 0 V < V_{IN} < V_{CCIO}			10	μΑ
I _{PU}	I/O Active Pull-up Current	0 < V _{IN} < 0.7 V _{CCIO}	-30		-309	μΑ
I _{PD}	I/O Active Pull-down Current	V _{IL} (MAX) < V _{IN} < V _{CCIO}	30	—	305	μA
I _{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I _{BHHS}	Bus Hold High sustaining current	V _{IN} = 0.7V _{CCIO}	-30	_	_	μΑ
I _{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	_	—	305	μΑ
І _{внно}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	_	_	-309	μΑ
V _{BHT} ³	Bus Hold Trip Points		V _{IL} (MAX)	—	V _{IH} (MIN)	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)$	3	5	9	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)$	3	5.5	7	pf
		V _{CCIO} = 3.3 V, Hysteresis = Large	_	450	—	mV
		V _{CCIO} = 2.5 V, Hysteresis = Large		250	—	mV
	Hysteresis for Schmitt Trigger Inputs ⁵	V _{CCIO} = 1.8 V, Hysteresis = Large		125	—	mV
V		V _{CCIO} = 1.5 V, Hysteresis = Large	_	100	_	mV
VHYST		V _{CCIO} = 3.3 V, Hysteresis = Small	_	250	_	mV
		V _{CCIO} = 2.5 V, Hysteresis = Small	_	150	_	mV
		V _{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V _{CCIO} = 1.5 V, Hysteresis = Small	_	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25 °C, f = 1.0 MHz.

3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.

 When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6mA can occur on the high-tolow transition. For true LVDS output pins in MachXO3L/LF devices, V_{IH} must be less than or equal to V_{CCIO}.

5. With bus keeper circuit turned on. For more details, refer to TN1280, MachXO3 sysIO Usage Guide.



Table 3-5. MIPI D-PHY Output DC Conditions¹

	Description	Min.	Тур.	Max.	Units			
Transmitter								
External Termination	on							
RL	1% external resistor with VCCIO = 2.5 V —		50		Ohms			
	1% external resistor with VCCIO = 3.3 V	—	50	—				
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	erformance up to 800 — 330 — up 900 Mbps when		Ohms				
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	_	464	—	Ohms			
High Speed	· ·							
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	_	2.5	_	V			
	VCCIO of the Bank with LVDS Emulated output buffer	_	3.3	—	V			
VCMTX	HS transmit static common mode voltage	150	200	250	mV			
VOD	HS transmit differential voltage	140	200	270	mV			
VOHHS	HS output high voltage	_	—	360	V			
ZOS	Single ended output impedance		50	_	Ohms			
ΔZOS	Single ended output impedance mismatch		—	10	%			
Low Power	· · · ·							
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	_	1.2	_	V			
VOH	Output high level	1.1	1.2	1.3	V			
VOL	Output low level	-50	0	50	mV			
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms			

1. Over Recommended Operating Conditions



Typical Building Block Function Performance – C/E Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	–6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

 The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.



DC and Switching Characteristics MachXO3 Family Data Sheet

Parameter Description Device Min. Max. Min. Max. L General I/O Pin Parameters (Using Edge Clock without PLL)
General I/O Pin Parameters (Using Edge Clock without PLL) t _{COE} MachXO3L/LF-1300 - 7.53 - 7.76 MachXO3L/LF-2100 - 7.53 - 7.76 MachXO3L/LF-2100 - 7.45 - 7.68 MachXO3L/LF-6900 - 7.53 - 7.76 MachXO3L/LF-9400 - 8.93 - 9.35 MachXO3L/LF-1300 -0.19 - - 0.19 -
MachXO3L/LF-1300 - 7.53 - 7.76 t _{COE} Clock to Output - PIO Output Register MachXO3L/LF-2100 - 7.53 - 7.76 MachXO3L/LF-2100 - 7.45 - 7.68 MachXO3L/LF-6900 - 7.53 - 7.76 MachXO3L/LF-9400 - 8.93 - 9.35 MachXO3L/LF-1300 -0.19 - - 0.19 -
MachXO3L/LF-2100 — 7.53 — 7.76 Clock to Output - PIO Output Register MachXO3L/LF-4300 — 7.45 — 7.68 MachXO3L/LF-6900 — 7.53 — 7.76 MachXO3L/LF-9400 — 8.93 — 9.35 MachXO3L/LF-1300 -0.19 — -0.19 —
t _{COE} Clock to Output - PIO Output Register MachXO3L/LF-4300 7.45 7.68 MachXO3L/LF-6900 7.53 7.76 MachXO3L/LF-9400 8.93 9.35 MachXO3L/LF-1300 -0.19 -0.19
MachXO3L/LF-6900 — 7.53 — 7.76 MachXO3L/LF-9400 — 8.93 — 9.35 MachXO3L/LF-1300 -0.19 — -0.19 —
MachXO3L/LF-9400 — 8.93 — 9.35 MachXO3L/LF-1300 -0.19 — -0.19 —
MachXO3L/LF-1300 -0.190.19 -
MachXO3L/LF-2100 -0.190.19 -
t _{SUE} Clock to Data Setup - PIO Input Register MachXO3L/LF-4300 -0.160.16 -
MachXO3L/LF-6900 -0.190.19 -
MachXO3L/LF-9400 -0.200.20 -
MachXO3L/LF-1300 1.97 — 2.24 —
MachXO3L/LF-2100 1.97 — 2.24 —
t _{HE} Clock to Data Hold - PIO Input Register MachXO3L/LF-4300 1.89 - 2.16 -
MachXO3L/LF-6900 1.97 — 2.24 —
MachXO3L/LF-9400 1.98 — 2.25 —
MachXO3L/LF-1300 1.56 — 1.69 —
MachXO3L/LF-2100 1.56 — 1.69 —
tsu DELE with Data laput Dalay
MachXO3L/LF-6900 1.66 — 1.81 —
MachXO3L/LF-9400 1.71 — 1.85 —
MachXO3L/LF-1300 -0.230.23 -
MachXO3L/LF-2100 -0.230.23 -
tH DELE Input Data Hold - PIO Input Register with MachXO3L/LF-4300 -0.340.34 -
MachXO3L/LF-6900 -0.290.29 -
MachXO3L/LF-9400 -0.300.30 -
General I/O Pin Parameters (Using Primary Clock with PLL)
MachXO3L/LF-1300 — 5.98 — 6.01
MachXO3L/LF-2100 — 5.98 — 6.01
t _{COPL1} Clock to Output - PIO Output Register MachXO3L/LF-4300 — 5.99 — 6.02
MachXO3L/LF-6900 — 6.02 — 6.06
MachXO3L/LF-9400 — 5.55 — 6.13
MachXO3L/LF-1300 0.36 — 0.36 —
MachXO3L/LF-2100 0.36 — 0.36 —
t _{SUPU} Clock to Data Setup - PIO Input Register MachXO3L/LF-4300 0.35 — 0.35 —
MachXO3L/LF-6900 0.34 — 0.34 —
MachXO3L/LF-9400 0.33 — 0.33 —
MachXO3L/LF-1300 0.42 — 0.49 —
MachXO3L/LF-2100 0.42 — 0.49 —
t _{HPL1} Clock to Data Hold - PIO Input Register MachXO3L/LF-4300 0.43 - 0.50 -
MachXO3L/LF-6900 0.46 — 0.54 —
MachXO3L/LF-9400 0.47 — 0.55 —



DC and Switching Characteristics MachXO3 Family Data Sheet

			-	-6		5	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	2.87		3.18		ns
		MachXO3L/LF-2100	2.87		3.18	—	ns
t _{SU_DELPLL}		MachXO3L/LF-4300	2.96		3.28		ns
		MachXO3L/LF-6900	3.05		3.35		ns
		MachXO3L/LF-9400	3.06		3.37		ns
	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L/LF-1300	-0.83		-0.83		ns
^t H_DELPLL		MachXO3L/LF-2100	-0.83		-0.83		ns
		MachXO3L/LF-4300	-0.87		-0.87		ns
		MachXO3L/LF-6900	-0.91		-0.91	—	ns
		MachXO3L/LF-9400	-0.93	—	-0.93		ns



DC and Switching Characteristics MachXO3 Family Data Sheet

		-6		-5			
Description	Device	Min.	Max.	Min.	Max.	Units	
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered ^{8, 9}							
Output Data Valid Before CLK Output		0.455		0.570		ns	
Output Data Valid After CLK Output		0.455	—	0.570	_	ns	
DDRX4 Serial Output Data Speed	MachXO3L/LF devices,	—	800	—	630	Mbps	
DDRX4 ECLK Frequency (minimum limited by PLL)	top side only	_	400	_	315	MHz	
SCLK Frequency	-		100		79	MHz	
Itputs – GDDR71_TX.ECLK.7:1 ^{8, 9}							
Output Data Invalid Before CLK Output			0.160	_	0.180	ns	
Output Data Invalid After CLK Output			0.160		0.180	ns	
DDR71 Serial Output Data Speed	MachXO3L/LF devices,		756		630	Mbps	
DDR71 ECLK Frequency	top side only	_	378	—	315	MHz	
7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL)		_	108	_	90	MHz	
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_TX.ECLK.Centered ^{10, 11, 12}							
Output Data Valid Before CLK Output		0.200	—	0.200	_	UI	
Output Data Valid After CLK Output		0.200	—	0.200	_	UI	
MIPI D-PHY Output Data Speed	All MachXO3L/LF	_	900	—	900	Mbps	
MIPI D-PHY ECLK Frequency (minimum limited by PLL)	devices, top side only	_	450	_	450	MHz	
SCLK Frequency	<u> </u>	—	112.5	—	112.5	MHz	
	Description RX4 Outputs with Clock and Data Centered CECLK.Centered ^{8, 9} Output Data Valid Before CLK Output Output Data Valid After CLK Output DDRX4 Serial Output Data Speed DDRX4 ECLK Frequency (minimum limited by PLL) SCLK Frequency ttputs – GDDR71_TX.ECLK.7:1 ^{8, 9} Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed DDR71 ECLK Frequency 7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL) Outputs with Clock and Data Centered at P C.ECLK.Centered ^{10, 11, 12} Output Data Valid Before CLK Output Output Data Valid After CLK Output MIPI D-PHY Output Data Speed MIPI D-PHY ECLK Frequency (minimum limited by PLL) SCLK Frequency	DescriptionDeviceRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for C.ECLK.Centered ^{8, 9} In Using PCLK Pin for C.ECLK.Centered ^{8, 9} Output Data Valid Before CLK OutputMachXO3L/LF devices, top side onlyDDRX4 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side onlySCLK FrequencyOutput Data Invalid Before CLK OutputOutput Data Invalid Before CLK OutputMachXO3L/LF devices, top side onlyOutput Data Invalid After CLK OutputMachXO3L/LF devices, top side onlyDDR71 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDT71 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side onlyOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputMachXO3L/LF devices, top side onlyOutput Data Valid Before CLK OutputAll MachXO3L/LFOutput Data Valid After CLK OutputAll MachXO3L/LFMIPI D-PHY Output Data SpeedAll MachXO3L/LFMIPI D-PHY ECLK Frequency (minimum limited by PLL)All MachXO3L/LFSCLK FrequencyAll MachXO3L/LF	Description Device Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock (LECLK.Centered ^{8,9}) 0.455 Output Data Valid Before CLK Output 0.455 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only SCLK Frequency Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed MachXO3L/LF devices, top side only DDR71 ECLK Frequency Output Clock Frequency (SCLK) (minimum limited by PLL) Output Data Valid After CLK Output Output Data Valid Before CLK Output Output Data Valid After CLK Output 0.200 0.200 0.200 Output Data Valid After CLK Out	-6Min.Max.RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - CLECLK.Centered ^{8, 9} Output Data Valid Before CLK Output0.455Output Data Valid After CLK OutputMachXO3L/LF devices, top side only0.455DDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side only800SCLK Frequency (minimum limited by PLL)100400Output Data Invalid Before CLK Output0.160Output Data Invalid After CLK Output0.160DDR71 Serial Output Data Speed DDR71 Serial Output Data SpeedMachXO3L/LF devices, top side only108Output Swith Clock and Data Centered at Pin Using PCLK Pin for Clock Input - t.ECLK.Centered ^{10, 11, 12} 0.200Output Data Valid Before CLK Output DDR71 Serial Output Data SpeedAll MachXO3L/LF devices, top side only0.200Output Data Valid After CLK Output Mup PLL)All MachXO3L/LF devices, top side only0.200MIPI D-PHY Output Data Speed MIPI D-PHY CLK Frequency (minimum limited by PLL)All MachXO3L/LF devices, top side only450MIPI D-PHY ECLK Frequency (minimum limited by PLL)450450	Description Image: Description Image: Description Max. Min. Max. Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{8, 9} 0.455 - 0.570 Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only - 800 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 400 - SCLK Frequency - 0.160 -	Description Device Min. Max. Min. Max. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{9,9} 0.455 - 0.570 - Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 800 - 630 SCLK Frequency - 0.160 - 916 - 916 Output Data Invalid Before CLK Output MachXO3L/LF devices, top side only - 0.160 - 0.180 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 108 - 90 Output Data Valid After CLK Output MachXO3L/LF	

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

5. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.

6. The t_{SU DEL} and t_{H DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).

7. This number for general purpose usage. Duty cycle tolerance is +/-10%.

8. Duty cycle is $\pm -5\%$ for system usage.

9. Performance is calculated with 0.225 UI.

10. Performance is calculated with 0.20 UI.

11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.

12. Performance for Industrial devices and -5 devices are not modeled in the Diamond design tool.

13. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

14. Above 800 Mbps is only supported with WLCSP and csfBGA packages

15. Between 800 Mbps to 900 Mbps:

a. VIDTH exceeds the MIPI D-PHY Input DC Conditions Table 3-4 and can be calculated with the equation tSU or tH = -0.0005*VIDTH + 0.3284

b. Example calculations

i. tSU and tHO = 0.28 with VIDTH = 100 mV

ii. tSU and tHO = 0.25 with VIDTH = 170 mV

iii. tSU and tHO = 0.20 with VIDTH = 270 mV



JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	TCK clock frequency	—	25	MHz
t _{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t _{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t _{BTS}	TCK [BSCAN] setup time	10	—	ns
t _{BTH}	TCK [BSCAN] hold time	8	—	ns
t _{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t _{BTCODIS}	TAP controller falling edge of clock to valid disable	—	10	ns
t _{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t _{BTCRS}	BSCAN test capture register setup time	8	—	ns
t _{BTCRH}	BSCAN test capture register hold time	20	—	ns
t _{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t _{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t _{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-8. JTAG Port Timing Waveforms





MachXO3 Family Data Sheet Pinout Information

February 2017

Advance Data Sheet DS1047

Signal Descriptions

Signal Name	I/O	Descriptions			
General Purpose					
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).			
		Row/Column Number] indicates the PFU row or the column of the device on which the PIO aroup exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.			
		[A/B/C/D] indicates the PIO within the group to which the pad is connected.			
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	ome of these user-programmable pins are shared with special function pins. When not use special function pins, these pins can be programmed as I/Os for user logic.			
		During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.			
NC	—	No connect.			
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.			
VCC	_	$_{\rm CC}$ – The power supply pins for core logic. Dedicated pins. It is recommended that all VC re tied to the same supply.			
VCCIOx	_	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.			
PLL and Clock Functi	ons (Us	ed as user-programmable I/O pins when not used for PLL or clock pins)			
[LOC]_GPLL[T, C]_IN	_	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.			
[LOC]_GPLL[T, C]_FB	_	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.			
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.			
Test and Programmin	g (Dual f	function pins used for test access port and during sysCONFIG™)			
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.			
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.			
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.			
TDO	0	Output pin – Test Data output pin used to shift data out of the device using 1149.1.			
		Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:			
JTAGENB	I	If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.			
		If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.			
		For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.			

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	MachXO3L/LF-2100					
	WLCSP49	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324
General Purpose IO per Bank		•	•			
Bank 0	19	24	50	71	50	71
Bank 1	0	26	52	62	52	68
Bank 2	13	26	52	72	52	72
Bank 3	0	7	16	22	16	24
Bank 4	0	7	16	14	16	16
Bank 5	6	10	20	27	20	28
Total General Purpose Single Ended IO	38	100	206	268	206	279
Differential IO per Bank						
Bank 0	10	12	25	36	25	36
Bank 1	0	13	26	30	26	34
Bank 2	6	13	26	36	26	36
Bank 3	0	3	8	10	8	12
Bank 4	0	3	8	6	8	8
Bank 5	3	5	10	13	10	14
Total General Purpose Differential IO	19	49	103	131	103	140
Dual Function IO	25	33	33	37	33	37
Number 7:1 or 8:1 Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18
High-speed Differential Outputs						
Bank 0	5	7	14	18	14	18
VCCIO Pins		•	•			
Bank 0	2	1	4	4	4	4
Bank 1	0	1	3	4	4	4
Bank 2	1	1	4	4	4	4
Bank 3	0	1	2	2	1	2
Bank 4	0	1	2	2	2	2
Bank 5	1	1	2	2	1	2
VCC	2	4	8	8	8	10
GND	4	10	24	16	24	16
NC	0	0	0	13	1	0
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	49	121	256	324	256	324



MachXO3 Family Data Sheet Ordering Information

May 2016

Advance Data Sheet DS1047

MachXO3 Part Number Description



Ordering Information

MachXO3L/LF devices have top-side markings as shown in the examples below, on the 256-Ball caBGA package with MachXO3-6900 device in Commercial Temperature in Speed Grade 5. Notice that for the MachXO3LF device, *LMXO3LF* is used instead of *LCMXO3LF* as in the Part Number.



with LMXO3LF

Note: Markings are abbreviated for small packages.

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Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	СОМ
LCMXO3LF-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND



Date	Version	Section	Change Summary
April 2016	1.6	Introduction	Updated Features section. — Revised logic density range and IO to LUT ratio under Flexible Archi- tecture. — Revised 0.8 mm pitch information under Advanced Packaging. — Added MachXO3L-9400/MachXO3LF-9400 information to Table 1-1, MachXO3L/LF Family Selection Guide.
			Updated Introduction section. — Changed density from 6900 to 9400 LUTs. — Changed caBGA packaging to 19 x 19 mm.
		Architecture	Updated Architecture Overview section. — Changed statement to "All logic density devices in this family" — Updated Figure 2-2 heading and notes.
			Updated sysCLOCK Phase Locked Loops (PLLs) section. — Changed statement to "All MachXO3L/LF devices have one or more sysCLOCK PLL."
			Updated Programmable I/O Cells (PIC) section. — Changed statement to "All PIO pairs can implement differential receivers."
			Updated sysIO Buffer Banks section. Updated Figure 2-5 heading.
			Updated Device Configuration section. Added Password and Soft Error Correction.
		DC and Switching Characteristics	Updated Static Supply Current – C/E Devices section. Added LCMXO3L/ LF-9400C and LCMXO3L/LF-9400E devices.
	Updated Program — Added LCMX — Changed LCM	Updated Programming and Erase Supply Current – C/E Devices section. — Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices. — Changed LCMXO3L/LF-640E and LCMXO3L/LF-1300E Typ. values.	
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. Added MachXO3L/LF-9400 devices.
			Updated NVCM/Flash Download Time section. Added LCMXO3L/LF- 9400C device.
		Updated sysCONFIG Port Timing — Added LCMXO3L/LF-9400C do — Changed t _{INITL} units to from ns — Changed toppoor	Updated sysCONFIG Port Timing Specifications section. — Added LCMXO3L/LF-9400C device. — Changed t _{INITL} units to from ns to us. — Changed t _{DPPINIT} and t _{DPPDONE} Max. values are per PCN#03A-16.
		Pinout Information	Updated Pin Information Summary section. Added LCMXO3L/LF-9400C device.
		Ordering Information	Updated MachXO3 Part Number Description section. — Added 9400 = 9400 LUTs. — Added BG484 package.
			Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.





Date	Version	Section	Change Summary
June 2014	1.0	—	Product name/trademark adjustment.
		Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Changed fcCSP packages to csfBGA. Adjusted 121-ball csfBGA arrow.
			Introduction section general update.
		Architecture	General update.
		DC and Switching Characteristics	Updated sysIO Recommended Operating Conditions section. Removed V _{REF} (V) column. Added standards.
			Updated Maximum sysIO Buffer Performance section. Added MIPI I/O standard.
			Updated MIPI D-PHY Emulation section. Changed Low Speed to Low Power. Updated Table 3-4, MIPI DC Conditions.
			Updated Table 3-5, MIPI D-PHY Output DC Conditions.
			Updated Maximum sysIO Buffer Performance section.
			Updated MachXO3L External Switching Characteristics – C/E Device section.
May 2014	00.3	Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Moved 121-ball fcCSP arrow.
			General update of Introduction section.
		Architecture	General update.
		Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
		Ordering Information	Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
			Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers.
February 2014	00.2	DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.
	00.1		Initial release.