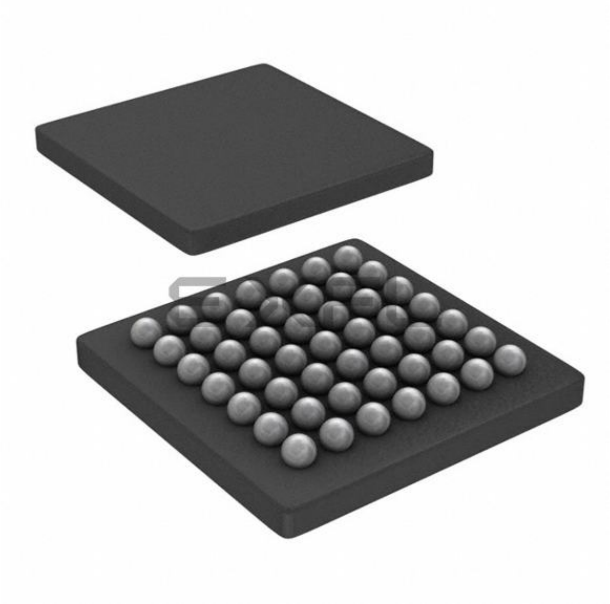


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	38
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.11x3.19)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-2100e-5uwg49itr

Table 1-1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900	9400
Distributed RAM (kbits)		5	10	16	34	54	73
EBR SRAM (kbits)		64	64	74	92	240	432
Number of PLLs		1	1	1	2	2	2
Hardened Functions:	I^2C	2	2	2	2	2	2
	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY Support		Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Programmable NVCM		MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400
Packages		**IO**					
36-ball WLCSP[1] (2.5 mm x 2.5 mm, 0.4 mm)			28				
49-ball WLCSP[1] (3.2 mm x 3.2 mm, 0.4 mm)				38			
81-ball WLCSP[1] (3.8 mm x 3.8 mm, 0.4 mm)					63		
121-ball csfBGA[1] (6 mm x 6 mm, 0.5 mm)		100	100	100	100		
256-ball csfBGA[1] (9 mm x 9 mm, 0.5 mm)			206	206	206	206	206
324-ball csfBGA[1] (10 mm x 10 mm, 0.5 mm)				268	268	281	
256-ball caBGA[2] (14 mm x 14 mm, 0.8 mm)			206	206	206	206	206
324-ball caBGA[2] (15 mm x 15 mm, 0.8 mm)				279	279	279	
400-ball caBGA[2] (17 mm x 17 mm, 0.8 mm)					335	335	335
484-ball caBGA[2] (19 mm x 19 mm, 0.8 mm)							384

1. Package is only available for E=1.2 V devices.
2. Package is only available for C=2.5 V/3.3 V devices.

Introduction

MachXO3™ device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I^2C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  — A greater-than-or-equal-to B
  — A not-equal-to B
  — A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3L/LF devices support distributed memory initialization.

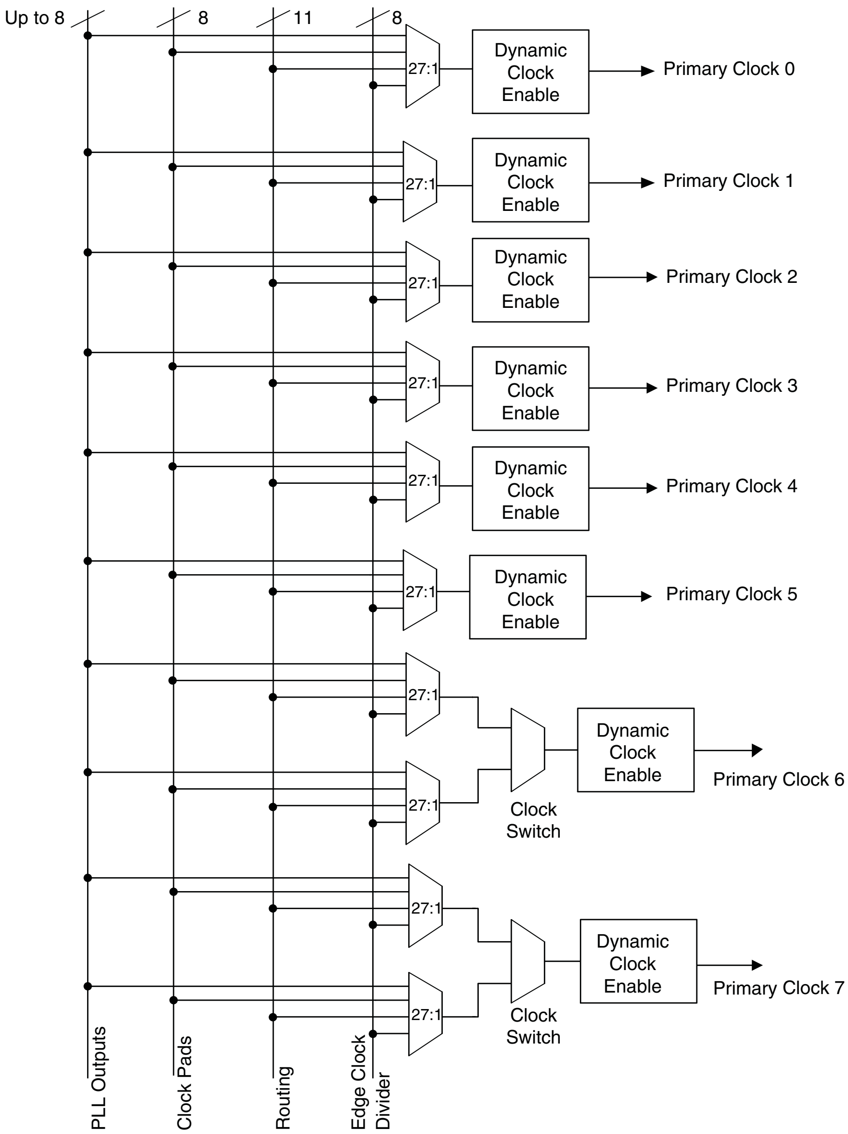
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO3L/LF devices, please see TN1290, Memory Usage Guide for MachXO3 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

Figure 2-5. Primary Clocks for MachXO3L/LF Devices



Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO3L/LF External Switching Characteristics table.

Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

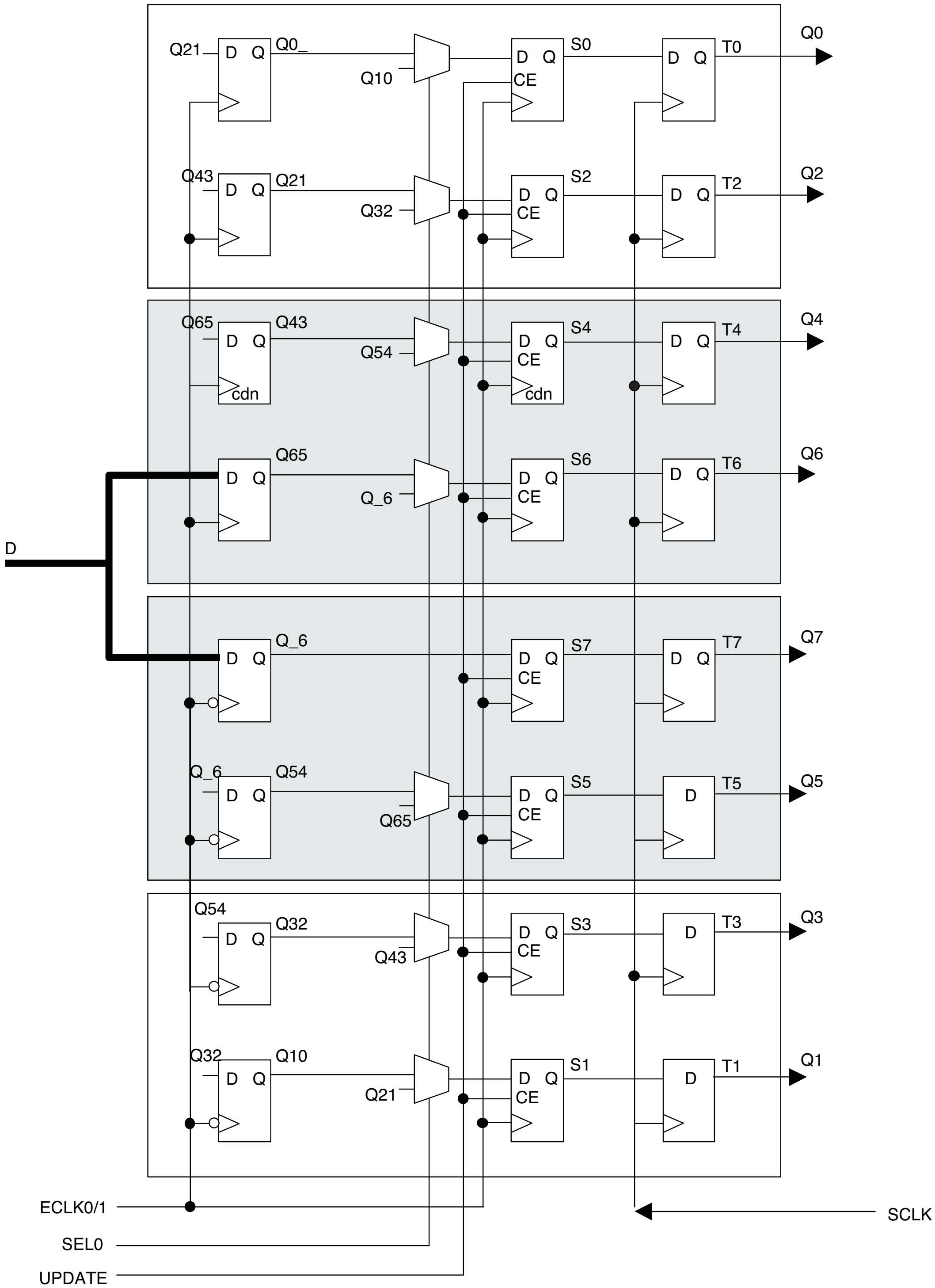
Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset

Figure 2-13. Input Gearbox



More information on the input gearbox is available in TN1281, Implementing High-Speed Interfaces with MachXO3 Devices.

Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  — Watchdog timer
  — Clear timer on compare match
  — Fast PWM
  — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

Figure 2-20. Timer/Counter Block Diagram

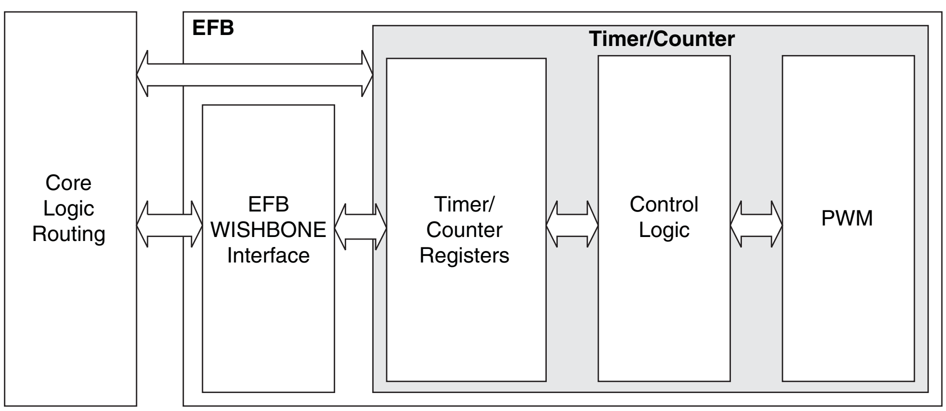


Table 2-16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

1. Internal NVCM/Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, MachXO3 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and NVCM/Flash spaces is allowed.
2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

Password

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to TN1313, Using Password Security with MachXO3 Devices.

Dual Boot

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1292, MachXO3 Soft Error Detection Usage Guide.

Soft Error Correction

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to TN1292, MachXO3 Soft Error Detection (SED)/Correction (SEC) Usage Guide.

TraceID

Each MachXO3L/LF device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

Density Shifting

The MachXO3L/LF family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO3 migration files.

Static Supply Current – C/E Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO3L/LF-1300C 256 Ball Package	4.8	mA
		LCMXO3L/LF-2100C	4.8	mA
		LCMXO3L/LF-2100C 324 Ball Package	8.45	mA
		LCMXO3L/LF-4300C	8.45	mA
		LCMXO3L/LF-4300C 400 Ball Package	12.87	mA
		LCMXO3L/LF-6900C[7]	12.87	mA
		LCMXO3L/LF-9400C[7]	17.86	mA
		LCMXO3L/LF-640E	1.00	mA
		LCMXO3L/LF-1300E	1.00	mA
		LCMXO3L/LF-1300E 256 Ball Package	1.39	mA
		LCMXO3L/LF-2100E	1.39	mA
		LCMXO3L/LF-2100E 324 Ball Package	2.55	mA
		LCMXO3L/LF-4300E	2.55	mA
		LCMXO3L/LF-6900E	4.06	mA
		LCMXO3L/LF-9400E	5.66	mA
I_{CCIO}	Bank Power Supply[5] VCCIO = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1289, Power Estimation and Management for MachXO3 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO3L/LF peak start-up current data, use the Power Calculator tool.
7. Determination of safe ambient operating conditions requires use of the Diamond Power Calculator tool.

Programming and Erase Supply Current – C/E Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO3L/LF-1300C 256 Ball Package	22.1	mA
		LCMXO3L/LF-2100C	22.1	mA
		LCMXO3L/LF-2100C 324 Ball Package	26.8	mA
		LCMXO3L/LF-4300C	26.8	mA
		LCMXO3L/LF-4300C 400 Ball Package	33.2	mA
		LCMXO3L/LF-6900C	33.2	mA
		LCMXO3L/LF-9400C	39.6	mA
		LCMXO3L/LF-640E	17.7	mA
		LCMXO3L/LF-1300E	17.7	mA
		LCMXO3L/LF-1300E 256 Ball Package	18.3	mA
		LCMXO3L/LF-2100E	18.3	mA
		LCMXO3L/LF-2100E 324 Ball Package	20.4	mA
		LCMXO3L/LF-4300E	20.4	mA
		LCMXO3L/LF-6900E	23.9	mA
		LCMXO3L/LF-9400E	28.5	mA
I_{CCIO}	Bank Power Supply[5] VCCIO = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1289, Power Estimation and Management for MachXO3 Devices.
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

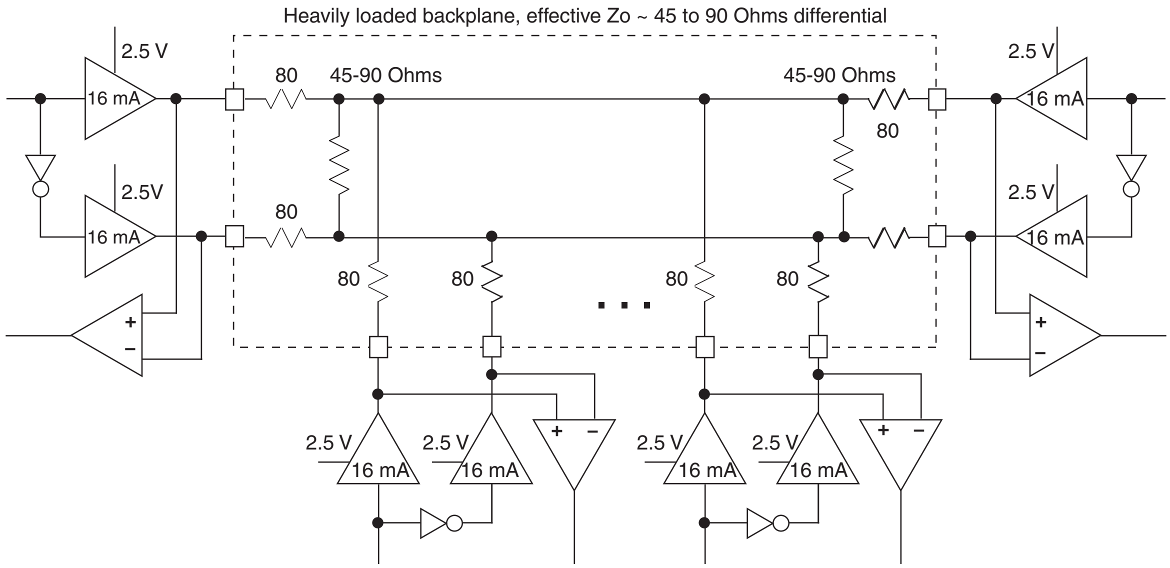


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

LVPECL

The MachXO3L/LF family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

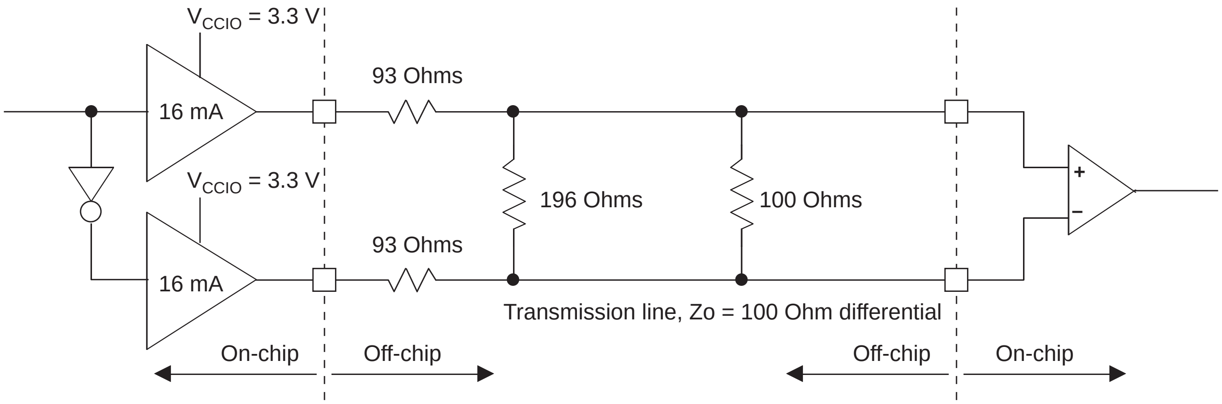


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

MIPI D-PHY Emulation

MachXO3L/LF devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed IOs use the LVDS25E buffer and Low Power IOs use the LVCMOS buffers. The scheme shown in Figure 3-4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3-5 is one possible solution for MIPI D-PHY Transmitter implementation.

Figure 3-4. MIPI D-PHY Input Using External Resistors

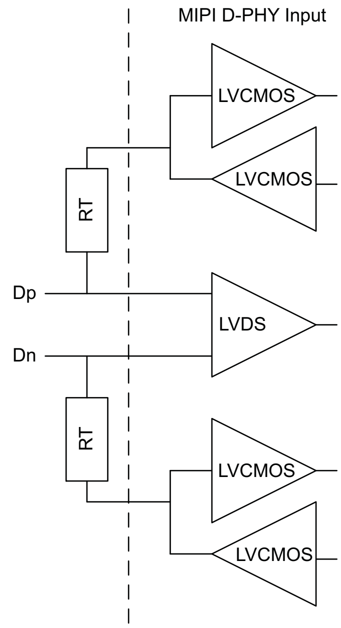


Table 3-4. MIPI DC Conditions[1]

	Description	Min.	Typ.	Max.	Units
Receiver					
External Termination					
RT	1% external resistor with VCCIO=2.5 V	—	50	—	Ohms
	1% external resistor with VCCIO=3.3 V	—	50	—	Ohms
High Speed					
VCCIO	VCCIO of the Bank with LVDS Emulated input buffer	—	2.5	—	V
	VCCIO of the Bank with LVDS Emulated input buffer	—	3.3	—	V
VCMRX	Common-mode voltage HS receive mode	150	200	250	mV
VIDTH	Differential input high threshold	—	—	100	mV
VIDTL	Differential input low threshold	–100	—	—	mV
VIHHS	Single-ended input high voltage	—	—	300	mV
VILHS	Single-ended input low voltage	100	—	—	mV
ZID	Differential input impedance	80	100	120	Ohms

MachXO3L/LF External Switching Characteristics – C/E Devices[1, 2, 3, 4, 5, 6, 10]

Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Clocks							
Primary Clocks							
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	All MachXO3L/LF devices	—	388	—	323	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO3L/LF devices	0.5	—	0.6	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO3L/LF-1300	—	867	—	897	ps
		MachXO3L/LF-2100	—	867	—	897	ps
		MachXO3L/LF-4300	—	865	—	892	ps
		MachXO3L/LF-6900	—	902	—	942	ps
		MachXO3L/LF-9400	—	908	—	950	ps
Edge Clock							
f_{MAX_EDGE}[7]	Frequency for Edge Clock	MachXO3L/LF	—	400	—	333	MHz
Pin-LUT-Pin Propagation Delay							
t_{PD}	Best case propagation delay through one LUT-4	All MachXO3L/LF devices	—	6.72	—	6.96	ns
General I/O Pin Parameters (Using Primary Clock without PLL)							
t_{CO}	Clock to Output - PIO Output Register	MachXO3L/LF-1300	—	7.46	—	7.66	ns
		MachXO3L/LF-2100	—	7.46	—	7.66	ns
		MachXO3L/LF-4300	—	7.51	—	7.71	ns
		MachXO3L/LF-6900	—	7.54	—	7.75	ns
		MachXO3L/LF-9400	—	7.53	—	7.83	ns
t_{SU}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-1300	–0.20	—	–0.20	—	ns
		MachXO3L/LF-2100	–0.20	—	–0.20	—	ns
		MachXO3L/LF-4300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-6900	–0.23	—	–0.23	—	ns
		MachXO3L/LF-9400	–0.24	—	–0.24	—	ns
t_H	Clock to Data Hold - PIO Input Register	MachXO3L/LF-1300	1.89	—	2.13	—	ns
		MachXO3L/LF-2100	1.89	—	2.13	—	ns
		MachXO3L/LF-4300	1.94	—	2.18	—	ns
		MachXO3L/LF-6900	1.98	—	2.23	—	ns
		MachXO3L/LF-9400	1.99	—	2.24	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	1.61	—	1.76	—	ns
		MachXO3L/LF-2100	1.61	—	1.76	—	ns
		MachXO3L/LF-4300	1.66	—	1.81	—	ns
		MachXO3L/LF-6900	1.53	—	1.67	—	ns
		MachXO3L/LF-9400	1.65	—	1.80	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-2100	–0.23	—	–0.23	—	ns
		MachXO3L/LF-4300	–0.25	—	–0.25	—	ns
		MachXO3L/LF-6900	–0.21	—	–0.21	—	ns
		MachXO3L/LF-9400	–0.24	—	–0.24	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO3L/LF devices	—	388	—	323	MHz

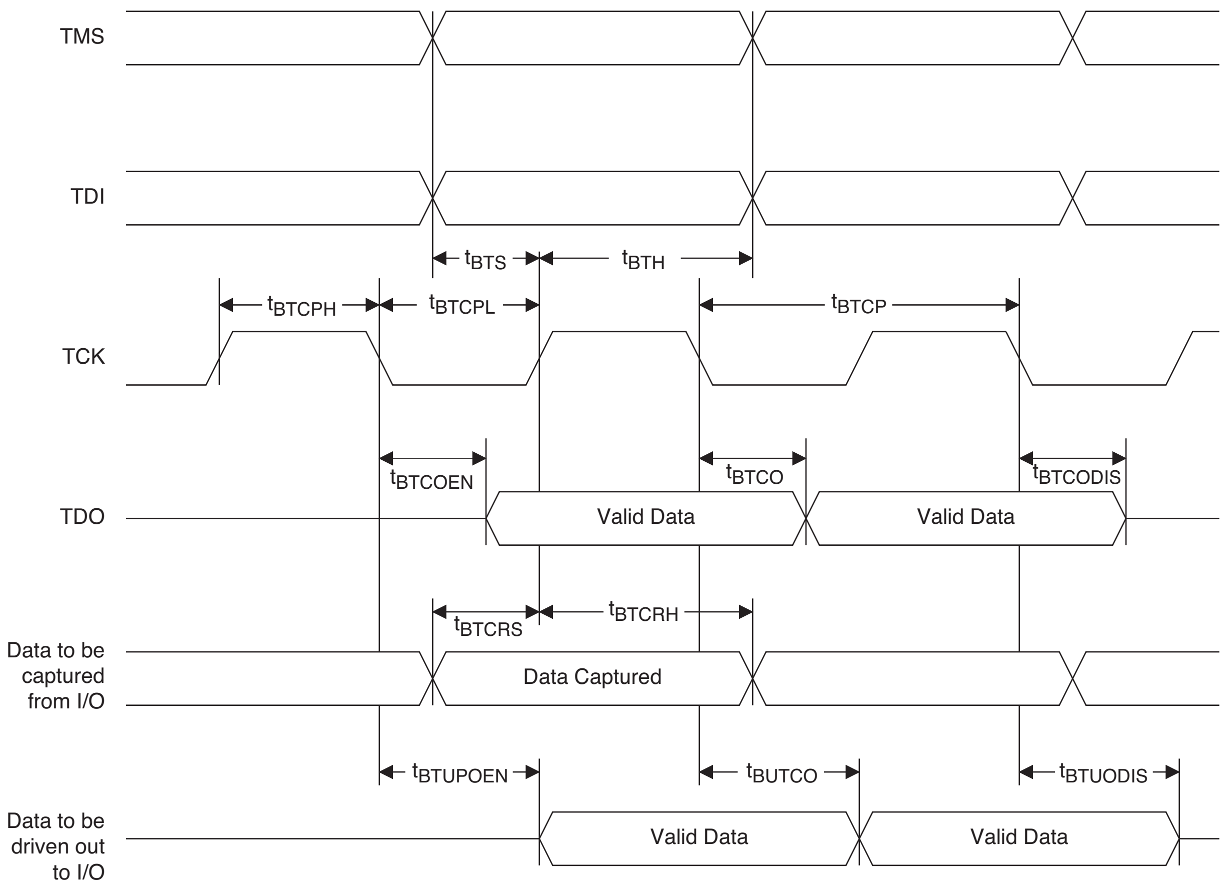
Parameter	Description	Device	–6 Min.	–6 Max.	–5 Min.	–5 Max.	Units
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[8, 9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3L/LF devices, top side only	0.455	—	0.570	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[8, 9]							
t_{DIB}	Output Data Invalid Before CLK Output	MachXO3L/LF devices, top side only	—	0.160	—	0.180	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_TX.ECLK.Centered[10, 11, 12]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3L/LF devices, top side only	0.200	—	0.200	—	UI
t_{DVA}	Output Data Valid After CLK Output		0.200	—	0.200	—	UI
f_{DATA}[14]	MIPI D-PHY Output Data Speed		—	900	—	900	Mbps
f_{DDRX4}[14]	MIPI D-PHY ECLK Frequency (minimum limited by PLL)		—	450	—	450	MHz
f_{SCLK}[14]	SCLK Frequency		—	112.5	—	112.5	MHz

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
5. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
6. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
7. This number for general purpose usage. Duty cycle tolerance is +/–10%.
8. Duty cycle is +/– 5% for system usage.
9. Performance is calculated with 0.225 UI.
10. Performance is calculated with 0.20 UI.
11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.
12. Performance for Industrial devices and –5 devices are not modeled in the Diamond design tool.
13. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
14. Above 800 Mbps is only supported with WLCSP and csfBGA packages
15. Between 800 Mbps to 900 Mbps:
    a. VIDTH exceeds the MIPI D-PHY Input DC Conditions Table 3-4 and can be calculated with the equation tSU or tH = -0.0005*VIDTH + 0.3284
    b. Example calculations
        i. tSU and tHO = 0.28 with VIDTH = 100 mV
        ii. tSU and tHO = 0.25 with VIDTH = 170 mV
        iii. tSU and tHO = 0.20 with VIDTH = 270 mV

JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-8. JTAG Port Timing Waveforms



Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3L-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND

MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-5MG121I	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-5MG121I	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-6MG121I	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300C-5BG256C	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-6BG256C	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-5BG256I	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-1300C-6BG256I	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-6MG121I	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND