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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	335
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-4300c-5bg400c

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Table 1-1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900	9400
Distributed R/	AM (kbits)	5	10	16	34	54	73
EBR SRAM (I	kbits)	64	64	74	92	240	432
Number of PL	Ls	1	1	1	2	2	2
Hardened	l ² C	2	2	2	2	2	2
Functions:	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY S	Support	Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Pro	ogrammable	MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400
Packages				ΙΟ			
36-ball WLCSP ¹ (2.5 mm x 2.5 mm, 0.4 mm)			28				
49-ball WLCSP ¹ (3.2 mm x 3.2 mm, 0.4 mm)				38			
81-ball WLCSP ¹ (3.8 mm x 3.8 mm, 0.4 mm)					63		
121-ball csfBGA ¹ (6 mm x 6 mm, 0.5 mm)		100	100	100	100		
256-ball csfB (9 mm x 9 mn	GA ¹ n, 0.5 mm)		206	206	206	206	206
324-ball csfB (10 mm x 10	GA ¹ mm, 0.5 mm)		2	268	268	281	
256-ball caBGA ² (14 mm x 14 mm, 0.8 mm)			206	206	206	206	206
324-ball caBC (15 mm x 15 i	àA² mm, 0.8 mm)			279	279	279	
400-ball caB0 (17 mm x 17 i	àA² mm, 0.8 mm)				335	335	335
484-ball caBC (19 mm x 19	3A² mm, 0.8 mm)						384

1. Package is only available for E=1.2 V devices.

2. Package is only available for C=2.5 V/3.3 V devices.

Introduction

MachXO3[™] device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I²C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs



MachXO3 Family Data Sheet Architecture

February 2017

Advance Data Sheet DS1047

Architecture Overview

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK[™] PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.





Notes:

MachXO3L/LF-640 is similar to MachXO3L/LF-1300. MachXO3L/LF-640 has a lower LUT count.

MachXO3L devices have NVCM, MachXO3LF devices have Flash.

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 MachXO3L/LF-1300, MachXO3L/LF-2100, MachXO3L/LF-6900 and MachXO3L/LF-9400 are similar to MachXO3L/LF-4300. MachXO3L/LF-1300 has a lower LUT count, one PLL, and seven EBR blocks. MachXO3L/LF-2100 has a lower LUT count, one PLL, and eight EBR blocks. MachXO3L/LF-6900 has a higher LUT count, two PLLs, and 26 EBR blocks. MachXO3L/LF-9400 has a higher LUT count, two PLLs, and 48 EBR blocks.

• MachXO3L devices have NVCM, MachXO3LF devices have Flash.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO3L/LF family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO3L/LF registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO3L/LF architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. These blocks are located at the ends of the on-chip NVCM/Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO3L/LF devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter.

MachXO3LF devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO3L/LF devices are available for operation from 3.3 V, 2.5 V and 1.2 V power sup-plies, providing easy integration into the overall system.



Figure 2-5. Primary Clocks for MachXO3L/LF Devices



Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO3L/LF External Switching Characteristics table.



state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-9. Memory Core Reset



For further information on the sysMEM EBR block, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram

Reset	
Clock	
Clock	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f_{MAX} (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.



If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1290, Memory Usage Guide for MachXO3 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO3L/LF devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO3L/LF devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

All PIO pairs can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these devices have on-chip differential termination and also provide PCI support.



Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-12 shows the output register block on the left, top and bottom edges.

Figure 2-12. MachXO3L/LF Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.



Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-13 shows a block diagram of the input gearbox.



Figure 2-15. MachXO3L/LF-1300 in 256 Ball Packages, MachXO3L/LF-2100, MachXO3L/LF-4300, MachXO3L/LF-6900 and MachXO3L/LF-9400 Banks



Figure 2-16. MachXO3L/LF-640 and MachXO3L/LF-1300 Banks





Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-13 lists all the available MCLK frequencies.

Table 2-13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133



Figure 2-18. PC Core Block Diagram



Table 2-14 describes the signals interfacing with the I²C cores.

 Table 2-14. PC Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I ² C core. The signal is an output if the I ² C core is in master mode. The signal is an input if the I ² C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO3L/LF device.
i2c_sda	Bi-directional	Bi-directional data line of the l^2C core. The signal is an output when data is transmitted from the l^2C core. The signal is an input when data is received into the l^2C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of l^2C ports in each MachXO3L/LF device.
i2c_irqo	Output	Interrupt request output signal of the I ² C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I ² C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.

Hardened SPI IP Core

Every MachXO3L/LF device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO3L/LF devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface



There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1293, Using Hardened Control Functions in MachXO3 Devices

Figure 2-19. SPI Core Block Diagram



Table 2-15 describes the signals interfacing with the SPI cores.

Table 2-15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	0	Master	SPI master chip-select output
spi_csn[17]	0	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	0	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Con- figuration Logic.
cfg_stdby	0	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.
cfg_wake	0	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.



For more details on these embedded functions, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

User Flash Memory (UFM)

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

Standby Mode and Power Saving Options

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the E devices operate at 1.2 V V_{CC}.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I²C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned "off" or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.



sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V V	Input Voltage	V _{CCIO} = 3.3 V	0	_	2.605	V
VINP VINM		V _{CCIO} = 2.5 V	0	_	2.05	V
V _{THD}	Differential Input Threshold		±100	_		mV
V	Input Common Mode Voltage	V _{CCIO} = 3.3 V	0.05	_	2.6	V
V ^{CM}	Input Common Mode Voltage	V _{CCIO} = 2.5 V	0.05	_	2.0	V
I _{IN}	Input current	Power on	_	_	±10	μA
V _{OH}	Output high voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.375	_	V
V _{OL}	Output low voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.90	1.025	_	V
V _{OD}	Output voltage differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} between high and low		_	_	50	mV
V _{OS}	Output voltage offset	(V _{OP} - V _{OM})/2, R _T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V _{OS} between H and L		—	—	50	mV
IOSD	Output short circuit current	V _{OD} = 0 V driver outputs shorted	_	_	24	mA

Over Recommended Operating Conditions



LVPECL

The MachXO3L/LF family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL



Table 3-3. LVPECL DC Conditions¹

Symbol	Description	Nominal	Units
Z _{OUT}	Output impedance	20	Ohms
R _S	Driver series resistor	93	Ohms
R _P	Driver parallel resistor	196	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	2.05	V
V _{OL}	Output low voltage	1.25	V
V _{OD}	Output differential voltage	0.80	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	100.5	Ohms
I _{DC}	DC output current	12.11	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.



Table 3-5. MIPI D-PHY Output DC Conditions¹

	Description	Min.	Тур.	Max.	Units
Transmitter	· · ·			•	
External Termination	on				
RL	1% external resistor with VCCIO = 2.5 V		50		Ohms
	1% external resistor with VCCIO = 3.3 V	—	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	_	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	_	464	—	Ohms
High Speed	· ·				
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	_	2.5	_	V
	VCCIO of the Bank with LVDS Emulated output buffer	_	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage	_	—	360	V
ZOS	Single ended output impedance		50	_	Ohms
ΔZOS	Single ended output impedance mismatch		—	10	%
Low Power	· · · ·				
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	_	1.2	_	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	-50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

1. Over Recommended Operating Conditions



DC and Switching Characteristics MachXO3 Family Data Sheet

Parameter Description Device Min. Max. Min. Max. L General I/O Pin Parameters (Using Edge Clock without PLL)
General I/O Pin Parameters (Using Edge Clock without PLL) t _{COE} MachXO3L/LF-1300 - 7.53 - 7.76 MachXO3L/LF-2100 - 7.53 - 7.76 MachXO3L/LF-2100 - 7.45 - 7.68 MachXO3L/LF-6900 - 7.53 - 7.76 MachXO3L/LF-9400 - 8.93 - 9.35 MachXO3L/LF-1300 -0.19 - - 0.19 -
MachXO3L/LF-1300 - 7.53 - 7.76 t _{COE} Clock to Output - PIO Output Register MachXO3L/LF-2100 - 7.53 - 7.76 MachXO3L/LF-2100 - 7.45 - 7.68 MachXO3L/LF-6900 - 7.53 - 7.76 MachXO3L/LF-9400 - 8.93 - 9.35 MachXO3L/LF-1300 -0.19 - - 0.19 -
MachXO3L/LF-2100 — 7.53 — 7.76 Clock to Output - PIO Output Register MachXO3L/LF-4300 — 7.45 — 7.68 MachXO3L/LF-6900 — 7.53 — 7.76 MachXO3L/LF-9400 — 8.93 — 9.35 MachXO3L/LF-1300 -0.19 — -0.19 —
t _{COE} Clock to Output - PIO Output Register MachXO3L/LF-4300 7.45 7.68 MachXO3L/LF-6900 7.53 7.76 MachXO3L/LF-9400 8.93 9.35 MachXO3L/LF-1300 -0.19 -0.19
MachXO3L/LF-6900 — 7.53 — 7.76 MachXO3L/LF-9400 — 8.93 — 9.35 MachXO3L/LF-1300 -0.19 — -0.19 —
MachXO3L/LF-9400 — 8.93 — 9.35 MachXO3L/LF-1300 -0.19 — -0.19 —
MachXO3L/LF-1300 -0.190.19 -
MachXO3L/LF-2100 -0.190.19 -
t _{SUE} Clock to Data Setup - PIO Input Register MachXO3L/LF-4300 -0.160.16 -
MachXO3L/LF-6900 -0.190.19 -
MachXO3L/LF-9400 -0.200.20 -
MachXO3L/LF-1300 1.97 — 2.24 —
MachXO3L/LF-2100 1.97 — 2.24 —
t _{HE} Clock to Data Hold - PIO Input Register MachXO3L/LF-4300 1.89 - 2.16 -
MachXO3L/LF-6900 1.97 — 2.24 —
MachXO3L/LF-9400 1.98 — 2.25 —
MachXO3L/LF-1300 1.56 — 1.69 —
MachXO3L/LF-2100 1.56 — 1.69 —
tsu DELE with Data laput Dalay
MachXO3L/LF-6900 1.66 — 1.81 —
MachXO3L/LF-9400 1.71 — 1.85 —
MachXO3L/LF-1300 -0.230.23 -
MachXO3L/LF-2100 -0.230.23 -
tH DELE Input Data Hold - PIO Input Register with MachXO3L/LF-4300 -0.340.34 -
MachXO3L/LF-6900 -0.290.29 -
MachXO3L/LF-9400 -0.300.30 -
General I/O Pin Parameters (Using Primary Clock with PLL)
MachXO3L/LF-1300 — 5.98 — 6.01
MachXO3L/LF-2100 — 5.98 — 6.01
t _{COPL1} Clock to Output - PIO Output Register MachXO3L/LF-4300 — 5.99 — 6.02
MachXO3L/LF-6900 — 6.02 — 6.06
MachXO3L/LF-9400 — 5.55 — 6.13
MachXO3L/LF-1300 0.36 — 0.36 —
MachXO3L/LF-2100 0.36 — 0.36 —
t _{SUPU} Clock to Data Setup - PIO Input Register MachXO3L/LF-4300 0.35 — 0.35 —
MachXO3L/LF-6900 0.34 — 0.34 —
MachXO3L/LF-9400 0.33 — 0.33 —
MachXO3L/LF-1300 0.42 — 0.49 —
MachXO3L/LF-2100 0.42 — 0.49 —
t _{HPL1} Clock to Data Hold - PIO Input Register MachXO3L/LF-4300 0.43 - 0.50 -
MachXO3L/LF-6900 0.46 — 0.54 —
MachXO3L/LF-9400 0.47 — 0.55 —



DC and Switching Characteristics MachXO3 Family Data Sheet

			-	-6		-5	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	2.87		3.18		ns
		MachXO3L/LF-2100	2.87		3.18	—	ns
t _{SU_DELPLL}		MachXO3L/LF-4300	2.96		3.28		ns
		MachXO3L/LF-6900	3.05		3.35		ns
		MachXO3L/LF-9400	3.06		3.37		ns
	Clock to Data Hold - PIO Input Register with	MachXO3L/LF-1300	-0.83		-0.83		ns
^t H_DELPLL		MachXO3L/LF-2100	-0.83		-0.83		ns
		MachXO3L/LF-4300	-0.87		-0.87		ns
		MachXO3L/LF-6900	-0.91		-0.91	—	ns
		MachXO3L/LF-9400	-0.93	—	-0.93		ns



LCMXO3L-9400C-6BG484I

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND
	I			Γ	I	I
Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-5BG4001	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND

2.5 V/3.3 V

6

Halogen-Free caBGA

484

IND

9400



MachXO3 Family Data Sheet Revision History

February 2017

Advance Data Sheet DS1047

Date	Version	Section	Change Summary
February 2017 1.8	1.8	Architecture	Updated Supported Standards section. Corrected "MDVS" to "MLDVS" in Table 2-11, Supported Input Standards.
		DC and Switching Characteristics	Updated ESD Performance section. Added reference to the MachXO2 Product Family Qualification Summary document.
			Updated Static Supply Current – C/E Devices section. Added footnote 7.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. — Populated values for MachXO3L/LF-9400. — Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, corrected "t _{DVB} " to "t _{DIB} " and "t _{DVA} " to "t _{DIA} " and revised their descriptions. — Added Figure 3-6, Receiver GDDR71_RX Waveforms and Figure 3-7, Transmitter GDDR71_TX Waveforms.
		Pinout Information	Updated the Pin Information Summary section. Added MachXO3L/LF- 9600C packages.
May 2016 1.7 DC and S Charact		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Modified I/O Tri-state Volt- age Applied and Dedicated Input Voltage Applied footnotes.
			Updated sysIO Recommended Operating Conditions section. — Added standards. — Added V _{REF} (V) — Added footnote 4.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Added I/O standards.
		Ordering Information	Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.

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