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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	63
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	81-UFBGA, WLCSP
Supplier Device Package	81-WLCSP (3.80x3.69)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-4300e-5uwg81itr50">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-4300e-5uwg81itr50</a>

and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO3L/LF devices are available in two versions C and E with two speed grades: -5 and -6, with -6 being the fastest. C devices have an internal linear voltage regulator which supports external VCC supply voltages of 3.3 V or 2.5 V. E devices only accept 1.2 V as the external VCC supply voltage. With the exception of power supply voltage both C and E are functionally compatible with each other.

The MachXO3L/LF PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 x 2.5 mm WLCSP to the 19 x 19 mm caBGA. MachXO3L/LF devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The MachXO3L/LF devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

A user-programmable internal oscillator is included in MachXO3L/LF devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO3L/LF devices also provide flexible, reliable and secure configuration from on-chip NVCM/Flash. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I<sup>2</sup>C port. Additionally, MachXO3L/LF devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

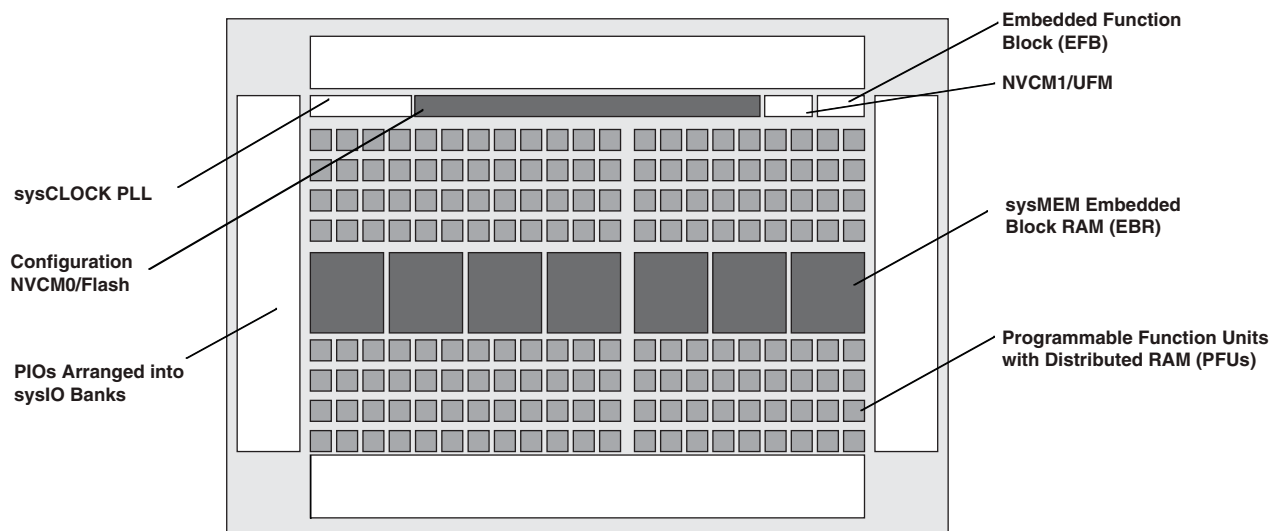
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO3L/LF family of devices. Popular logic synthesis tools provide synthesis library support for MachXO3L/LF. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO3L/LF device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO3L/LF PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

## Architecture Overview

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

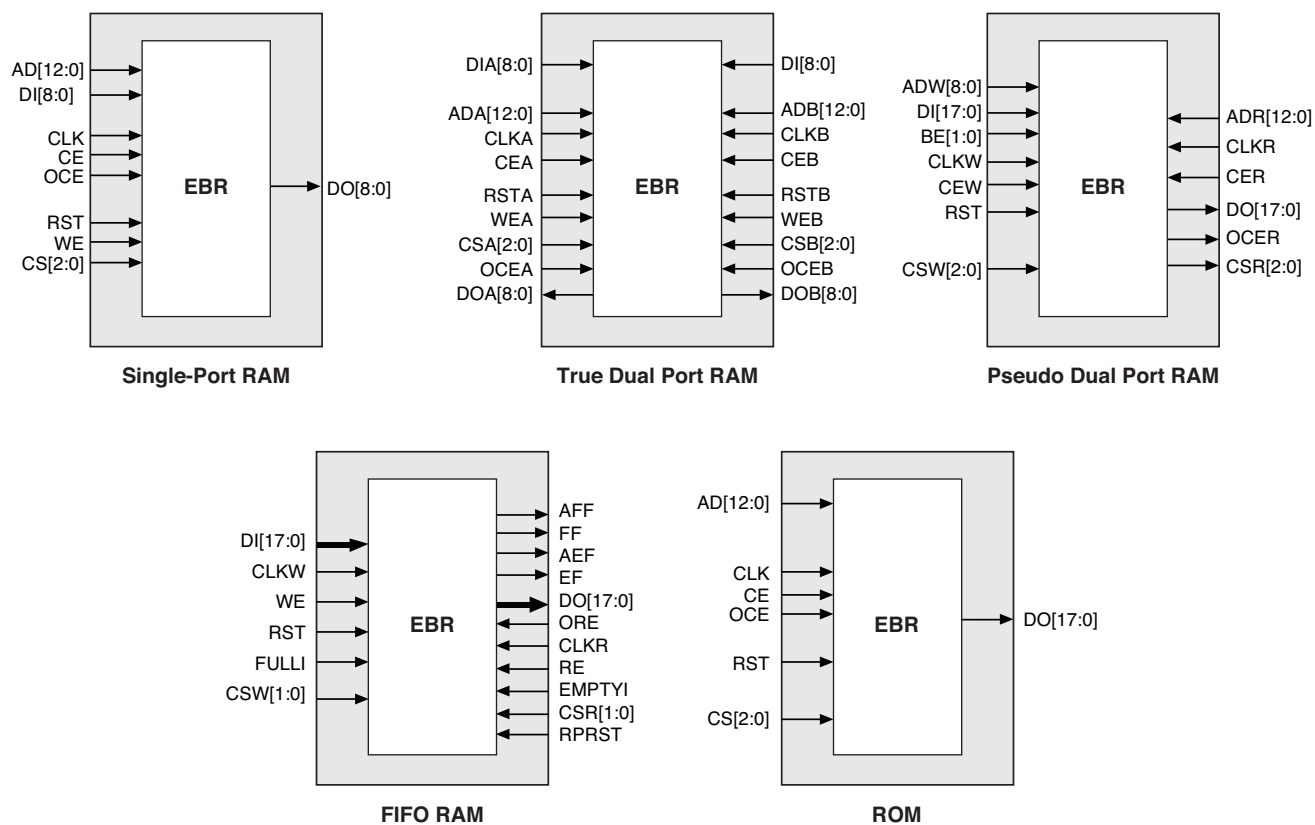
**Figure 2-1. Top View of the MachXO3L/LF-1300 Device**



**Notes:**

- MachXO3L/LF-640 is similar to MachXO3L/LF-1300. MachXO3L/LF-640 has a lower LUT count.
- MachXO3L devices have NVCM, MachXO3LF devices have Flash.

**Figure 2-8. sysMEM Memory Primitives**

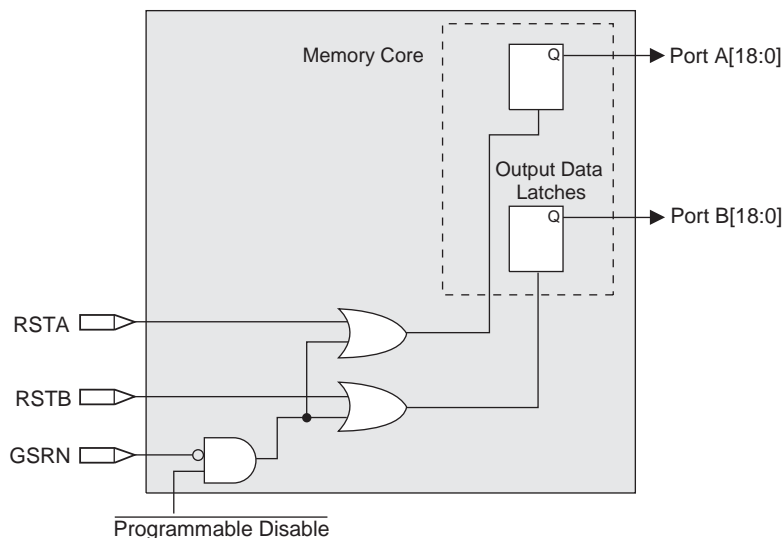


state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

### Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

**Figure 2-9. Memory Core Reset**

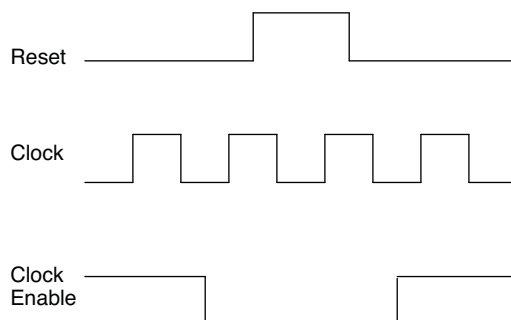


For further information on the sysMEM EBR block, please refer to TN1290, [Memory Usage Guide for MachXO3 Devices](#).

### EBR Asynchronous Reset

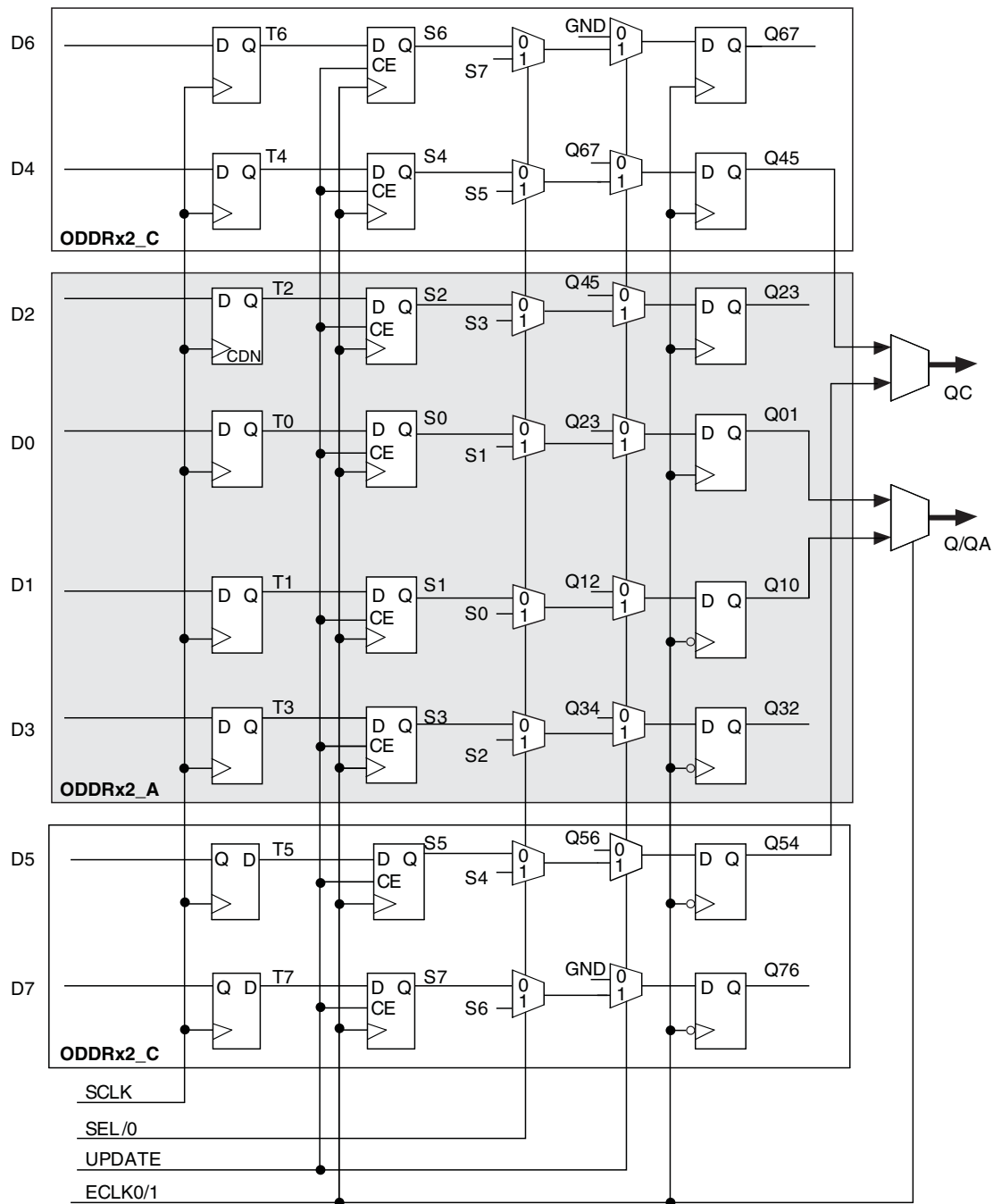
EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

**Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram**



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of  $1/t_{MAX}$  (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

Figure 2-14. Output Gearbox



More information on the output gearbox is available in TN1281, [Implementing High-Speed Interfaces with MachXO3 Devices](#).

**Table 2-12. Supported Output Standards**

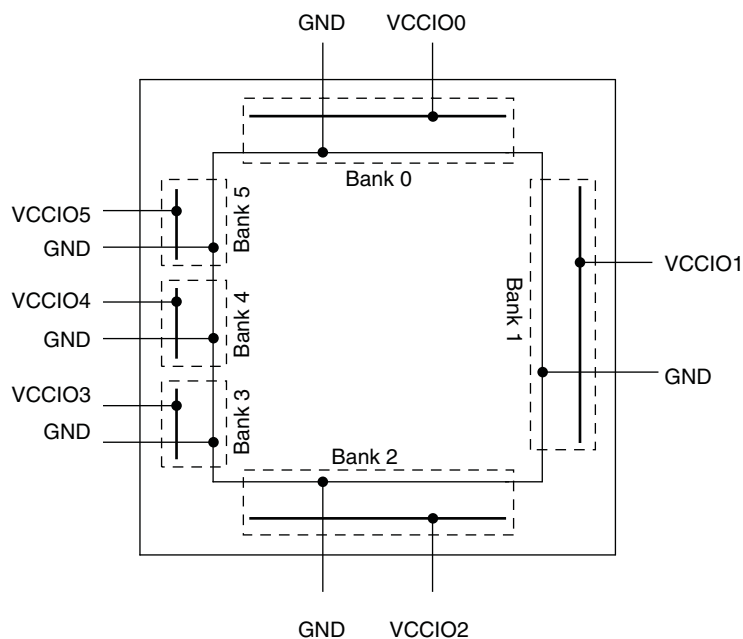
Output Standard	V <sub>CCIO</sub> (Typ.)
<b>Single-Ended Interfaces</b>	
LVTTL	3.3
LVC MOS33	3.3
LVC MOS25	2.5
LVC MOS18	1.8
LVC MOS15	1.5
LVC MOS12	1.2
LVC MOS33, Open Drain	—
LVC MOS25, Open Drain	—
LVC MOS18, Open Drain	—
LVC MOS15, Open Drain	—
LVC MOS12, Open Drain	—
PCI33	3.3
<b>Differential Interfaces</b>	
LVDS <sup>1</sup>	2.5, 3.3
BLVDS, MLVDS, RSDS <sup>1</sup>	2.5
LVPECL <sup>1</sup>	3.3
MIPI <sup>1</sup>	2.5
LVTTL D	3.3
LVC MOS33D	3.3
LVC MOS25D	2.5
LVC MOS18D	1.8

1. These interfaces can be emulated with external resistors in all devices.

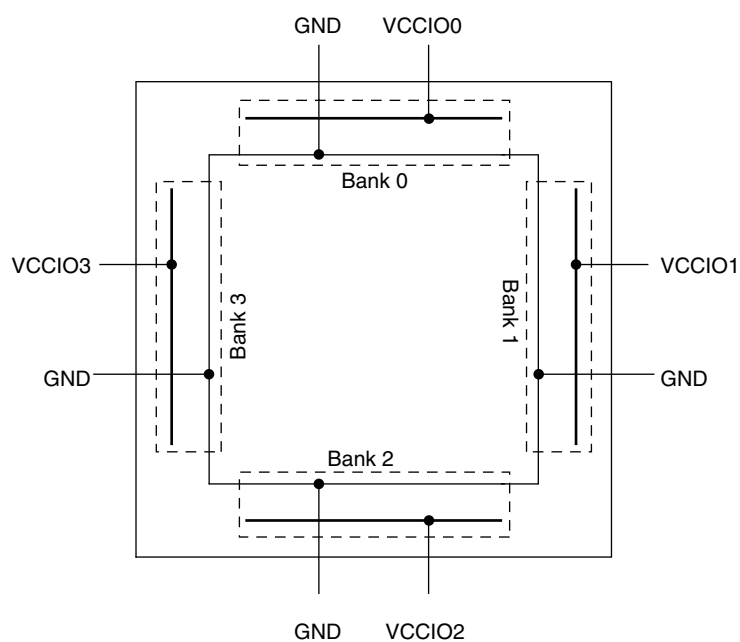
## sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO3L/LF-1300 in the 256 Ball packages and the MachXO3L/LF-2100 and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO3L/LF-1300 and lower density devices have four banks (one bank per side). Figures 2-15 and 2-16 show the sysIO banks and their associated supplies for all devices.

**Figure 2-15. MachXO3L/LF-1300 in 256 Ball Packages, MachXO3L/LF-2100, MachXO3L/LF-4300, MachXO3L/LF-6900 and MachXO3L/LF-9400 Banks**



**Figure 2-16. MachXO3L/LF-640 and MachXO3L/LF-1300 Banks**





## Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

## On-chip Oscillator

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-13 lists all the available MCLK frequencies.

**Table 2-13. Available MCLK Frequencies**

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) (Appendix B)
- TN1293, [Using Hardened Control Functions in MachXO3 Devices](#)

**Figure 2-19. SPI Core Block Diagram**

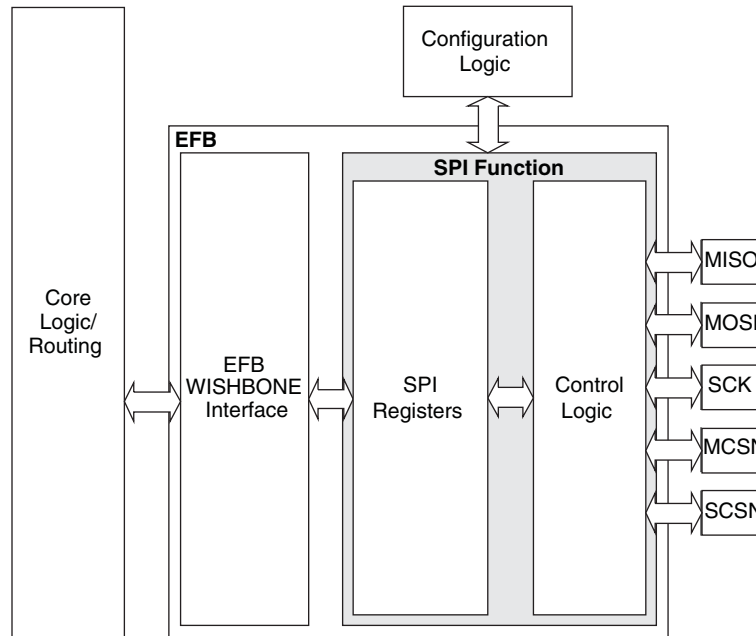


Table 2-15 describes the signals interfacing with the SPI cores.

**Table 2-15. SPI Core Signal Description**

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Configuration Logic.
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

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## Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V<sub>CCIO</sub> Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

### Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

1. Internal NVCM/Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, [MachXO3 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, [MachXO3 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, [MachXO3 Programming and Configuration Usage Guide](#).

### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

## sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

### LVDS

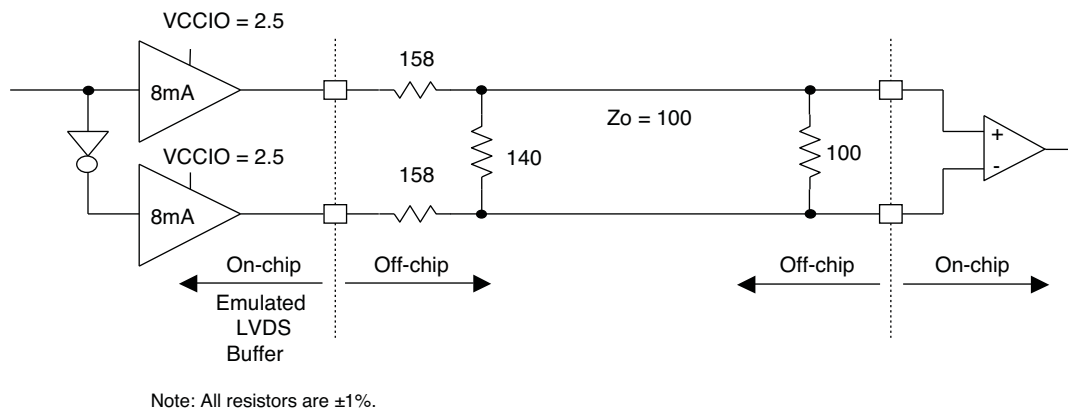
#### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}$ $V_{INM}$	Input Voltage	$V_{CCIO} = 3.3\text{ V}$	0	—	2.605	V
		$V_{CCIO} = 2.5\text{ V}$	0	—	2.05	V
$V_{THD}$	Differential Input Threshold		$\pm 100$	—		mV
$V_{CM}$	Input Common Mode Voltage	$V_{CCIO} = 3.3\text{ V}$	0.05	—	2.6	V
		$V_{CCIO} = 2.5\text{ V}$	0.05	—	2.0	V
$I_{IN}$	Input current	Power on	—	—	$\pm 10$	$\mu\text{A}$
$V_{OH}$	Output high voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\text{ Ohm}$	—	1.375	—	V
$V_{OL}$	Output low voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\text{ Ohm}$	0.90	1.025	—	V
$V_{OD}$	Output voltage differential	$(V_{OP} - V_{OM})$ , $R_T = 100\text{ Ohm}$	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between high and low		—	—	50	mV
$V_{OS}$	Output voltage offset	$(V_{OP} - V_{OM})/2$ , $R_T = 100\text{ Ohm}$	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in $V_{OS}$ between H and L		—	—	50	mV
$I_{OSD}$	Output short circuit current	$V_{OD} = 0\text{ V}$ driver outputs shorted	—	—	24	mA

### LVDS Emulation

MachXO3L/LF devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVC MOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

**Figure 3-1. LVDS Using External Resistors (LVDS25E)**



**Table 3-1. LVDS25E DC Conditions**

#### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	158	Ohms
$R_P$	Driver parallel resistor	140	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.35	V
$V_{CM}$	Output common mode voltage	1.25	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	6.03	mA

**Table 3-5. MIPI D-PHY Output DC Conditions<sup>1</sup>**

	Description	Min.	Typ.	Max.	Units
<b>Transmitter</b>					
<b>External Termination</b>					
RL	1% external resistor with VCCIO = 2.5 V	—	50	—	Ohms
	1% external resistor with VCCIO = 3.3 V	—	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	—	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	—	464	—	Ohms
<b>High Speed</b>					
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	—	2.5	—	V
	VCCIO of the Bank with LVDS Emulated output buffer	—	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage	—	—	360	V
ZOS	Single ended output impedance	—	50	—	Ohms
ΔZOS	Single ended output impedance mismatch	—	—	10	%
<b>Low Power</b>					
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	—	1.2	—	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	–50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

<sup>1</sup>. Over Recommended Operating Conditions

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned <sup>8,9</sup>							
t <sub>DVA</sub>	Input Data Valid After CLK	All MachXO3L/LF devices, all sides	—	0.317	—	0.344	UI
t <sub>DVE</sub>	Input Data Hold After CLK		0.742	—	0.702	—	UI
f <sub>DATA</sub>	DDRX1 Input Data Speed		—	300	—	250	Mbps
f <sub>DDR1</sub>	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered <sup>8,9</sup>							
t <sub>SU</sub>	Input Data Setup Before CLK	All MachXO3L/LF devices, all sides	0.566	—	0.560	—	ns
t <sub>HO</sub>	Input Data Hold After CLK		0.778	—	0.879	—	ns
f <sub>DATA</sub>	DDRX1 Input Data Speed		—	300	—		Mbps
f <sub>DDR1</sub>	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned <sup>8,9</sup>							
t <sub>DVA</sub>	Input Data Valid After CLK	MachXO3L/LF devices, bottom side only	—	0.316	—	0.342	UI
t <sub>DVE</sub>	Input Data Hold After CLK		0.710	—	0.675	—	UI
f <sub>DATA</sub>	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f <sub>DDR2</sub>	DDRX2 ECLK Frequency		—	332	—	277	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered <sup>8,9</sup>							
t <sub>SU</sub>	Input Data Setup Before CLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t <sub>HO</sub>	Input Data Hold After CLK		0.287	—	0.287	—	ns
f <sub>DATA</sub>	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f <sub>DDR2</sub>	DDRX2 ECLK Frequency		—	332	—	277	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	166	—	139	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Aligned <sup>8</sup>							
t <sub>DVA</sub>	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.307	—	0.320	UI
t <sub>DVE</sub>	Input Data Hold After ECLK		0.782	—	0.699	—	UI
f <sub>DATA</sub>	DDR4 Serial Input Data Speed		—	800	—	630	Mbps
f <sub>DDR4</sub>	DDR4 ECLK Frequency		—	400	—	315	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	100	—	79	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Centered <sup>8</sup>							
t <sub>SU</sub>	Input Data Setup Before ECLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t <sub>HO</sub>	Input Data Hold After ECLK		0.287	—	0.287	—	ns
f <sub>DATA</sub>	DDR4 Serial Input Data Speed		—	800	—	630	Mbps
f <sub>DDR4</sub>	DDR4 ECLK Frequency		—	400	—	315	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1) <sup>9</sup>							
t <sub>DVA</sub>	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.290	—	0.320	UI
t <sub>DVE</sub>	Input Data Hold After ECLK		0.739	—	0.699	—	UI
f <sub>DATA</sub>	DDR71 Serial Input Data Speed		—	756	—	630	Mbps
f <sub>DDR71</sub>	DDR71 ECLK Frequency		—	378	—	315	MHz
f <sub>CLKIN</sub>	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz

## Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
<b>Configuration</b> (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I <sup>2</sup> C clock input and master I <sup>2</sup> C clock output.
SDA	I/O	Slave I <sup>2</sup> C data input and master I <sup>2</sup> C data output.



	MachXO3L/LF-2100					
	WLCSP49	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324
<b>General Purpose IO per Bank</b>						
Bank 0	19	24	50	71	50	71
Bank 1	0	26	52	62	52	68
Bank 2	13	26	52	72	52	72
Bank 3	0	7	16	22	16	24
Bank 4	0	7	16	14	16	16
Bank 5	6	10	20	27	20	28
<b>Total General Purpose Single Ended IO</b>	<b>38</b>	<b>100</b>	<b>206</b>	<b>268</b>	<b>206</b>	<b>279</b>
<b>Differential IO per Bank</b>						
Bank 0	10	12	25	36	25	36
Bank 1	0	13	26	30	26	34
Bank 2	6	13	26	36	26	36
Bank 3	0	3	8	10	8	12
Bank 4	0	3	8	6	8	8
Bank 5	3	5	10	13	10	14
<b>Total General Purpose Differential IO</b>	<b>19</b>	<b>49</b>	<b>103</b>	<b>131</b>	<b>103</b>	<b>140</b>
<b>Dual Function IO</b>	<b>25</b>	<b>33</b>	<b>33</b>	<b>37</b>	<b>33</b>	<b>37</b>
<b>Number 7:1 or 8:1 Gearboxes</b>						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18
<b>High-speed Differential Outputs</b>						
Bank 0	5	7	14	18	14	18
<b>VCCIO Pins</b>						
Bank 0	2	1	4	4	4	4
Bank 1	0	1	3	4	4	4
Bank 2	1	1	4	4	4	4
Bank 3	0	1	2	2	1	2
Bank 4	0	1	2	2	2	2
Bank 5	1	1	2	2	1	2
<b>VCC</b>	<b>2</b>	<b>4</b>	<b>8</b>	<b>8</b>	<b>8</b>	<b>10</b>
<b>GND</b>	<b>4</b>	<b>10</b>	<b>24</b>	<b>16</b>	<b>24</b>	<b>16</b>
<b>NC</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>13</b>	<b>1</b>	<b>0</b>
<b>Reserved for Configuration</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>
<b>Total Count of Bonded Pins</b>	<b>49</b>	<b>121</b>	<b>256</b>	<b>324</b>	<b>256</b>	<b>324</b>

	MachXO3L/LF-4300						
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
<b>General Purpose IO per Bank</b>							
Bank 0	29	24	50	71	50	71	83
Bank 1	0	26	52	62	52	68	84
Bank 2	20	26	52	72	52	72	84
Bank 3	7	7	16	22	16	24	28
Bank 4	0	7	16	14	16	16	24
Bank 5	7	10	20	27	20	28	32
<b>Total General Purpose Single Ended IO</b>	63	100	206	268	206	279	335
<b>Differential IO per Bank</b>							
Bank 0	15	12	25	36	25	36	42
Bank 1	0	13	26	30	26	34	42
Bank 2	10	13	26	36	26	36	42
Bank 3	3	3	8	10	8	12	14
Bank 4	0	3	8	6	8	8	12
Bank 5	3	5	10	13	10	14	16
<b>Total General Purpose Differential IO</b>	31	49	103	131	103	140	168
<b>Dual Function IO</b>	25	37	37	37	37	37	37
<b>Number 7:1 or 8:1 Gearboxes</b>							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21
<b>High-speed Differential Outputs</b>							
Bank 0	10	7	18	18	18	18	21
<b>VCCIO Pins</b>							
Bank 0	3	1	4	4	4	4	5
Bank 1	0	1	3	4	4	4	5
Bank 2	2	1	4	4	4	4	5
Bank 3	1	1	2	2	1	2	2
Bank 4	0	1	2	2	2	2	2
Bank 5	1	1	2	2	1	2	2
<b>VCC</b>	4	4	8	8	8	10	10
<b>GND</b>	6	10	24	16	24	16	33
<b>NC</b>	0	0	0	13	1	0	0
<b>Reserved for Configuration</b>	1	1	1	1	1	1	1
<b>Total Count of Bonded Pins</b>	<b>81</b>	<b>121</b>	<b>256</b>	<b>324</b>	<b>256</b>	<b>324</b>	<b>400</b>

	MachXO3L/LF-9400C			
	CSFBGA256	CABGA256	CABGA400	CABGA484
<b>General Purpose IO per Bank</b>				
Bank 0	50	50	83	95
Bank 1	52	52	84	96
Bank 2	52	52	84	96
Bank 3	16	16	28	36
Bank 4	16	16	24	24
Bank 5	20	20	32	36
<b>Total General Purpose Single Ended IO</b>	<b>206</b>	<b>206</b>	<b>335</b>	<b>383</b>
<b>Differential IO per Bank</b>				
Bank 0	25	25	42	48
Bank 1	26	26	42	48
Bank 2	26	26	42	48
Bank 3	8	8	14	18
Bank 4	8	8	12	12
Bank 5	10	10	16	18
<b>Total General Purpose Differential IO</b>	<b>103</b>	<b>103</b>	<b>168</b>	<b>192</b>
<b>Dual Function IO</b>	<b>37</b>	<b>37</b>	<b>37</b>	<b>45</b>
<b>Number 7:1 or 8:1 Gearboxes</b>				
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	20	22	24
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	20	22	24
<b>High-speed Differential Outputs</b>				
Bank 0	20	20	21	24
<b>VCCIO Pins</b>				
Bank 0	4	4	5	9
Bank 1	3	4	5	9
Bank 2	4	4	5	9
Bank 3	2	1	2	3
Bank 4	2	2	2	3
Bank 5	2	1	2	3
<b>VCC</b>	<b>8</b>	<b>8</b>	<b>10</b>	<b>12</b>
<b>GND</b>	<b>24</b>	<b>24</b>	<b>33</b>	<b>52</b>
<b>NC</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>0</b>
<b>Reserved for Configuration</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>
<b>Total Count of Bonded Pins</b>	<b>256</b>	<b>256</b>	<b>400</b>	<b>484</b>

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Date	Version	Section	Change Summary
April 2016	1.6	Introduction	Updated Features section. — Revised logic density range and IO to LUT ratio under Flexible Architecture. — Revised 0.8 mm pitch information under Advanced Packaging. — Added MachXO3L-9400/MachXO3LF-9400 information to Table 1-1, MachXO3L/LF Family Selection Guide.
			Updated Introduction section. — Changed density from 6900 to 9400 LUTs. — Changed caBGA packaging to 19 x 19 mm.
		Architecture	Updated Architecture Overview section. — Changed statement to “All logic density devices in this family...” — Updated Figure 2-2 heading and notes.
			Updated sysCLOCK Phase Locked Loops (PLLs) section. — Changed statement to “All MachXO3L/LF devices have one or more sysCLOCK PLL.”
			Updated Programmable I/O Cells (PIC) section. — Changed statement to “All PIO pairs can implement differential receivers.”
			Updated sysIO Buffer Banks section. Updated Figure 2-5 heading.
			Updated Device Configuration section. Added Password and Soft Error Correction.
		DC and Switching Characteristics	Updated Static Supply Current – C/E Devices section. Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices.
			Updated Programming and Erase Supply Current – C/E Devices section. — Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices. — Changed LCMXO3L/LF-640E and LCMXO3L/LF-1300E Typ. values.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. Added MachXO3L/LF-9400 devices.
			Updated NVCM/Flash Download Time section. Added LCMXO3L/LF-9400C device.
			Updated sysCONFIG Port Timing Specifications section. — Added LCMXO3L/LF-9400C device. — Changed $t_{INITL}$ units to from ns to us. — Changed $t_{DPPINIT}$ and $t_{DPPDONE}$ Max. values are per PCN#03A-16.
		Pinout Information	Updated Pin Information Summary section. Added LCMXO3L/LF-9400C device.
		Ordering Information	Updated MachXO3 Part Number Description section. — Added 9400 = 9400 LUTs. — Added BG484 package.
			Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.