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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	121-VFBGA, CSPBGA
Supplier Device Package	121-CSFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-4300e-6mg121c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Table 1-1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400	
LUTs		640	1300	2100	4300	6900	9400	
Distributed RAM (kbits)		5	10	16	34	54	73	
EBR SRAM (I	kbits)	64	64	74	92	240	432	
Number of PL	Ls	1	1	1	2 2 2 2		2	
Hardened	l ² C	2	2	2	2	2	2	
Functions:	SPI	1	1	1	1	1	1	
	Timer/Counter	1	1	1	1	1	1	
	Oscillator	1	1	1	1	1	1	
MIPI D-PHY S	Support	Yes	Yes	Yes	Yes	Yes	Yes	
Multi Time Pro	ogrammable	MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400	
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400	
Packages				ΙΟ				
36-ball WLCSP ¹ (2.5 mm x 2.5 mm, 0.4 mm)			28					
49-ball WLCSP ¹ (3.2 mm x 3.2 mm, 0.4 mm)				38				
81-ball WLCSP ¹ (3.8 mm x 3.8 mm, 0.4 mm)					63			
121-ball csfBGA ¹ (6 mm x 6 mm, 0.5 mm)		100	100	100	100			
256-ball csfB (9 mm x 9 mn	GA ¹ n, 0.5 mm)		206	206	206	206	206	
324-ball csfB (10 mm x 10	GA ¹ mm, 0.5 mm)		2	268	268	281		
256-ball caBGA ² (14 mm x 14 mm, 0.8 mm)			206	206	206	206	206	
324-ball caBC (15 mm x 15 i	àA² mm, 0.8 mm)			279	279	279		
400-ball caB0 (17 mm x 17 i	àA² mm, 0.8 mm)				335	335	335	
484-ball caBC (19 mm x 19	3A² mm, 0.8 mm)						384	

1. Package is only available for E=1.2 V devices.

2. Package is only available for C=2.5 V/3.3 V devices.

Introduction

MachXO3[™] device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I²C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs







 MachXO3L/LF-1300, MachXO3L/LF-2100, MachXO3L/LF-6900 and MachXO3L/LF-9400 are similar to MachXO3L/LF-4300. MachXO3L/LF-1300 has a lower LUT count, one PLL, and seven EBR blocks. MachXO3L/LF-2100 has a lower LUT count, one PLL, and eight EBR blocks. MachXO3L/LF-6900 has a higher LUT count, two PLLs, and 26 EBR blocks. MachXO3L/LF-9400 has a higher LUT count, two PLLs, and 48 EBR blocks.

• MachXO3L devices have NVCM, MachXO3LF devices have Flash.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO3L/LF family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO3L/LF registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO3L/LF architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. These blocks are located at the ends of the on-chip NVCM/Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO3L/LF devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter.

MachXO3LF devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO3L/LF devices are available for operation from 3.3 V, 2.5 V and 1.2 V power sup-plies, providing easy integration into the overall system.



PFU Blocks

The core of the MachXO3L/LF device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Block Diagram



Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

	PFU Block						
Slice	Resources	Modes					
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM					
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM					
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM					
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM					

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.



ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

Routing

There are many resources provided in the MachXO3L/LF devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO3L/LF device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO3L/LF architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO3L/LF devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3L/LF devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3L/LF External Switching Characteristics table.

Primary clock signals for the MachXO3L/LF-1300 and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sys-CLOCK PLL outputs.



 Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the NVCM or Configuration Flash.

MachXO3LF EBR initialization data can also be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO3LF devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.



state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-9. Memory Core Reset



For further information on the sysMEM EBR block, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram

Reset	
Clock	
Clock	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f_{MAX} (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.



Figure 2-11. Group of Four Programmable I/O Cells





Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-12 shows the output register block on the left, top and bottom edges.

Figure 2-12. MachXO3L/LF Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.



There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1293, Using Hardened Control Functions in MachXO3 Devices

Figure 2-19. SPI Core Block Diagram



Table 2-15 describes the signals interfacing with the SPI cores.

Table 2-15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	0	Master	SPI master chip-select output
spi_csn[17]	0	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	0	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Con- figuration Logic.
cfg_stdby	0	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.
cfg_wake	0	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.



For more details on these embedded functions, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

User Flash Memory (UFM)

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

Standby Mode and Power Saving Options

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the E devices operate at 1.2 V V_{CC}.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I²C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned "off" or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.



sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
	Input Voltage	V _{CCIO} = 3.3 V	0	_	2.605	V
VINP VINM		V _{CCIO} = 2.5 V	0	_	2.05	V
V _{THD}	Differential Input Threshold		±100	_		mV
V	Input Common Mode Voltage	V _{CCIO} = 3.3 V	0.05	_	2.6	V
VCM	Input Common Mode Voltage	V _{CCIO} = 2.5 V	0.05	_	2.0	V
I _{IN}	Input current	Power on	_	_	±10	μA
V _{OH}	Output high voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.375	_	V
V _{OL}	Output low voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.90	1.025	_	V
V _{OD}	Output voltage differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} between high and low		_	_	50	mV
V _{OS}	Output voltage offset	(V _{OP} - V _{OM})/2, R _T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V _{OS} between H and L		—	—	50	mV
IOSD	Output short circuit current	V _{OD} = 0 V driver outputs shorted	_	_	24	mA

Over Recommended Operating Conditions



BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example



Table 3-2. BLVDS DC Conditions¹

Over Recommended	Operating	Conditions
	operating	oonantions

		Noi		
Symbol	Description	Zo = 45	Zo = 90	Units
Z _{OUT}	Output impedance	20	20	Ohms
R _S	Driver series resistance	80	80	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.376	1.480	V
V _{OL}	Output low voltage	1.124	1.020	V
V _{OD}	Output differential voltage	0.253	0.459	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.



MIPI D-PHY Emulation

MachXO3L/LF devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed IOs use the LVDS25E buffer and Low Power IOs use the LVCMOS buffers. The scheme shown in Figure 3-4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3-5 is one possible solution for MIPI D-PHY Transmitter implementation.

Figure 3-4. MIPI D-PHY Input Using External Resistors



Table 3-4. MIPI DC Conditions¹

	Description	Min.	Тур.	Max.	Units			
Receiver								
External Terminatio	n							
RT	1% external resistor with VCCIO=2.5 V		50	—	Ohms			
	1% external resistor with VCCIO=3.3 V	—	50	—	Ohms			
High Speed								
VCCIO	VCCIO of the Bank with LVDS Emulated input buffer	—	2.5	—	V			
	VCCIO of the Bank with LVDS Emulated input buffer	—	3.3	—	V			
VCMRX	Common-mode voltage HS receive mode	150	200	250	mV			
VIDTH	Differential input high threshold	—	—	100	mV			
VIDTL	Differential input low threshold	-100	—	—	mV			
VIHHS	Single-ended input high voltage		—	300	mV			
VILHS	Single-ended input low voltage	100	—	—	mV			
ZID	Differential input impedance	80	100	120	Ohms			



	_6 _5					-5		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units	
Generic DDF GDDRX1_RX	RX1 Inputs with Clock and Data Aligned at K.SCLK.Aligned ^{8,9}	Pin Using PCLK Pin for Clo	ock Inpu	t –				
t _{DVA}	Input Data Valid After CLK			0.317	—	0.344	UI	
t _{DVE}	Input Data Hold After CLK	All MachXO3L/LF	0.742		0.702		UI	
f _{DATA}	DDRX1 Input Data Speed	-devices, all sides		300	—	250	Mbps	
f _{DDRX1}	DDRX1 SCLK Frequency			150	—	125	MHz	
Generic DD GDDRX1_R	RX1 Inputs with Clock and Data Centered X.SCLK.Centered ^{8, 9}	at Pin Using PCLK Pin fo	or Clock	Input –		1	1	
t _{SU}	Input Data Setup Before CLK		0.566		0.560		ns	
t _{HO}	Input Data Hold After CLK	All MachXO3L/LF	0.778		0.879		ns	
f _{DATA}	DDRX1 Input Data Speed	-devices, all sides		300	—		Mbps	
f _{DDRX1}	DDRX1 SCLK Frequency		_	150	—	125	MHz	
Generic DD GDDRX2_R	RX2 Inputs with Clock and Data Aligned at X.ECLK.Aligned ^{8, 9}	Pin Using PCLK Pin for C	lock Inp	out –				
t _{DVA}	Input Data Valid After CLK		—	0.316	—	0.342	UI	
t _{DVE}	Input Data Hold After CLK	-	0.710		0.675		UI	
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO3L/LF devices,		664	—	554	Mbps	
f _{DDRX2}	DDRX2 ECLK Frequency	bollom side only		332	—	277	MHz	
f _{SCLK}	SCLK Frequency			166	—	139	MHz	
Generic DD GDDRX2_R	Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input –							
t _{SU}	Input Data Setup Before CLK		0.233		0.219		ns	
t _{HO}	Input Data Hold After CLK	-	0.287	—	0.287		ns	
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO3L/LF devices,		664	—	554	Mbps	
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only		332	—	277	MHz	
f _{SCLK}	SCLK Frequency	-		166	—	139	MHz	
Generic DDI	R4 Inputs with Clock and Data Aligned at P	in Using PCLK Pin for Cloo	k Input	- GDDR	X4_RX.	ECLK.A	ligned ⁸	
t _{DVA}	Input Data Valid After ECLK		—	0.307	—	0.320	UI	
t _{DVE}	Input Data Hold After ECLK	-	0.782	—	0.699	—	UI	
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO3L/LF devices,		800	—	630	Mbps	
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only		400	—	315	MHz	
f _{SCLK}	SCLK Frequency			100	—	79	MHz	
Generic DDF	A4 Inputs with Clock and Data Centered at P	in Using PCLK Pin for Cloc	k Input	- GDDR	X4_RX.E	CLK.Ce	entered ⁸	
t _{SU}	Input Data Setup Before ECLK		0.233	—	0.219	—	ns	
t _{HO}	Input Data Hold After ECLK		0.287	—	0.287		ns	
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO3L/LF devices,	_	800	—	630	Mbps	
f _{DDRX4}	DDRX4 ECLK Frequency		_	400	—	315	MHz	
f _{SCLK}	SCLK Frequency			100	—	79	MHz	
7:1 LVDS In	outs (GDDR71_RX.ECLK.7:1) ⁹							
t _{DVA}	Input Data Valid After ECLK		—	0.290	—	0.320	UI	
t _{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	UI	
f _{DATA}	DDR71 Serial Input Data Speed	MachXO3L/LF devices,	—	756	—	630	Mbps	
f _{DDR71}	DDR71 ECLK Frequency	bottom side only	—	378	—	315	MHz	
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (mini- mum limited by PLL)		_	108	—	90	MHz	



DC and Switching Characteristics MachXO3 Family Data Sheet

		-6		-5			
Description	Device	Min.	Max.	Min.	Max.	Units	
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered ^{8, 9}							
Output Data Valid Before CLK Output		0.455		0.570		ns	
Output Data Valid After CLK Output		0.455	—	0.570	_	ns	
DDRX4 Serial Output Data Speed	MachXO3L/LF devices,	—	800	_	630	Mbps	
DDRX4 ECLK Frequency (minimum limited by PLL)	top side only	_	400	_	315	MHz	
SCLK Frequency	-		100		79	MHz	
Itputs – GDDR71_TX.ECLK.7:1 ^{8, 9}							
Output Data Invalid Before CLK Output			0.160	_	0.180	ns	
Output Data Invalid After CLK Output	— 0.				0.180	ns	
DDR71 Serial Output Data Speed	MachXO3L/LF devices,		756		630	Mbps	
DDR71 ECLK Frequency	top side only	_	378	—	315	MHz	
7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL)		_	108	_	90	MHz	
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_TX.ECLK.Centered ^{10, 11, 12}							
Output Data Valid Before CLK Output		0.200	—	0.200	_	UI	
Output Data Valid After CLK Output		0.200	—	0.200	_	UI	
MIPI D-PHY Output Data Speed	All MachXO3L/LF	_	900	_	900	Mbps	
MIPI D-PHY ECLK Frequency (minimum limited by PLL)	devices, top side only	_	450	_	450	MHz	
SCLK Frequency	<u> </u>	—	112.5	—	112.5	MHz	
	Description RX4 Outputs with Clock and Data Centered CECLK.Centered ^{8, 9} Output Data Valid Before CLK Output Output Data Valid After CLK Output DDRX4 Serial Output Data Speed DDRX4 ECLK Frequency (minimum limited by PLL) SCLK Frequency ttputs – GDDR71_TX.ECLK.7:1 ^{8, 9} Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed DDR71 ECLK Frequency 7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL) Outputs with Clock and Data Centered at P C.ECLK.Centered ^{10, 11, 12} Output Data Valid Before CLK Output Output Data Valid After CLK Output MIPI D-PHY Output Data Speed MIPI D-PHY ECLK Frequency (minimum limited by PLL) SCLK Frequency	DescriptionDeviceRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for C.ECLK.Centered ^{8, 9} In Using PCLK Pin for C.ECLK.Centered ^{8, 9} Output Data Valid Before CLK OutputMachXO3L/LF devices, top side onlyDDRX4 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side onlySCLK FrequencyOutput Data Invalid Before CLK OutputOutput Data Invalid Before CLK OutputMachXO3L/LF devices, top side onlyOutput Data Invalid After CLK OutputMachXO3L/LF devices, top side onlyDDR71 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDT71 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side onlyOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputMachXO3L/LF devices, top side onlyOutput Data Valid Before CLK OutputAll MachXO3L/LFOutput Data Valid After CLK OutputAll MachXO3L/LFMIPI D-PHY Output Data SpeedAll MachXO3L/LFMIPI D-PHY CLK Frequency (minimum limited by PLL)All MachXO3L/LFSCLK FrequencyAll MachXO3L/LF	Description Device Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock (LECLK.Centered ^{8,9}) 0.455 Output Data Valid Before CLK Output 0.455 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only SCLK Frequency Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed MachXO3L/LF devices, top side only DDR71 ECLK Frequency Output Clock Frequency (SCLK) (minimum limited by PLL) Output Data Valid After CLK Output Output Data Valid Before CLK Output Output Data Valid After CLK Output 0.200 0.200 0.200 Output Data Valid After CLK Out	-6Min.Max.RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - CLECLK.Centered ^{8, 9} Output Data Valid Before CLK Output0.455Output Data Valid After CLK OutputMachXO3L/LF devices, top side only0.455DDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side only800SCLK Frequency (minimum limited by PLL)100400Output Data Invalid Before CLK Output0.160Output Data Invalid After CLK Output0.160DDR71 Serial Output Data Speed DDR71 Serial Output Data SpeedMachXO3L/LF devices, top side only108Output Swith Clock and Data Centered at Pin Using PCLK Pin for Clock Input - t.ECLK.Centered ^{10, 11, 12} 0.200Output Data Valid Before CLK Output DDR71 Serial Output Data SpeedAll MachXO3L/LF devices, top side only0.200Output Data Valid After CLK Output Mup PLL)All MachXO3L/LF devices, top side only0.200MIPI D-PHY Output Data Speed MIPI D-PHY CLK Frequency (minimum limited by PLL)All MachXO3L/LF devices, top side only450MIPI D-PHY ECLK Frequency (minimum limited by PLL)450450	Description Image: Description Image: Description Max. Min. Max. Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{8, 9} 0.455 - 0.570 Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only - 800 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 400 - SCLK Frequency - 0.160 -	Description Device Min. Max. Min. Max. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{9,9} 0.455 - 0.570 - Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 800 - 630 SCLK Frequency - 0.160 - 916 - 916 Output Data Invalid Before CLK Output MachXO3L/LF devices, top side only - 0.160 - 0.180 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 108 - 90 Output Data Valid After CLK Output MachXO3L/LF	

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

5. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.

6. The t_{SU DEL} and t_{H DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).

7. This number for general purpose usage. Duty cycle tolerance is +/-10%.

8. Duty cycle is $\pm -5\%$ for system usage.

9. Performance is calculated with 0.225 UI.

10. Performance is calculated with 0.20 UI.

11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.

12. Performance for Industrial devices and -5 devices are not modeled in the Diamond design tool.

13. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

14. Above 800 Mbps is only supported with WLCSP and csfBGA packages

15. Between 800 Mbps to 900 Mbps:

a. VIDTH exceeds the MIPI D-PHY Input DC Conditions Table 3-4 and can be calculated with the equation tSU or tH = -0.0005*VIDTH + 0.3284

b. Example calculations

i. tSU and tHO = 0.28 with VIDTH = 100 mV

ii. tSU and tHO = 0.25 with VIDTH = 170 mV

iii. tSU and tHO = 0.20 with VIDTH = 270 mV



sysCLOCK PLL Timing

Parameter	Descriptions Conditions		Min.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS)		1.5625	400	MHz
f _{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f _{VCO}	PLL VCO Frequency		200	800	MHz
f _{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteri	stics	•			
t _{DT}	Output Clock Duty Cycle	Without duty trim selected ³	45	55	%
t _{DT_TRIM} ⁷	Edge Duty Trim Accuracy		-75	75	%
t _{PH} ⁴	Output Phase Accuracy		-6	6	%
	Output Cleak Pariad littar	f _{OUT} > 100 MHz	—	150	ps p-p
		f _{OUT} < 100 MHz	—	0.007	UIPP
		f _{OUT} > 100 MHz	—	180	ps p-p
		f _{OUT} < 100 MHz	—	0.009	UIPP
+ 1.8		f _{PFD} > 100 MHz	—	160	ps p-p
^t OPJIT ^{',°}	Output Clock Phase Jitter	f _{PFD} < 100 MHz	—	0.011	UIPP
		f _{OUT} > 100 MHz	—	230	ps p-p
	Output Clock Period Jitter (Fractional-N)	f _{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter	f _{OUT} > 100 MHz	—	230	ps p-p
	(Fractional-N)	f _{OUT} < 100 MHz	—	0.12	UIPP
t _{SPO}	Static Phase Offset	Divider ratio = integer	-120	120	ps
t _W	Output Clock Pulse Width	At 90% or 10% ³	0.9	—	ns
tLOCK ^{2, 5}	PLL Lock-in Time		—	15	ms
t _{UNLOCK}	PLL Unlock Time		—	50	ns
t _{IPJIT} ⁶	Innut Clask Daviad Littar	f _{PFD} ≥ 20 MHz	—	1,000	ps p-p
		f _{PFD} < 20 MHz	—	0.02	UIPP
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t _{STABLE} ⁵	STANDBY High to PLL Stable		—	15	ms
t _{RST}	RST/RESETM Pulse Width		1	—	ns
t _{RSTREC}	RST Recovery Time		1	—	ns
t _{RST DIV}	RESETC/D Pulse Width		10	—	ns
t _{RSTREC} DIV	RESETC/D Recovery Time		1	—	ns
t _{ROTATE-SETUP}	PHASESTEP Setup Time		10	—	ns
t _{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

Over Recommended Operating Conditions

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide for more details.

5. At minimum $\rm f_{PFD}$ As the $\rm f_{PFD}$ increases the time will decrease to approximately 60% the value listed.

6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.

7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.

8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.



Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions		
Configuration (Dual function pins used during sysCONFIG)				
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.		
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.		
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.		
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.		
SN	I	Slave SPI active low chip select input.		
CSSPIN	I/O	Master SPI active low chip select output.		
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.		
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.		
SCL	I/O	Slave I ² C clock input and master I ² C clock output.		
SDA	I/O	Slave I ² C data input and master I ² C data output.		



	MachXO3L/LF-2100					
	WLCSP49	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324
General Purpose IO per Bank		•	•			
Bank 0	19	24	50	71	50	71
Bank 1	0	26	52	62	52	68
Bank 2	13	26	52	72	52	72
Bank 3	0	7	16	22	16	24
Bank 4	0	7	16	14	16	16
Bank 5	6	10	20	27	20	28
Total General Purpose Single Ended IO	38	100	206	268	206	279
Differential IO per Bank						
Bank 0	10	12	25	36	25	36
Bank 1	0	13	26	30	26	34
Bank 2	6	13	26	36	26	36
Bank 3	0	3	8	10	8	12
Bank 4	0	3	8	6	8	8
Bank 5	3	5	10	13	10	14
Total General Purpose Differential IO	19	49	103	131	103	140
Dual Function IO	25	33	33	37	33	37
Number 7:1 or 8:1 Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18
High-speed Differential Outputs						
Bank 0	5	7	14	18	14	18
VCCIO Pins		•	•			
Bank 0	2	1	4	4	4	4
Bank 1	0	1	3	4	4	4
Bank 2	1	1	4	4	4	4
Bank 3	0	1	2	2	1	2
Bank 4	0	1	2	2	2	2
Bank 5	1	1	2	2	1	2
VCC	2	4	8	8	8	10
GND	4	10	24	16	24	16
NC	0	0	0	13	1	0
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	49	121	256	324	256	324



Date	Version	Section	Change Summary
April 2016	1.6	Introduction	Updated Features section. — Revised logic density range and IO to LUT ratio under Flexible Archi- tecture. — Revised 0.8 mm pitch information under Advanced Packaging. — Added MachXO3L-9400/MachXO3LF-9400 information to Table 1-1, MachXO3L/LF Family Selection Guide.
			Updated Introduction section. — Changed density from 6900 to 9400 LUTs. — Changed caBGA packaging to 19 x 19 mm.
		Architecture	Updated Architecture Overview section. — Changed statement to "All logic density devices in this family" — Updated Figure 2-2 heading and notes.
			Updated sysCLOCK Phase Locked Loops (PLLs) section. — Changed statement to "All MachXO3L/LF devices have one or more sysCLOCK PLL."
			Updated Programmable I/O Cells (PIC) section. — Changed statement to "All PIO pairs can implement differential receivers."
			Updated sysIO Buffer Banks section. Updated Figure 2-5 heading.
			Updated Device Configuration section. Added Password and Soft Error Correction.
		DC and Switching Characteristics	Updated Static Supply Current – C/E Devices section. Added LCMXO3L/ LF-9400C and LCMXO3L/LF-9400E devices.
			Updated Programming and Erase Supply Current – C/E Devices section. — Added LCMXO3L/LF-9400C and LCMXO3L/LF-9400E devices. — Changed LCMXO3L/LF-640E and LCMXO3L/LF-1300E Typ. values.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. Added MachXO3L/LF-9400 devices.
			Updated NVCM/Flash Download Time section. Added LCMXO3L/LF- 9400C device.
			Updated sysCONFIG Port Timing Specifications section. — Added LCMXO3L/LF-9400C device. — Changed t _{INITL} units to from ns to us. — Changed t _{DPPINIT} and t _{DPPDONE} Max. values are per PCN#03A-16.
		Pinout Information	Updated Pin Information Summary section. Added LCMXO3L/LF-9400C device.
		Ordering Information	Updated MachXO3 Part Number Description section. — Added 9400 = 9400 LUTs. — Added BG484 package.
			Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.



Date	Version	Section	Change Summary		
September 2015	1.5	DC and Switching Characteristics	Updated the MIPI D-PHY Emulation section. Revised Table 3-5, MIPI D- PHY Output DC Conditions. — Revised RL Typ. value. — Revised RH description and values.		
			Updated the Maximum sysIO Buffer Performance section. Revised MIPI Max. Speed value.		
			Updated the MachXO3L/LF External Switching Characteristics – C/E Devices section. Added footnotes 14 and 15.		
August 2015	1.4	Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.		
		Ordering Information	Updated the top side markings section to indicate the use of LMXO3LF for the LCMXO3LF device.		
March 2015	1.3	All	General update. Added MachXO3LF devices.		
October 2014	1.2	Introduction	Updated Table 1-1, MachXO3L Family Selection Guide. Revised XO3L- 2100 and XO3L-4300 IO for 324-ball csfBGA package.		
		Architecture	Updated the Dual Boot section. Corrected information on where the pri- mary bitstream and the golden image must reside.		
		Pinout Information	Updated the Pin Information Summary section.		
			Changed General Purpose IO Bank 5 values for MachXO3L-2100 and MachXO3L-4300 CSFBGA 324 package.		
			Changed Number 7:1 or 8:1 Gearboxes for MachXO3L-640 and MachXO3L-1300.		
			Removed DQS Groups (Bank 1) section.		
			Changed VCCIO Pins Bank 1 values for MachXO3L-1300, MachXO3L- 2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.		
			Changed GND values for MachXO3L-1300, MachXO3L-2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.		
			Changed NC values for MachXO3L-2100 and MachXO3L-4300 CSF- BGA 324 package.		
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.		
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.		
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.		
July 2014	1.1	DC and Switching Characteristics	Updated the Static Supply Current – C/E Devices section. Added devices.		
			Updated the Programming and Erase Supply Current – C/E Device section. Added devices.		
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Revised footnote 4.		
			Added the NVCM Download Time section.		
			Updated the Typical Building Block Function Performance – C/E Devices section. Added information to footnote.		
		Pinout Information	Updated the Pin Information Summary section.		
		Ordering Information	Updated the MachXO3L Part Number Description section. Added packages.		
			Updated the Ordering Information section. General update.		