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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	65536
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	121-VFBGA, CSPBGA
Supplier Device Package	121-CSFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-640e-6mg121i

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# MachXO3 Family Data Sheet Introduction

#### January 2016

## **Features**

### Solutions

- Smallest footprint, lowest power, high data throughput bridging solutions for mobile applications
- Optimized footprint, logic density, IO count, IO performance devices for IO management and logic applications
- High IO/logic, lowest cost/IO, high IO devices for IO expansion applications

## ■ Flexible Architecture

- Logic Density ranging from 640 to 9.4K LUT4
- High IO to LUT ratio with up to 384 IO pins

## Advanced Packaging

- 0.4 mm pitch: 1K to 4K densities in very small footprint WLCSP (2.5 mm x 2.5 mm to 3.8 mm x 3.8 mm) with 28 to 63 IOs
- 0.5 mm pitch: 640 to 6.9K LUT densities in 6 mm x 6 mm to 10 mm x 10 mm BGA packages with up to 281 IOs
- 0.8 mm pitch: 1K to 9.4K densities with up to 384 IOs in BGA packages

## Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRx2, DDRx4

## High Performance, Flexible I/O Buffer

- Programmable sysIO<sup>™</sup> buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - LVDS, Bus-LVDS, MLVDS, LVPECL
  - MIPI D-PHY Emulated
  - Schmitt trigger inputs, up to 0.5 V hysteresis
- Ideal for IO bridging applications
- I/Os support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

## ■ Flexible On-Chip Clocking

- · Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
  - Wide input frequency range (7 MHz to 400 MHz)
- Non-volatile, Multi-time Programmable
  - Instant-on
    - Powers up in microseconds
    - · Optional dual boot with external SPI memory
    - Single-chip, secure solution
    - Programmable through JTAG, SPI or I<sup>2</sup>C
    - MachXO3L includes multi-time programmable
       NVCM
    - MachXO3LF infinitely reconfigurable Flash

       Supports background programming of non-volatile memory

## ■ TransFR Reconfiguration

In-field logic update while IO holds the system state

## Enhanced System Level Support

- On-chip hardened functions: SPI, I<sup>2</sup>C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

### Applications

- Consumer Electronics
- Compute and Storage
- Wireless Communications
- Industrial Control Systems
- Automotive System

### Low Cost Migration Path

- Migration from the Flash based MachXO3LF to the NVCM based MachXO3L
- · Pin compatible and equivalent timing

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#### Advance Data Sheet DS1047



## Figure 2-4. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
   WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

 Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in <sup>1</sup>
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 <sup>2</sup> MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out <sup>1</sup>

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

## Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

## **Ripple Mode**

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

## **RAM Mode**

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3L/LF devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO3L/LF devices, please see TN1290, Memory Usage Guide for MachXO3 Devices.

### Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4	
Number of slices	3	3	
Note: SPB = Single Port RAM_PDPB = Pseudo Dual Port RAM			

ote: SPR = Single Port RAM, PDPR = Pseudo Dual



#### Figure 2-6. Secondary High Fanout Nets for MachXO3L/LF Devices



## sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO3L/LF devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO3L/LF sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO3L/LF clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.



This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the  $t_{I,OCK}$  parameter has been satisfied.

The MachXO3L/LF also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO3L/LF PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t<sub>LOCK</sub> parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.



### Figure 2-7. PLL Diagram

Table 2-4 provides signal descriptions of the PLL block.

Table 2-4	. PLL	Signal	Descriptions
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Port Name	I/O	Description
CLKI	Ι	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	Ι	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	Ι	Dynamic Phase step – toggle shifts VCO phase adjust by one step.



 Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

#### Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

#### **RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the NVCM or Configuration Flash.

MachXO3LF EBR initialization data can also be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO3LF devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

#### Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

#### Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.



### Figure 2-8. sysMEM Memory Primitives





## PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Pin Name	I/О Туре	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

## Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

## Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.



## Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

### Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-13 shows a block diagram of the input gearbox.



## **Configuration and Testing**

This section describes the configuration and testing features of the MachXO3L/LF family.

## IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with  $V_{CCIO}$  Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

## **Device Configuration**

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

- 1. Internal NVCM/Flash Download
- 2. JTAG
- 3. Standard Serial Peripheral Interface (Master SPI mode) interface to boot PROM memory
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, MachXO3 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/ LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.



### Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and NVCM/Flash spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

#### Password

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to TN1313, Using Password Security with MachXO3 Devices.

#### **Dual Boot**

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

#### Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1292, MachXO3 Soft Error Detection Usage Guide.

#### Soft Error Correction

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND\_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to TN1292, MachXO3 Soft Error Detection (SED)/Correction (SEC) Usage Guide.



# MachXO3 Family Data Sheet DC and Switching Characteristics

#### February 2017

#### Advance Data Sheet DS1047

## Absolute Maximum Ratings<sup>1, 2, 3</sup>

	MachXO3L/LF E (1.2 V)	MachXO3L/LF C (2.5 V/3.3 V)
Supply Voltage V <sub>CC</sub>	$\ldots$ .–0.5 V to 1.32 V $\ldots$ .	–0.5 V to 3.75 V
Output Supply Voltage V <sub>CCIO</sub>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied <sup>4, 5</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied <sup>4</sup>	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T <sub>1</sub> )	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

4. Overshoot and undershoot of -2 V to (V<sub>IHMAX</sub> + 2) volts is permitted for a duration of <20 ns.

5. The dual function  $I^2C$  pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

## **Recommended Operating Conditions**<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
V = = <sup>1</sup>	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
Core Supply Voltage for 2.5 V/3.3 V Devices	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V <sub>CCIO</sub> <sup>1, 2, 3</sup>	I/O Driver Supply Voltage	1.14	3.465	V
t <sub>JCOM</sub>	Junction Temperature Commercial Operation	0	85	°C
t <sub>JIND</sub>	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if V<sub>CCIO</sub> and V<sub>CC</sub> are both the same voltage, they must also be the same supply.

2. See recommended voltages by I/O standard in subsequent table.

3. V<sub>CCIO</sub> pins of unused I/O banks should be connected to the V<sub>CC</sub> power supply on boards.

## Power Supply Ramp Rates<sup>1</sup>

	iyp.	wax.	Units
t <sub>RAMP</sub> Power supply ramp rates for all power supplies. 0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

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# Static Supply Current – C/E Devices<sup>1, 2, 3, 6</sup>

Symbol	Parameter	Device	Typ.⁴	Units
I <sub>CC</sub>	Core Power Supply	LCMXO3L/LF-1300C 256 Ball Package	4.8	mA
		LCMXO3L/LF-2100C	4.8	mA
		LCMXO3L/LF-2100C 324 Ball Package	8.45	mA
		LCMXO3L/LF-4300C	8.45	mA
		LCMXO3L/LF-4300C 400 Ball Package	12.87	mA
		LCMXO3L/LF-6900C <sup>7</sup>	12.87	mA
		LCMXO3L/LF-9400C <sup>7</sup>	17.86	mA
		LCMXO3L/LF-640E	1.00	mA
		LCMXO3L/LF-1300E	1.00	mA
		LCMXO3L/LF-1300E 256 Ball Package	1.39	mA
		LCMXO3L/LF-2100E	1.39	mA
		LCMXO3L/LF-2100E 324 Ball Package	2.55	mA
		LCMXO3L/LF-4300E	2.55	mA
		LCMXO3L/LF-6900E	4.06	mA
		LCMXO3L/LF-9400E	5.66	mA
I <sub>CCIO</sub>	Bank Power Supply <sup>5</sup> VCCIO = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1289, Power Estimation and Management for MachXO3 Devices.

2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V<sub>CCIO</sub> or GND, on-chip oscillator is off, on-chip PLL is off.

3. Frequency = 0 MHz.

4.  $T_J = 25$  °C, power supplies at nominal voltage.

5. Does not include pull-up/pull-down.

6. To determine the MachXO3L/LF peak start-up current data, use the Power Calculator tool.

7. Determination of safe ambient operating conditions requires use of the Diamond Power Calculator tool.



## sysIO Recommended Operating Conditions

		V <sub>CCIO</sub> (V)		V <sub>REF</sub> (V)		
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25 <sup>1, 2</sup>	2.375	2.5	2.625	—	—	—
LVDS33 <sup>1, 2</sup>	3.135	3.3	3.465	—	—	—
LVPECL <sup>1</sup>	3.135	3.3	3.465	—	—	—
BLVDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
MIPI <sup>3</sup>	2.375	2.5	2.625	—	—	—
MIPI_LP <sup>3</sup>	1.14	1.2	1.26	—	—	—
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R334	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R254	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33 <sup>4</sup>	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25 <sup>₄</sup>	2.375	2.5	2.625	0.35	0.5	0.65

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. For the dedicated LVDS buffers.

3. Requires the addition of external resistors.

4. Supported only for inputs and BIDIs for -6 speed grade devices.



## sysIO Single-Ended DC Electrical Characteristics<sup>1, 2</sup>

Input/Output	V	/IL	v	н	Voi Max.	Vou Min.	lo, Max,⁴	ו <sub>ס⊔</sub> Max.⁴
Standard	Min. (V) <sup>3</sup>	Max. (V)	Min. (V)	Max. (V)	(V)	(V)	(mA)	(mA)
						V <sub>CCIO</sub> - 0.4	4	-4
					0.4		8	-8
	-0.3	0.8	2.0	3.6	0.4		12	-12
							16	-16
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
				3.6			4	-4
			1.7		0.4	V 04	8	-8
LVCMOS 2.5	-0.3	0.7			0.4	V <sub>CCIO</sub> - 0.4	12	-12
							16	-16
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
							4	-4
	-0.3	0.051/		0.4	V <sub>CCIO</sub> - 0.4	8	-8	
LVCMOS 1.8		0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	3.6			12	-12
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
	-0.3	3 0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>		3.6 0.4	V <sub>CCIO</sub> - 0.4	4	-4
LVCMOS 1.5				3.6			8	-8
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
	-0.3	–0.3 0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	3.6	0.4	V <sub>CCIO</sub> - 0.4	4	-2
LVCMOS 1.2							8	-6
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVCMOS25R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS10R25	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

 MachXO3L/LF devices allow LVCMOS inputs to be placed in I/O banks where V<sub>CCIO</sub> is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO3L/LF devices do not meet the relevant JEDEC specification are documented in the table below.

2. MachXO3L/LF devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1280, MachXO3 sysIO Usage Guide.

3. The dual function I<sup>2</sup>C pins SCL and SDA are limited to a  $V_{IL}$  min of -0.25 V or to -0.3 V with a duration of <10 ns.

4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n \* 8 mA. "n" is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.



## sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

## LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V V	Input Voltage	V <sub>CCIO</sub> = 3.3 V	0	_	2.605	V
VINP VINM		V <sub>CCIO</sub> = 2.5 V	0	_	2.05	V
V <sub>THD</sub>	Differential Input Threshold		±100	_		mV
V	Input Common Mode Voltage	V <sub>CCIO</sub> = 3.3 V	0.05	_	2.6	V
VCM	Input Common Mode Voltage	V <sub>CCIO</sub> = 2.5 V	0.05	_	2.0	V
I <sub>IN</sub>	Input current	Power on	_	_	±10	μA
V <sub>OH</sub>	Output high voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	_	1.375	_	V
V <sub>OL</sub>	Output low voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	0.90	1.025	_	V
V <sub>OD</sub>	Output voltage differential	(V <sub>OP</sub> - V <sub>OM</sub> ), R <sub>T</sub> = 100 Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in V <sub>OD</sub> between high and low		_	_	50	mV
V <sub>OS</sub>	Output voltage offset	(V <sub>OP</sub> - V <sub>OM</sub> )/2, R <sub>T</sub> = 100 Ohm	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in V <sub>OS</sub> between H and L		—	—	50	mV
IOSD	Output short circuit current	V <sub>OD</sub> = 0 V driver outputs shorted	_	_	24	mA

## **Over Recommended Operating Conditions**



## Table 3-5. MIPI D-PHY Output DC Conditions<sup>1</sup>

	Description	Min.	Тур.	Max.	Units
Transmitter	· · ·			•	•
External Termination	on				
RL	1% external resistor with VCCIO = 2.5 V	_	50		Ohms
	1% external resistor with VCCIO = 3.3 V	—	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	_	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	_	464	—	Ohms
High Speed	· ·				
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	_	2.5	_	V
	VCCIO of the Bank with LVDS Emulated output buffer	_	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage	_	—	360	V
ZOS	Single ended output impedance		50	_	Ohms
ΔZOS	Single ended output impedance mismatch		—	10	%
Low Power	· · · ·				
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	_	1.2	_	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	-50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

1. Over Recommended Operating Conditions



## sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Mo	odes				
t <sub>PRGM</sub>	PROGRAMN low p	PROGRAMN low pulse accept			ns
t <sub>PRGMJ</sub>	PROGRAMN low p	ulse rejection	_	25	ns
t <sub>INITL</sub>	INITN low time	LCMXO3L/LF-640/ LCMXO3L/LF-1300	—	55	us
		LCMXO3L/LF-1300 256-Ball Package/ LCMXO3L/LF-2100	_	70	us
		LCMXO3L/LF-2100 324-Ball Package/ LCMXO3-4300	_	105	us
		LCMXO3L/LF-4300 400-Ball Package/ LCMXO3-6900	_	130	us
		LCMXO3L/LF-9400C	_	175	us
t <sub>DPPINIT</sub>	PROGRAMN low to	NITN low	_	150	ns
t <sub>DPPDONE</sub>	PROGRAMN low to	DONE low	_	150	ns
t <sub>IODISS</sub>	PROGRAMN low to	o I/O disable	_	120	ns
Slave SPI					
f <sub>MAX</sub>	CCLK clock frequer	ncy		66	MHz
t <sub>CCLKH</sub>	CCLK clock pulse v	CCLK clock pulse width high			ns
t <sub>CCLKL</sub>	CCLK clock pulse v	vidth low	7.5	_	ns
t <sub>STSU</sub>	CCLK setup time		2	_	ns
t <sub>STH</sub>	CCLK hold time		0	_	ns
t <sub>STCO</sub>	CCLK falling edge t	to valid output	—	10	ns
t <sub>STOZ</sub>	CCLK falling edge t	to valid disable	_	10	ns
t <sub>STOV</sub>	CCLK falling edge t	to valid enable	_	10	ns
t <sub>SCS</sub>	Chip select high tim	ne	25	—	ns
t <sub>SCSS</sub>	Chip select setup ti	me	3	—	ns
t <sub>SCSH</sub>	Chip select hold tim	ne	3	_	ns
Master SPI				•	
f <sub>MAX</sub>	MCLK clock freque	ncy	—	133	MHz
t <sub>MCLKH</sub>	MCLK clock pulse v	width high	3.75	—	ns
t <sub>MCLKL</sub>	MCLK clock pulse v	width low	3.75	—	ns
t <sub>STSU</sub>	MCLK setup time		5	—	ns
t <sub>STH</sub>	MCLK hold time		1	—	ns
t <sub>CSSPI</sub>	INITN high to chip s	select low	100	200	ns
t <sub>MCI K</sub>	INITN high to first N	/ICLK edge	0.75	1	us



## Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions			
Configuration (Dual function pins used during sysCONFIG)					
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.			
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.			
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.			
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.			
SN	I	Slave SPI active low chip select input.			
CSSPIN	I/O	Master SPI active low chip select output.			
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.			
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.			
SCL	I/O	Slave I <sup>2</sup> C clock input and master I <sup>2</sup> C clock output.			
SDA	I/O	Slave I <sup>2</sup> C data input and master I <sup>2</sup> C data output.			



	MachXO3L/LF-2100						
	WLCSP49	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	
General Purpose IO per Bank		•	•			•	
Bank 0	19	24	50	71	50	71	
Bank 1	0	26	52	62	52	68	
Bank 2	13	26	52	72	52	72	
Bank 3	0	7	16	22	16	24	
Bank 4	0	7	16	14	16	16	
Bank 5	6	10	20	27	20	28	
Total General Purpose Single Ended IO	38	100	206	268	206	279	
Differential IO per Bank							
Bank 0	10	12	25	36	25	36	
Bank 1	0	13	26	30	26	34	
Bank 2	6	13	26	36	26	36	
Bank 3	0	3	8	10	8	12	
Bank 4	0	3	8	6	8	8	
Bank 5	3	5	10	13	10	14	
Total General Purpose Differential IO	19	49	103	131	103	140	
Dual Function IO	25	33	33	37	33	37	
Number 7:1 or 8:1 Gearboxes						•	
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18	
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18	
High-speed Differential Outputs						•	
Bank 0	5	7	14	18	14	18	
VCCIO Pins		•	•			•	
Bank 0	2	1	4	4	4	4	
Bank 1	0	1	3	4	4	4	
Bank 2	1	1	4	4	4	4	
Bank 3	0	1	2	2	1	2	
Bank 4	0	1	2	2	2	2	
Bank 5	1	1	2	2	1	2	
VCC	2	4	8	8	8	10	
GND	4	10	24	16	24	16	
NC	0	0	0	13	1	0	
Reserved for Configuration	1	1	1	1	1	1	
Total Count of Bonded Pins	49	121	256	324	256	324	