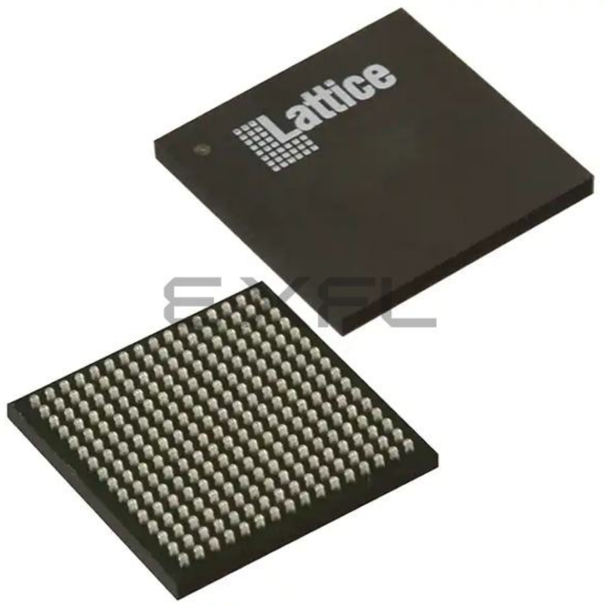

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	858
Number of Logic Elements/Cells	6864
Total RAM Bits	245760
Number of I/O	206
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-VFBGA
Supplier Device Package	256-CSFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-6900e-5mg256c

and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO3L/LF devices are available in two versions C and E with two speed grades: -5 and -6, with -6 being the fastest. C devices have an internal linear voltage regulator which supports external VCC supply voltages of 3.3 V or 2.5 V. E devices only accept 1.2 V as the external VCC supply voltage. With the exception of power supply voltage both C and E are functionally compatible with each other.

The MachXO3L/LF PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5 x 2.5 mm WLCSP to the 19 x 19 mm caBGA. MachXO3L/LF devices support density migration within the same package. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The MachXO3L/LF devices offer enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis.

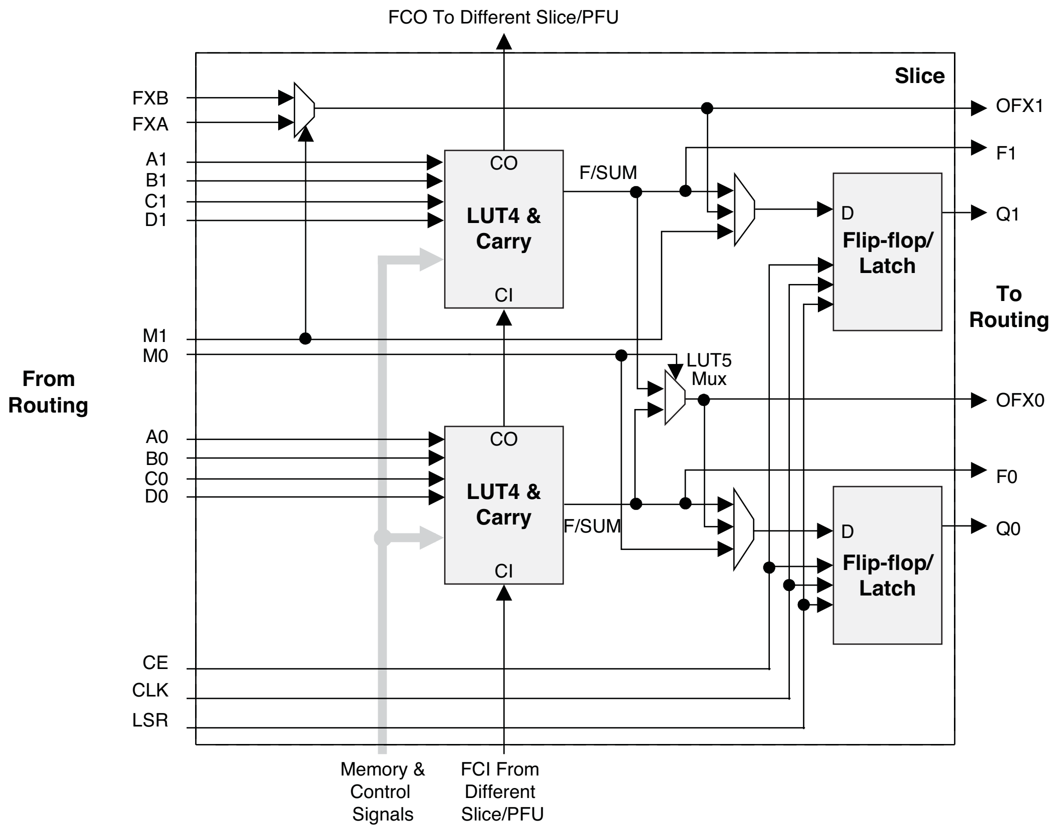
A user-programmable internal oscillator is included in MachXO3L/LF devices. The clock output from this oscillator may be divided by the timer/counter for use as clock input in functions such as LED control, key-board scanner and similar state machines.

The MachXO3L/LF devices also provide flexible, reliable and secure configuration from on-chip NVCM/Flash. These devices can also configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or through the I^2C port. Additionally, MachXO3L/LF devices support dual-boot capability (using external Flash memory) and remote field upgrade (TransFR) capability.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the MachXO3L/LF family of devices. Popular logic synthesis tools provide synthesis library support for MachXO3L/LF. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the MachXO3L/LF device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) LatticeCORE™ modules, including a number of reference designs licensed free of charge, optimized for the MachXO3L/LF PLD family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-4. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed-back signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO3L/LF devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

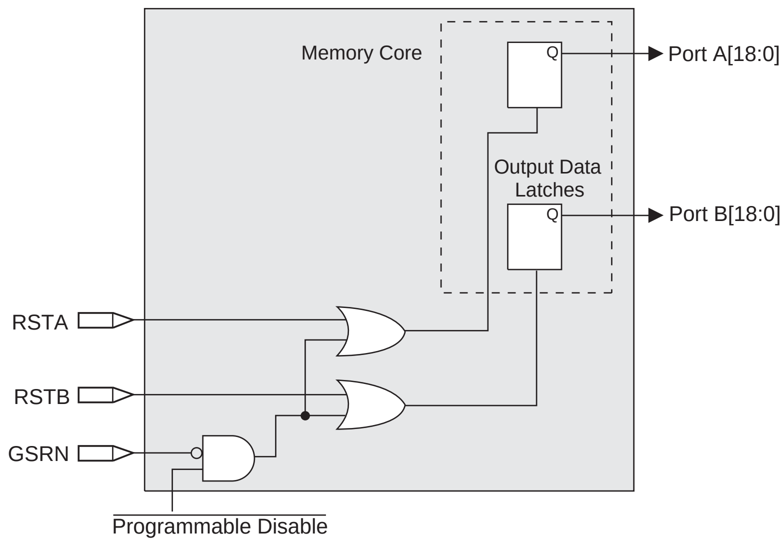
The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

Figure 2-9. Memory Core Reset

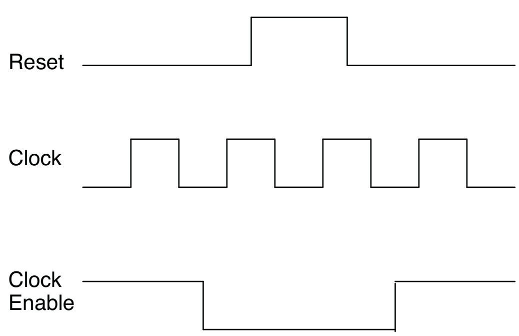


For further information on the sysMEM EBR block, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

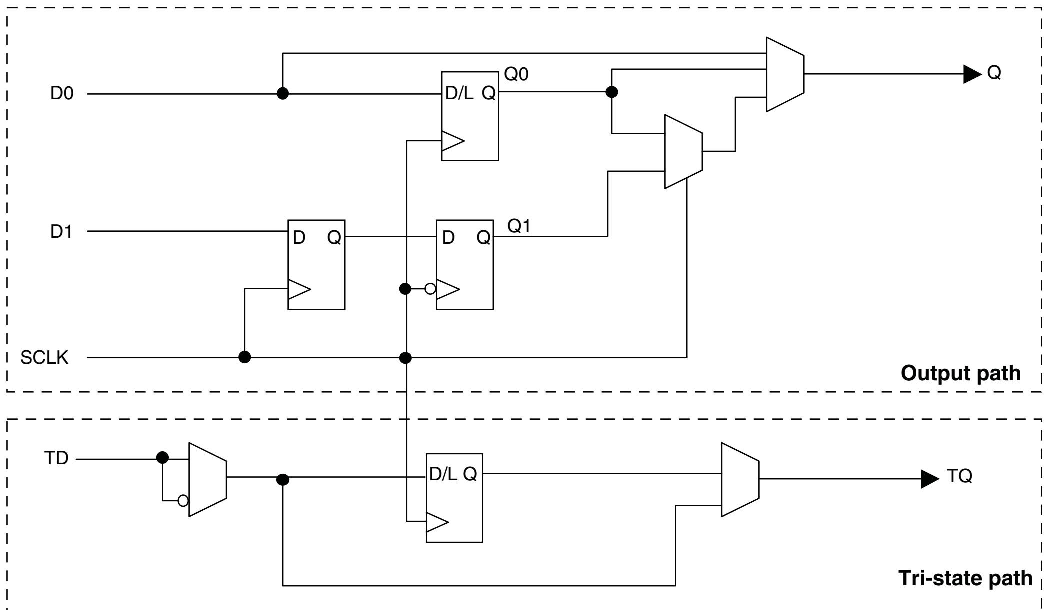
Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-12 shows the output register block on the left, top and bottom edges.

Figure 2-12. MachXO3L/LF Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-14 shows the output gearbox block diagram.

Table 2-11 shows the I/O standards (together with their supply and reference voltages) supported by the MachXO3L/LF devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1280, MachXO3 sysIO Usage Guide.

Table 2-11. Supported Input Standards

	VCCIO (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5 V**	**1.2 V**
Single-Ended Interfaces					
LVTTL	Yes				
LVCMOS33	Yes				
LVCMOS25		Yes			
LVCMOS18			Yes		
LVCMOS15				Yes	
LVCMOS12					Yes
PCI	Yes				
Differential Interfaces					
LVDS	Yes	Yes			
BLVDS, MLVDS, LVPECL, RSDS	Yes	Yes			
MIPI[1]	Yes	Yes			
LVTTLD	Yes				
LVCMOS33D	Yes				
LVCMOS25D		Yes			
LVCMOS18D			Yes		

1. These interfaces can be emulated with external resistors in all devices.

Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-13 lists all the available MCLK frequencies.

Table 2-13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

For more details on these embedded functions, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

User Flash Memory (UFM)

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

Standby Mode and Power Saving Options

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the E devices operate at 1.2 V V_{CC}.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I^2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

1. Internal NVCM/Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I^2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, MachXO3 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

TraceID

Each MachXO3L/LF device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I^2C, or JTAG interfaces.

Density Shifting

The MachXO3L/LF family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO3 migration files.

sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

LVDS

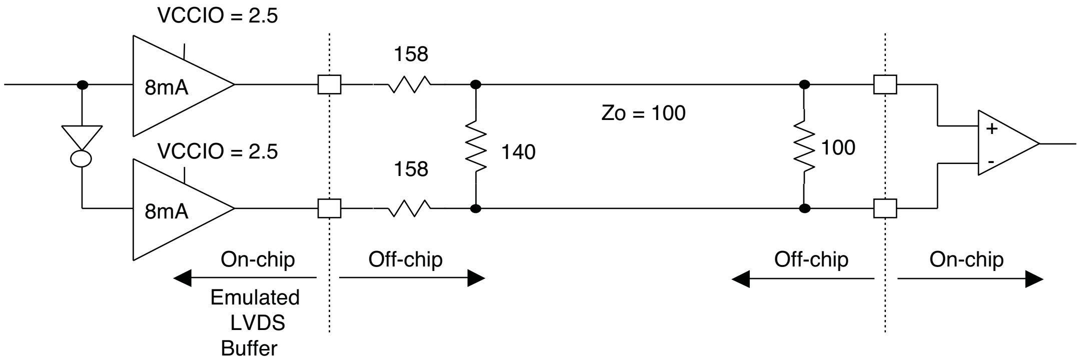
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3 V	0	—	2.605	V
		V_{CCIO} = 2.5 V	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

LVDS Emulation

MachXO3L/LF devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

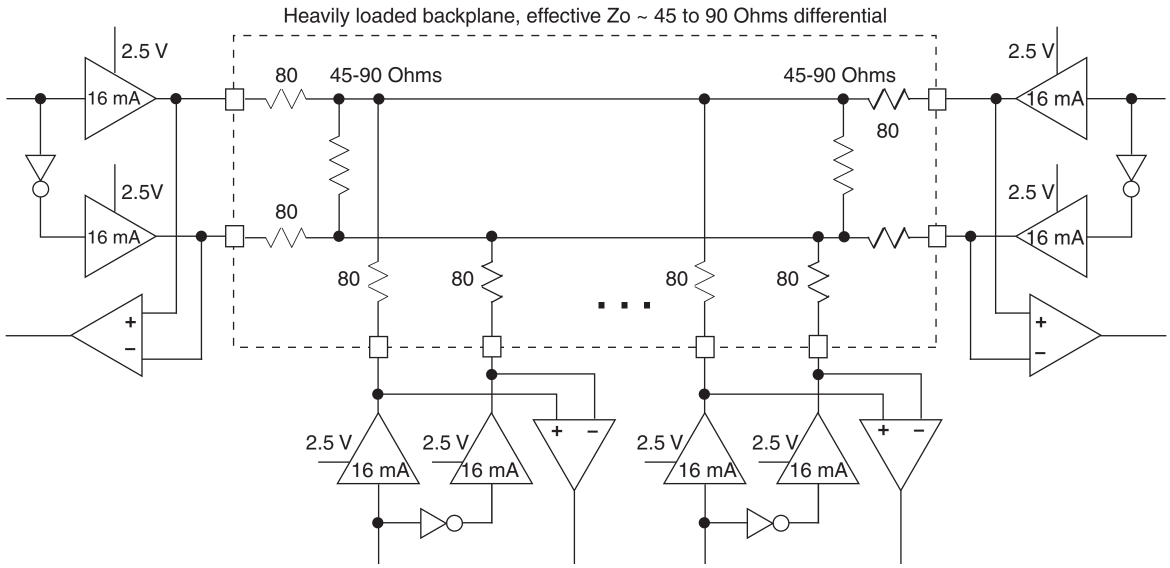


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

Parameter	Description	Device	–6 Min.	–6 Max.	–5 Min.	–5 Max.	Units
General I/O Pin Parameters (Using Edge Clock without PLL)							
t_{COE}	Clock to Output - PIO Output Register	MachXO3L/LF-1300	—	7.53	—	7.76	ns
		MachXO3L/LF-2100	—	7.53	—	7.76	ns
		MachXO3L/LF-4300	—	7.45	—	7.68	ns
		MachXO3L/LF-6900	—	7.53	—	7.76	ns
		MachXO3L/LF-9400	—	8.93	—	9.35	ns
t_{SUE}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-1300	–0.19	—	–0.19	—	ns
		MachXO3L/LF-2100	–0.19	—	–0.19	—	ns
		MachXO3L/LF-4300	–0.16	—	–0.16	—	ns
		MachXO3L/LF-6900	–0.19	—	–0.19	—	ns
		MachXO3L/LF-9400	–0.20	—	–0.20	—	ns
t_{HE}	Clock to Data Hold - PIO Input Register	MachXO3L/LF-1300	1.97	—	2.24	—	ns
		MachXO3L/LF-2100	1.97	—	2.24	—	ns
		MachXO3L/LF-4300	1.89	—	2.16	—	ns
		MachXO3L/LF-6900	1.97	—	2.24	—	ns
		MachXO3L/LF-9400	1.98	—	2.25	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	1.56	—	1.69	—	ns
		MachXO3L/LF-2100	1.56	—	1.69	—	ns
		MachXO3L/LF-4300	1.74	—	1.88	—	ns
		MachXO3L/LF-6900	1.66	—	1.81	—	ns
		MachXO3L/LF-9400	1.71	—	1.85	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-2100	–0.23	—	–0.23	—	ns
		MachXO3L/LF-4300	–0.34	—	–0.34	—	ns
		MachXO3L/LF-6900	–0.29	—	–0.29	—	ns
		MachXO3L/LF-9400	–0.30	—	–0.30	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)							
t_{COPLL}	Clock to Output - PIO Output Register	MachXO3L/LF-1300	—	5.98	—	6.01	ns
		MachXO3L/LF-2100	—	5.98	—	6.01	ns
		MachXO3L/LF-4300	—	5.99	—	6.02	ns
		MachXO3L/LF-6900	—	6.02	—	6.06	ns
		MachXO3L/LF-9400	—	5.55	—	6.13	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-1300	0.36	—	0.36	—	ns
		MachXO3L/LF-2100	0.36	—	0.36	—	ns
		MachXO3L/LF-4300	0.35	—	0.35	—	ns
		MachXO3L/LF-6900	0.34	—	0.34	—	ns
		MachXO3L/LF-9400	0.33	—	0.33	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	MachXO3L/LF-1300	0.42	—	0.49	—	ns
		MachXO3L/LF-2100	0.42	—	0.49	—	ns
		MachXO3L/LF-4300	0.43	—	0.50	—	ns
		MachXO3L/LF-6900	0.46	—	0.54	—	ns
		MachXO3L/LF-9400	0.47	—	0.55	—	ns

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[8, 9]							
t_{DVA}	Input Data Valid After CLK	All MachXO3L/LF devices, all sides	—	0.317	—	0.344	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[8, 9]							
t_{SU}	Input Data Setup Before CLK	All MachXO3L/LF devices, all sides	0.566	—	0.560	—	ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—		Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[8, 9]							
t_{DVA}	Input Data Valid After CLK	MachXO3L/LF devices, bottom side only	—	0.316	—	0.342	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[8, 9]							
t_{SU}	Input Data Setup Before CLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[8]							
t_{DVA}	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.307	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK		0.782	—	0.699	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[8]							
t_{SU}	Input Data Setup Before ECLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9]							
t_{DVA}	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.290	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy		–75	75	%
t_{PH}[4]	Output Phase Accuracy		–6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	150	ps p-p
		f_{OUT} < 100 MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100 MHz	—	180	ps p-p
		f_{OUT} < 100 MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100 MHz	—	160	ps p-p
		f_{PFD} < 100 MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100 MHz	—	230	ps p-p
		f_{OUT} < 100 MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq$ 20 MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE\text{-}SETUP}$	PHASESTEP Setup Time		10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

NVCM/Flash Download Time[1, 2]

Symbol	Parameter	Device	Typ.	Units
$t_{REFRESH}$	POR to Device I/O Active	LCMXO3L/LF-640	1.9	ms
		LCMXO3L/LF-1300	1.9	ms
		LCMXO3L/LF-1300 256-Ball Package	1.4	ms
		LCMXO3L/LF-2100	1.4	ms
		LCMXO3L/LF-2100 324-Ball Package	2.4	ms
		LCMXO3L/LF-4300	2.4	ms
		LCMXO3L/LF-4300 400-Ball Package	3.8	ms
		LCMXO3L/LF-6900	3.8	ms
		LCMXO3L/LF-9400C	5.2	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.
2. The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.

	MachXO3L/LF-6900				
	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank					
Bank 0	50	73	50	71	83
Bank 1	52	68	52	68	84
Bank 2	52	72	52	72	84
Bank 3	16	24	16	24	28
Bank 4	16	16	16	16	24
Bank 5	20	28	20	28	32
Total General Purpose Single Ended IO	206	281	206	279	335
Differential IO per Bank					
Bank 0	25	36	25	36	42
Bank 1	26	34	26	34	42
Bank 2	26	36	26	36	42
Bank 3	8	12	8	12	14
Bank 4	8	8	8	8	12
Bank 5	10	14	10	14	16
Total General Purpose Differential IO	103	140	103	140	168
Dual Function IO	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes					
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	21	20	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	21	20	21	21
High-speed Differential Outputs					
Bank 0	20	21	20	21	21
VCCIO Pins					
Bank 0	4	4	4	4	5
Bank 1	3	4	4	4	5
Bank 2	4	4	4	4	5
Bank 3	2	2	1	2	2
Bank 4	2	2	2	2	2
Bank 5	2	2	1	2	2
VCC	8	8	8	10	10
GND	24	16	24	16	33
NC	0	0	1	0	0
Reserved for Configuration	1	1	1	1	1
Total Count of Bonded Pins	**256**	**324**	**256**	**324**	**400**

Date	Version	Section	Change Summary
June 2014	1.0	—	Product name/trademark adjustment.
		Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Changed fcCSP packages to csfBGA. Adjusted 121-ball csfBGA arrow.
			Introduction section general update.
		Architecture	General update.
		DC and Switching Characteristics	Updated sysIO Recommended Operating Conditions section. Removed V_{REF} (V) column. Added standards.
			Updated Maximum sysIO Buffer Performance section. Added MIPI I/O standard.
			Updated MIPI D-PHY Emulation section. Changed Low Speed to Low Power. Updated Table 3-4, MIPI DC Conditions.
			Updated Table 3-5, MIPI D-PHY Output DC Conditions.
			Updated Maximum sysIO Buffer Performance section.
			Updated MachXO3L External Switching Characteristics – C/E Device section.
May 2014	00.3	Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Moved 121-ball fcCSP arrow.
			General update of Introduction section.
		Architecture	General update.
		Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
		Ordering Information	Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
			Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers.
February 2014	00.2	DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.
	00.1	—	Initial release.