# Evy Eatlice Semiconductor Corporation - <u>LCMXO3L-9400C-5BG256C Datasheet</u>



Welcome to E-XFL.COM

#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	1175
Number of Logic Elements/Cells	9400
Total RAM Bits	442368
Number of I/O	206
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-9400c-5bg256c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



#### Table 1-1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900	9400
Distributed R/	AM (kbits)	5	10	16	34	54	73
EBR SRAM (I	kbits)	64	64	74	92	240	432
Number of PL	Ls	1	1	1	2	2	2
Hardened	l <sup>2</sup> C	2	2	2	2	2	2
Functions:	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY S	Support	Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Pro	ogrammable	MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmabl	e Flash	MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400
Packages				ΙΟ			
36-ball WLCSP <sup>1</sup> (2.5 mm x 2.5 mm, 0.4 mm)			28				
49-ball WLCS (3.2 mm x 3.2	P <sup>1</sup> mm, 0.4 mm)			38			
81-ball WLCS (3.8 mm x 3.8	P <sup>1</sup> mm, 0.4 mm)				63		
121-ball csfB0 (6 mm x 6 mm	GA <sup>1</sup> n, 0.5 mm)	100	100	100	100		
256-ball csfB (9 mm x 9 mn	GA <sup>1</sup> n, 0.5 mm)		206	206	206	206	206
324-ball csfB (10 mm x 10	GA <sup>1</sup> mm, 0.5 mm)		2	268	268	281	
256-ball caBGA <sup>2</sup> (14 mm x 14 mm, 0.8 mm)			206	206	206	206	206
324-ball caBC (15 mm x 15 i	àA² mm, 0.8 mm)			279	279	279	
400-ball caB0 (17 mm x 17 i	àA² mm, 0.8 mm)				335	335	335
484-ball caBC (19 mm x 19	3A² mm, 0.8 mm)						384

1. Package is only available for E=1.2 V devices.

2. Package is only available for C=2.5 V/3.3 V devices.

### Introduction

MachXO3<sup>™</sup> device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I<sup>2</sup>C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs



#### Figure 2-8. sysMEM Memory Primitives





### PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Pin Name	I/О Туре	Description	
CE	Input	Clock Enable	
D	Input	Pin input from sysIO buffer.	
INDD	Output	Register bypassed input.	
INCK	Output	Clock input	
Q0	Output	DDR positive edge input	
Q1	Output	Registered input/DDR negative edge input	
D0	Input	Output signal from the core (SDR and DDR)	
D1	Input	Output signal from the core (DDR)	
TD	Input	Tri-state signal from the core	
Q	Output	Data output signals to sysIO Buffer	
TQ	Output	Tri-state output signals to sysIO Buffer	
SCLK	Input	System clock for input and output/tri-state blocks.	
RST	Input	Local set reset signal	

### Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

#### Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.



### Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

#### Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-13 shows a block diagram of the input gearbox.



### sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO3L/LF devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) input buffers are powered using I/O supply voltage ( $V_{CCIO}$ ). Each sysIO bank has its own  $V_{CCIO}$ .

MachXO3L/LF devices contain three types of sysIO buffer pairs.

#### 1. Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential input buffers.

#### 2. Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after  $V_{CC}$  and  $V_{CCIO}$  are at valid operating levels and the device has been configured.

#### 3. Top sysIO Buffer Pairs

The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two singleended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver.

### Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$  and  $V_{CCIO0}$  have reached  $V_{PORUP}$  level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pulldown to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to  $V_{CCIO}$  as the default functionality). The I/O pins will maintain the blank configuration until  $V_{CC}$  and  $V_{CCIO}$  (for I/O banks containing configuration I/Os) have reached  $V_{PORUP}$  levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

There are various ways a user can ensure that there are no spurious signals on critical outputs as the device powers up. These are discussed in more detail in TN1280, MachXO3 sysIO Usage Guide.

#### **Supported Standards**

The MachXO3L/LF sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO3L/LF devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO3L/LF devices. PCI support is provided in the bottom bank of the MachXO3L/LF devices. Table 2-11 summarizes the I/O characteristics of the MachXO3L/LF PLDs.



### Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - Watchdog timer
  - Clear timer on compare match
  - Fast PWM
  - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

#### Figure 2-20. Timer/Counter Block Diagram



Table 2-16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



#### Table 2-17. MachXO3L/LF Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe $V_{CC}$ drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1289, Power Estimation and Management for MachXO3 Devices.

### Power On Reset

MachXO3L/LF devices have power-on reset circuitry to monitor  $V_{CCINT}$  and  $V_{CCIO}$  voltage levels during power-up and operation. At power-up, the POR circuitry monitors  $V_{CCINT}$  and  $V_{CCIO}$  (controls configuration) voltage levels. It then triggers download from the on-chip configuration NVCM/Flash memory after reaching the  $V_{PORUP}$  level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For "E" devices without voltage regulators,  $V_{CCINT}$  is the same as the  $V_{CC}$  supply voltage. For "C" devices with voltage regulators,  $V_{CCINT}$  is regulated from the  $V_{CC}$  supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as NVCM/Flash Download Time ( $t_{REFRESH}$ ) in the DC and Switching Characteristics section of this data sheet. Before and during configuration. Note that for "C" devices, a separate POR circuit monitors external  $V_{CC}$  voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor  $V_{CCINT}$  levels. If  $V_{CCINT}$  drops below  $V_{PORDNBG}$  level (with the bandgap circuitry switched on) or below  $V_{PORDNSRAM}$  level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the  $V_{CCINT}$  and  $V_{CCIO}$  voltage levels.  $V_{PORDNBG}$  and  $V_{PORDNSRAM}$  are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once an "E" device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a mini-mal, low power POR circuit is still operational (this corresponds to the  $V_{PORDNSRAM}$  reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the  $V_{CC}$  supply dropping below  $V_{CC}$  (min) they should not shut down the bandgap or POR circuit.



### sysIO Recommended Operating Conditions

		V <sub>CCIO</sub> (V)		V <sub>REF</sub> (V)		
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25 <sup>1, 2</sup>	2.375	2.5	2.625	—	—	—
LVDS33 <sup>1, 2</sup>	3.135	3.3	3.465	—	—	—
LVPECL <sup>1</sup>	3.135	3.3	3.465	—	—	—
BLVDS <sup>1</sup>	2.375	2.5	2.625	—	—	—
MIPI <sup>3</sup>	2.375	2.5	2.625	—	—	—
MIPI_LP <sup>3</sup>	1.14	1.2	1.26	—	—	—
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R334	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R254	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33 <sup>4</sup>	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25 <sup>₄</sup>	2.375	2.5	2.625	0.35	0.5	0.65

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. For the dedicated LVDS buffers.

3. Requires the addition of external resistors.

4. Supported only for inputs and BIDIs for -6 speed grade devices.



### sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

### LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
	Input Voltage	V <sub>CCIO</sub> = 3.3 V	0	_	2.605	V
VINP VINM		V <sub>CCIO</sub> = 2.5 V	0	_	2.05	V
V <sub>THD</sub>	Differential Input Threshold		±100	_		mV
V <sub>CM</sub>	Input Common Mode Voltage	V <sub>CCIO</sub> = 3.3 V	0.05	_	2.6	V
	Input Common Mode Voltage	V <sub>CCIO</sub> = 2.5 V	0.05	_	2.0	V
I <sub>IN</sub>	Input current	Power on	_	_	±10	μA
V <sub>OH</sub>	Output high voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	_	1.375	_	V
V <sub>OL</sub>	Output low voltage for $V_{OP}$ or $V_{OM}$	R <sub>T</sub> = 100 Ohm	0.90	1.025	_	V
V <sub>OD</sub>	Output voltage differential	(V <sub>OP</sub> - V <sub>OM</sub> ), R <sub>T</sub> = 100 Ohm	250	350	450	mV
$\Delta V_{OD}$	Change in V <sub>OD</sub> between high and low		_	_	50	mV
V <sub>OS</sub>	Output voltage offset	(V <sub>OP</sub> - V <sub>OM</sub> )/2, R <sub>T</sub> = 100 Ohm	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in V <sub>OS</sub> between H and L		—	—	50	mV
IOSD	Output short circuit current	V <sub>OD</sub> = 0 V driver outputs shorted	_	_	24	mA

### **Over Recommended Operating Conditions**



### Table 3-5. MIPI D-PHY Output DC Conditions<sup>1</sup>

	Description	Min.	Тур.	Max.	Units				
Transmitter									
External Termination	on								
RL	1% external resistor with VCCIO = 2.5 V		50		Ohms				
	1% external resistor with VCCIO = 3.3 V	—	50	—					
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	_	Ohms				
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	_	464	—	Ohms				
High Speed	· ·								
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	_	2.5	_	V				
	VCCIO of the Bank with LVDS Emulated output buffer	_	3.3	—	V				
VCMTX	HS transmit static common mode voltage	150	200	250	mV				
VOD	HS transmit differential voltage	140	200	270	mV				
VOHHS	HS output high voltage	_	—	360	V				
ZOS	Single ended output impedance		50	_	Ohms				
ΔZOS	Single ended output impedance mismatch		—	10	%				
Low Power	· · · ·								
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	_	1.2	_	V				
VOH	Output high level	1.1	1.2	1.3	V				
VOL	Output low level	-50	0	50	mV				
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms				

1. Over Recommended Operating Conditions



## MachXO3L/LF External Switching Characteristics – C/E Devices<sup>1, 2, 3, 4, 5, 6, 10</sup>

			-6		-5		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
Clocks							
Primary Clo	cks						-
f <sub>MAX_PRI</sub> <sup>7</sup>	Frequency for Primary Clock Tree	All MachXO3L/LF devices	_	388	_	323	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	All MachXO3L/LF devices	0.5		0.6		ns
	Primary Clock Skew Within a Device	MachXO3L/LF-1300		867	_	897	ps
		MachXO3L/LF-2100		867		897	ps
t <sub>SKEW_PRI</sub>		MachXO3L/LF-4300	_	865	_	892	ps
		MachXO3L/LF-6900	_	902	_	942	ps
		MachXO3L/LF-9400	_	908	_	950	ps
Edge Clock							
f <sub>MAX_EDGE</sub> <sup>7</sup>	Frequency for Edge Clock	MachXO3L/LF		400	_	333	MHz
Pin-LUT-Pin	Propagation Delay						
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All MachXO3L/LF devices		6.72		6.96	ns
General I/O	Pin Parameters (Using Primary Clock with	out PLL)					
		MachXO3L/LF-1300	—	7.46	—	7.66	ns
		MachXO3L/LF-2100	_	7.46	_	7.66	ns
t <sub>CO</sub>	Clock to Output - PIO Output Register	MachXO3L/LF-4300	_	7.51		7.71	ns
		MachXO3L/LF-6900	_	7.54		7.75	ns
		MachXO3L/LF-9400	_	7.53		7.83	ns
		MachXO3L/LF-1300	-0.20	_	-0.20		ns
		MachXO3L/LF-2100	-0.20	_	-0.20		ns
t <sub>SU</sub>	Clock to Data Setup - PIO Input Register	MachXO3L/LF-4300	-0.23	_	-0.23		ns
		MachXO3L/LF-6900	-0.23		-0.23		ns
		MachXO3L/LF-9400	-0.24		-0.24		ns
		MachXO3L/LF-1300	1.89		2.13		ns
		MachXO3L/LF-2100	1.89	_	2.13		ns
t <sub>H</sub>	Clock to Data Hold - PIO Input Register	MachXO3L/LF-4300	1.94	_	2.18		ns
		MachXO3L/LF-6900	1.98	_	2.23		ns
		MachXO3L/LF-9400	1.99	_	2.24		ns
		MachXO3L/LF-1300	1.61	_	1.76		ns
		MachXO3L/LF-2100	1.61	_	1.76		ns
t <sub>SU DEL</sub>	Clock to Data Setup - PIO Input Register	MachXO3L/LF-4300	1.66	_	1.81		ns
	with Data input Delay	MachXO3L/LF-6900	1.53	_	1.67		ns
		MachXO3L/LF-9400	1.65	_	1.80		ns
		MachXO3L/LF-1300	-0.23	_	-0.23		ns
		MachXO3L/LF-2100	-0.23	—	-0.23	_	ns
<sup>t</sup> H DEL	Clock to Data Hold - PIO Input Register with	MachXO3L/LF-4300	-0.25	_	-0.25	_	ns
	Input Data Delay	MachXO3L/LF-6900	-0.21	_	-0.21	_	ns
		MachXO3L/LF-9400	-0.24	_	-0.24	_	ns
f <sub>MAX_IO</sub>	Clock Frequency of I/O and PFU Register	All MachXO3L/LF devices	—	388	—	323	MHz

### Over Recommended Operating Conditions



### NVCM/Flash Download Time<sup>1, 2</sup>

Symbol	Parameter	Device	Тур.	Units
t <sub>REFRESH</sub>	POR to Device I/O Active	LCMXO3L/LF-640	1.9	ms
		LCMXO3L/LF-1300	1.9	ms
		LCMXO3L/LF-1300 256-Ball Package	1.4	ms
		LCMXO3L/LF-2100	1.4	ms
		LCMXO3L/LF-2100 324-Ball Package	2.4	ms
		LCMXO3L/LF-4300	2.4	ms
		LCMXO3L/LF-4300 400-Ball Package	3.8	ms
		LCMXO3L/LF-6900	3.8	ms
		LCMXO3L/LF-9400C	5.2	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.



### sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Mo	odes				
t <sub>PRGM</sub>	PROGRAMN low p	ulse accept	55	_	ns
t <sub>PRGMJ</sub>	PROGRAMN low p	ulse rejection	_	25	ns
t <sub>INITL</sub>	INITN low time	LCMXO3L/LF-640/ LCMXO3L/LF-1300	—	55	us
		LCMXO3L/LF-1300 256-Ball Package/ LCMXO3L/LF-2100	_	70	us
		LCMXO3L/LF-2100 324-Ball Package/ LCMXO3-4300	_	105	us
		LCMXO3L/LF-4300 400-Ball Package/ LCMXO3-6900	_	130	us
		LCMXO3L/LF-9400C	_	175	us
t <sub>DPPINIT</sub>	PROGRAMN low to	NITN low	_	150	ns
t <sub>DPPDONE</sub>	PROGRAMN low to	DONE low	_	150	ns
t <sub>IODISS</sub>	PROGRAMN low to	o I/O disable	_	120	ns
Slave SPI					
f <sub>MAX</sub>	CCLK clock frequer	псу		66	MHz
t <sub>CCLKH</sub>	CCLK clock pulse v	vidth high	7.5	—	ns
t <sub>CCLKL</sub>	CCLK clock pulse v	vidth low	7.5	_	ns
t <sub>STSU</sub>	CCLK setup time		2	_	ns
t <sub>STH</sub>	CCLK hold time		0	_	ns
t <sub>STCO</sub>	CCLK falling edge t	o valid output	—	10	ns
t <sub>STOZ</sub>	CCLK falling edge t	o valid disable	—	10	ns
t <sub>STOV</sub>	CCLK falling edge t	o valid enable	—	10	ns
t <sub>SCS</sub>	Chip select high tim	ne	25	—	ns
t <sub>SCSS</sub>	Chip select setup ti	me	3	—	ns
t <sub>SCSH</sub>	Chip select hold tim	ne	3	—	ns
Master SPI					
f <sub>MAX</sub>	MCLK clock freque	ncy	_	133	MHz
t <sub>MCLKH</sub>	MCLK clock pulse v	vidth high	3.75	—	ns
t <sub>MCLKL</sub>	MCLK clock pulse v	width low	3.75	—	ns
t <sub>STSU</sub>	MCLK setup time		5	—	ns
t <sub>STH</sub>	MCLK hold time		1	—	ns
t <sub>CSSPI</sub>	INITN high to chip s	select low	100	200	ns
t <sub>MCLK</sub>	INITN high to first M	ICLK edge	0.75	1	US



### I<sup>2</sup>C Port Timing Specifications<sup>1, 2</sup>

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCL clock frequency		400	kHz

1. MachXO3L/LF supports the following modes:

• Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)

• Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)

2. Refer to the  $I^2C$  specification for timing requirements.

### SPI Port Timing Specifications<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	Maximum SCK clock frequency		45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

### **Switching Test Conditions**

Figure 3-9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

#### Figure 3-9. Output Test Load, LVTTL and LVCMOS Standards



Table 3-6. Test Fixture Required Components	, Non-Terminated Interfaces
---	-----------------------------

Test Condition	R1	CL	Timing Ref.	VT
			LVTTL, LVCMOS 3.3 = 1.5 V	_
		0pF	LVCMOS 2.5 = $V_{CCIO}/2$	_
LVTTL and LVCMOS settings (L -> H, H -> L)	$\infty$		LVCMOS 1.8 = $V_{CCIO}/2$	
			LVCMOS 1.5 = $V_{CCIO}/2$	_
			LVCMOS 1.2 = $V_{CCIO}/2$	_
LVTTL and LVCMOS 3.3 (Z -> H)			1.5	V <sub>OL</sub>
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V <sub>OH</sub>
Other LVCMOS (Z -> H)	188	0nE	V <sub>CCIO</sub> /2	V <sub>OL</sub>
Other LVCMOS (Z -> L) LVTTL + LVCMOS (H -> Z)	100	орі	V <sub>CCIO</sub> /2	V <sub>OH</sub>
			V <sub>OH</sub> - 0.15	V <sub>OL</sub>
LVTTL + LVCMOS (L -> Z)			V <sub>OL</sub> - 0.15	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.



## MachXO3 Family Data Sheet Pinout Information

February 2017

Advance Data Sheet DS1047

### **Signal Descriptions**

Signal Name	I/O	Descriptions			
General Purpose					
		[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).			
		[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.			
		[A/B/C/D] indicates the PIO within the group to which the pad is connected.			
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.			
		uring configuration of the user-programmable I/Os, the user has an option to tri-state the Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies unused pins (or those not bonded to a package pin). The default during configuration is for ser-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the evice is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, uch as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled hen the device is erased.			
NC	—	No connect.			
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.			
VCC	_	$V_{CC}$ – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.			
VCCIOx	_	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.			
PLL and Clock Functi	ons (Us	ed as user-programmable I/O pins when not used for PLL or clock pins)			
[LOC]_GPLL[T, C]_IN	_	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.			
[LOC]_GPLL[T, C]_FB	_	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.			
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.			
Test and Programmin	<b>g</b> (Dual f	function pins used for test access port and during sysCONFIG™)			
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.			
ТСК	I	Test Clock input pin, used to clock the 1149.1 state machine.			
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.			
TDO	0	Output pin – Test Data output pin used to shift data out of the device using 1149.1.			
		Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:			
JTAGENB	I	If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.			
		If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.			
		For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.			

© 2017 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



### **Pin Information Summary**

	MachXO3L/LF -640	MachXO3L/LF-1300			
	CSFBGA121	WLCSP36	CSFBGA121	CSFBGA256	CABGA256
General Purpose IO per Bank					
Bank 0	24	15	24	50	50
Bank 1	26	0	26	52	52
Bank 2	26	9	26	52	52
Bank 3	24	4	24	16	16
Bank 4	0	0	0	16	16
Bank 5	0	0	0	20	20
Total General Purpose Single Ended IO	100	28	100	206	206
Differential IO per Bank		•		•	•
Bank 0	12	8	12	25	25
Bank 1	13	0	13	26	26
Bank 2	13	4	13	26	26
Bank 3	11	2	11	8	8
Bank 4	0	0	0	8	8
Bank 5	0	0	0	10	10
Total General Purpose Differential IO	49	14	49	103	103
Dual Function IO	33	25	33	33	33
Number 7:1 or 8:1 Gearboxes	<u>.</u>				
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	7	3	7	14	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	7	2	7	14	14
High-speed Differential Outputs					
Bank 0	7	3	7	14	14
VCCIO Pins					
Bank 0	1	1	1	4	4
Bank 1	1	0	1	3	4
Bank 2	1	1	1	4	4
Bank 3	3	1	3	2	1
Bank 4	0	0	0	2	2
Bank 5	0	0	0	2	1
vcc	4	2	4	8	8
GND	10	2	10	24	24
NC	0	0	0	0	1
Reserved for Configuration	1	1	1	1	1
Total Count of Bonded Pins	121	36	121	256	256



# MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-5MG1211	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND
Part Number	l IITe	Supply Voltage	Sneed	Package	abea I	Tomn

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-5MG121I	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-6MG121I	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300C-5BG256C	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-6BG256C	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-5BG256I	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-1300C-6BG256I	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-6MG121I	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND



Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	СОМ
LCMXO3LF-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND



# MachXO3 Family Data Sheet Revision History

#### February 2017

Advance Data Sheet DS1047

Date	Version	Section	Change Summary
February 2017	1.8	Architecture	Updated Supported Standards section. Corrected "MDVS" to "MLDVS" in Table 2-11, Supported Input Standards.
		DC and Switching Characteristics	Updated ESD Performance section. Added reference to the MachXO2 Product Family Qualification Summary document.
			Updated Static Supply Current – C/E Devices section. Added footnote 7.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. — Populated values for MachXO3L/LF-9400. — Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, corrected "t <sub>DVB</sub> " to "t <sub>DIB</sub> " and "t <sub>DVA</sub> " to "t <sub>DIA</sub> " and revised their descriptions. — Added Figure 3-6, Receiver GDDR71_RX Waveforms and Figure 3-7, Transmitter GDDR71_TX Waveforms.
		Pinout Information	Updated the Pin Information Summary section. Added MachXO3L/LF- 9600C packages.
May 2016	1.7	DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Modified I/O Tri-state Volt- age Applied and Dedicated Input Voltage Applied footnotes.
			Updated sysIO Recommended Operating Conditions section. — Added standards. — Added V <sub>REF</sub> (V) — Added footnote 4.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Added I/O standards.
		Ordering Information	Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.

<sup>© 2017</sup> Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



Date	Version	Section	Change Summary
September 2015	1.5	DC and Switching Characteristics	Updated the MIPI D-PHY Emulation section. Revised Table 3-5, MIPI D- PHY Output DC Conditions. — Revised RL Typ. value. — Revised RH description and values.
			Updated the Maximum sysIO Buffer Performance section. Revised MIPI Max. Speed value.
			Updated the MachXO3L/LF External Switching Characteristics – C/E Devices section. Added footnotes 14 and 15.
August 2015	1.4	Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.
		Ordering Information	Updated the top side markings section to indicate the use of LMXO3LF for the LCMXO3LF device.
March 2015	1.3	All	General update. Added MachXO3LF devices.
October 2014	1.2	Introduction	Updated Table 1-1, MachXO3L Family Selection Guide. Revised XO3L- 2100 and XO3L-4300 IO for 324-ball csfBGA package.
		Architecture	Updated the Dual Boot section. Corrected information on where the pri- mary bitstream and the golden image must reside.
		Pinout Information	Updated the Pin Information Summary section.
			Changed General Purpose IO Bank 5 values for MachXO3L-2100 and MachXO3L-4300 CSFBGA 324 package.
			Changed Number 7:1 or 8:1 Gearboxes for MachXO3L-640 and MachXO3L-1300.
			Removed DQS Groups (Bank 1) section.
			Changed VCCIO Pins Bank 1 values for MachXO3L-1300, MachXO3L- 2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.
			Changed GND values for MachXO3L-1300, MachXO3L-2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.
			Changed NC values for MachXO3L-2100 and MachXO3L-4300 CSF- BGA 324 package.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	1.1	DC and Switching Characteristics	Updated the Static Supply Current – C/E Devices section. Added devices.
			Updated the Programming and Erase Supply Current – C/E Device section. Added devices.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Revised footnote 4.
			Added the NVCM Download Time section.
			Updated the Typical Building Block Function Performance – C/E Devices section. Added information to footnote.
		Pinout Information	Updated the Pin Information Summary section.
		Ordering Information	Updated the MachXO3L Part Number Description section. Added packages.
			Updated the Ordering Information section. General update.