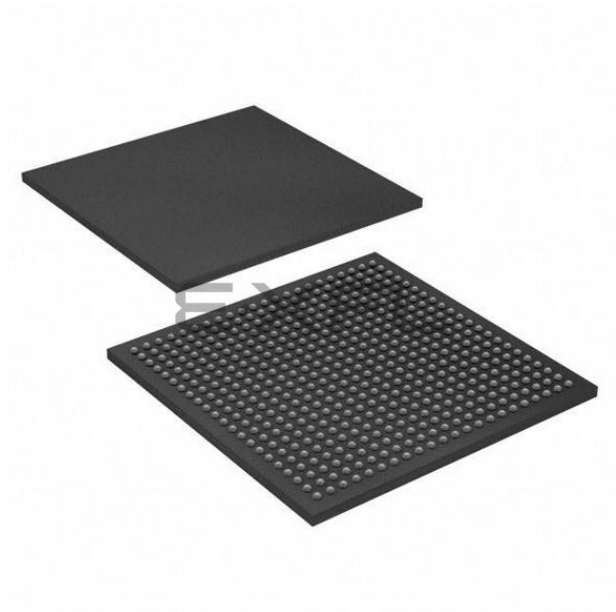
Lattice Semiconductor Corporation - LCMXO3L-9400C-5BG484I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1175
Number of Logic Elements/Cells	9400
Total RAM Bits	442368
Number of I/O	384
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-LFBGA
Supplier Device Package	484-CABGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-9400c-5bg484i

Table 1-1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900	9400
Distributed RAM (kbits)		5	10	16	34	54	73
EBR SRAM (kbits)		64	64	74	92	240	432
Number of PLLs		1	1	1	2	2	2
Hardened Functions:	I^2C	2	2	2	2	2	2
	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY Support		Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Programmable NVCM		MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400
Packages				**IO**			
36-ball WLCSP[1] (2.5 mm x 2.5 mm, 0.4 mm)			28				
49-ball WLCSP[1] (3.2 mm x 3.2 mm, 0.4 mm)				38			
81-ball WLCSP[1] (3.8 mm x 3.8 mm, 0.4 mm)					63		
121-ball csfBGA[1] (6 mm x 6 mm, 0.5 mm)		100	100	100	100		
256-ball csfBGA[1] (9 mm x 9 mm, 0.5 mm)			206	206	206	206	206
324-ball csfBGA[1] (10 mm x 10 mm, 0.5 mm)				268	268	281	
256-ball caBGA[2] (14 mm x 14 mm, 0.8 mm)			206	206	206	206	206
324-ball caBGA[2] (15 mm x 15 mm, 0.8 mm)				279	279	279	
400-ball caBGA[2] (17 mm x 17 mm, 0.8 mm)					335	335	335
484-ball caBGA[2] (19 mm x 19 mm, 0.8 mm)							384

1. Package is only available for E=1.2 V devices.
2. Package is only available for C=2.5 V/3.3 V devices.

Introduction

MachXO3™ device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I^2C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode
In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode
Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  — A greater-than-or-equal-to B
  — A not-equal-to B
  — A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3L/LF devices support distributed memory initialization.

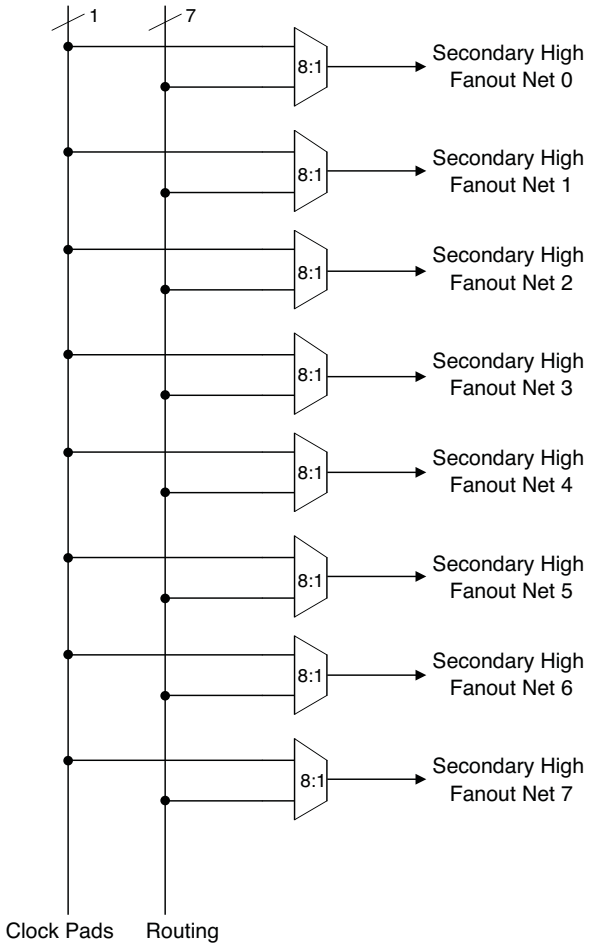
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO3L/LF devices, please see TN1290, Memory Usage Guide for MachXO3 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

Figure 2-6. Secondary High Fanout Nets for MachXO3L/LF Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO3L/LF devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO3L/LF sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO3L/LF clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO3L/LF devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE[1]	Output Clock Enable	Active High
RST	Reset	Active High
BE[1]	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.

3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

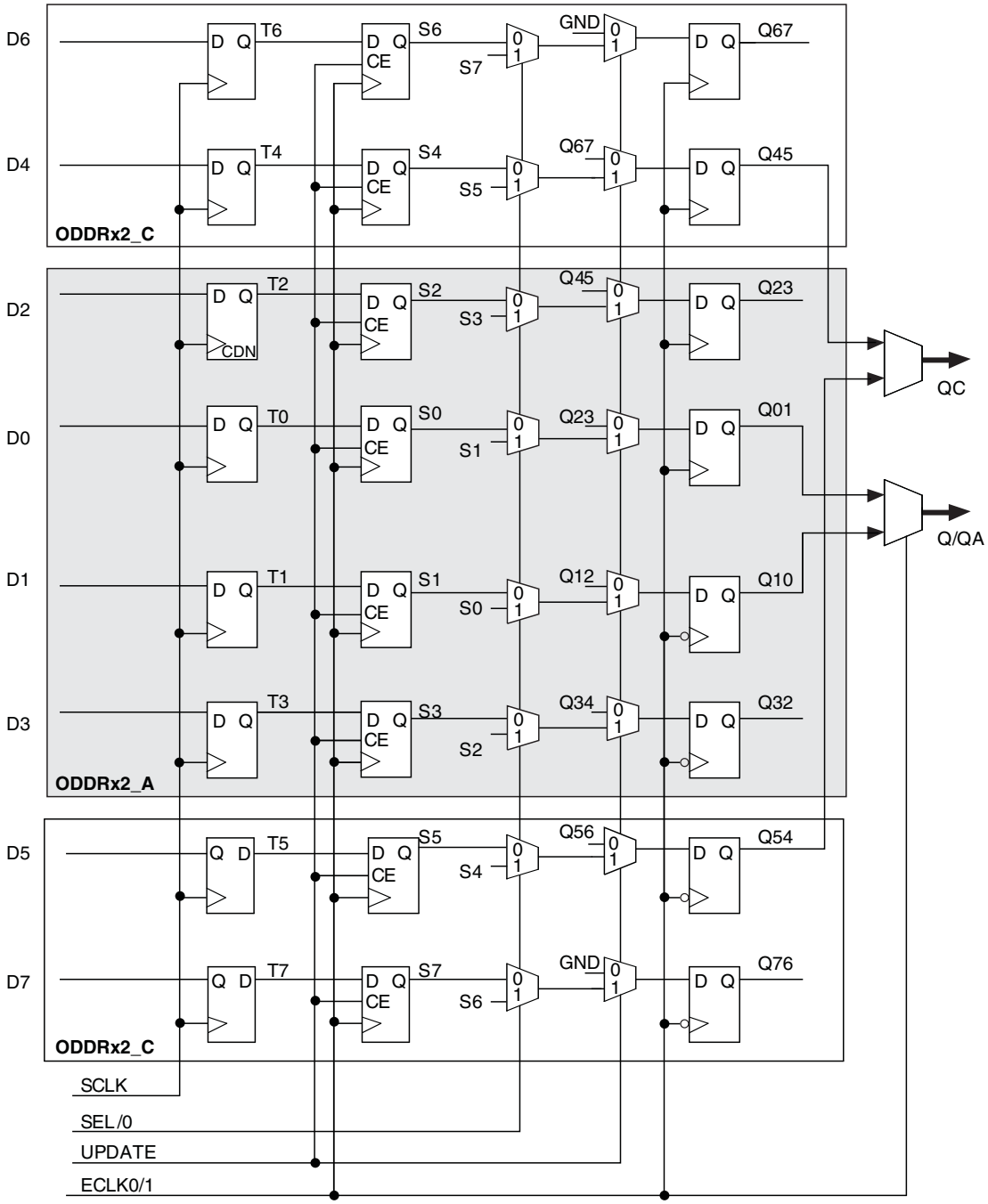
Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset

Figure 2-14. Output Gearbox



More information on the output gearbox is available in TN1281, Implementing High-Speed Interfaces with MachXO3 Devices.

There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1293, Using Hardened Control Functions in MachXO3 Devices

Figure 2-19. SPI Core Block Diagram

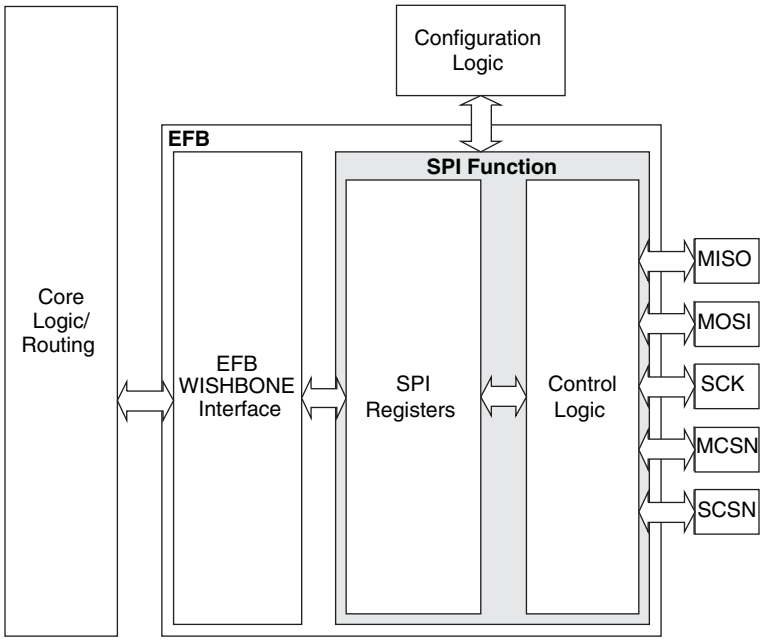


Table 2-15 describes the signals interfacing with the SPI cores.

Table 2-15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Configuration Logic.
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

For more details on these embedded functions, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

User Flash Memory (UFM)

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

Standby Mode and Power Saving Options

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the E devices operate at 1.2 V V_{CC}.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I^2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Power-On-Reset Voltage Levels[1, 2, 3, 4, 5]

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
3. Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
4. $V_{PORUPEXT}$ is for C devices only. In these devices a separate POR circuit monitors the external V_{CC} power supply.
5. V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	µA

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the MachXO2 Product Family Qualification Summary for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	µA
		Clamp OFF and V_{CCIO} - 0.97 V < V_{IN} < V_{CCIO}	–175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} - 0.97 V	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	µA
		Clamp ON and 0 V < $V_{IN} < V_{CCIO}$	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	–30	—	–309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < $V_{IN} < V_{CCIO}$	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points		V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5.5	7	pf
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For true LVDS output pins in MachXO3L/LF devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to TN1280, MachXO3 sysIO Usage Guide.

Static Supply Current – C/E Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Units
I_{CC}	Core Power Supply	LCMXO3L/LF-1300C 256 Ball Package	4.8	mA
		LCMXO3L/LF-2100C	4.8	mA
		LCMXO3L/LF-2100C 324 Ball Package	8.45	mA
		LCMXO3L/LF-4300C	8.45	mA
		LCMXO3L/LF-4300C 400 Ball Package	12.87	mA
		LCMXO3L/LF-6900C[7]	12.87	mA
		LCMXO3L/LF-9400C[7]	17.86	mA
		LCMXO3L/LF-640E	1.00	mA
		LCMXO3L/LF-1300E	1.00	mA
		LCMXO3L/LF-1300E 256 Ball Package	1.39	mA
		LCMXO3L/LF-2100E	1.39	mA
		LCMXO3L/LF-2100E 324 Ball Package	2.55	mA
		LCMXO3L/LF-4300E	2.55	mA
		LCMXO3L/LF-6900E	4.06	mA
		LCMXO3L/LF-9400E	5.66	mA
I_{CCIO}	Bank Power Supply[5] VCCIO = 2.5 V	All devices	0	mA

1. For further information on supply current, please refer to TN1289, Power Estimation and Management for MachXO3 Devices.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO3L/LF peak start-up current data, use the Power Calculator tool.
7. Determination of safe ambient operating conditions requires use of the Diamond Power Calculator tool.

Table 3-5. MIPI D-PHY Output DC Conditions[1]

	Description	Min.	Typ.	Max.	Units
Transmitter					
External Termination					
RL	1% external resistor with VCCIO = 2.5 V	—	50	—	Ohms
	1% external resistor with VCCIO = 3.3 V	—	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	—	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	—	464	—	Ohms
High Speed					
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	—	2.5	—	V
	VCCIO of the Bank with LVDS Emulated output buffer	—	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage	—	—	360	V
ZOS	Single ended output impedance	—	50	—	Ohms
ΔZOS	Single ended output impedance mismatch	—	—	10	%
Low Power					
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	—	1.2	—	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	–50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

1. Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Edge Clock without PLL)							
t_{COE}	Clock to Output - PIO Output Register	MachXO3L/LF-1300	—	7.53	—	7.76	ns
		MachXO3L/LF-2100	—	7.53	—	7.76	ns
		MachXO3L/LF-4300	—	7.45	—	7.68	ns
		MachXO3L/LF-6900	—	7.53	—	7.76	ns
		MachXO3L/LF-9400	—	8.93	—	9.35	ns
t_{SUE}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-1300	–0.19	—	–0.19	—	ns
		MachXO3L/LF-2100	–0.19	—	–0.19	—	ns
		MachXO3L/LF-4300	–0.16	—	–0.16	—	ns
		MachXO3L/LF-6900	–0.19	—	–0.19	—	ns
		MachXO3L/LF-9400	–0.20	—	–0.20	—	ns
t_{HE}	Clock to Data Hold - PIO Input Register	MachXO3L/LF-1300	1.97	—	2.24	—	ns
		MachXO3L/LF-2100	1.97	—	2.24	—	ns
		MachXO3L/LF-4300	1.89	—	2.16	—	ns
		MachXO3L/LF-6900	1.97	—	2.24	—	ns
		MachXO3L/LF-9400	1.98	—	2.25	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	1.56	—	1.69	—	ns
		MachXO3L/LF-2100	1.56	—	1.69	—	ns
		MachXO3L/LF-4300	1.74	—	1.88	—	ns
		MachXO3L/LF-6900	1.66	—	1.81	—	ns
		MachXO3L/LF-9400	1.71	—	1.85	—	ns
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-2100	–0.23	—	–0.23	—	ns
		MachXO3L/LF-4300	–0.34	—	–0.34	—	ns
		MachXO3L/LF-6900	–0.29	—	–0.29	—	ns
		MachXO3L/LF-9400	–0.30	—	–0.30	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)							
t_{COPLL}	Clock to Output - PIO Output Register	MachXO3L/LF-1300	—	5.98	—	6.01	ns
		MachXO3L/LF-2100	—	5.98	—	6.01	ns
		MachXO3L/LF-4300	—	5.99	—	6.02	ns
		MachXO3L/LF-6900	—	6.02	—	6.06	ns
		MachXO3L/LF-9400	—	5.55	—	6.13	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-1300	0.36	—	0.36	—	ns
		MachXO3L/LF-2100	0.36	—	0.36	—	ns
		MachXO3L/LF-4300	0.35	—	0.35	—	ns
		MachXO3L/LF-6900	0.34	—	0.34	—	ns
		MachXO3L/LF-9400	0.33	—	0.33	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	MachXO3L/LF-1300	0.42	—	0.49	—	ns
		MachXO3L/LF-2100	0.42	—	0.49	—	ns
		MachXO3L/LF-4300	0.43	—	0.50	—	ns
		MachXO3L/LF-6900	0.46	—	0.54	—	ns
		MachXO3L/LF-9400	0.47	—	0.55	—	ns

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	2.87	—	3.18	—	ns
		MachXO3L/LF-2100	2.87	—	3.18	—	ns
		MachXO3L/LF-4300	2.96	—	3.28	—	ns
		MachXO3L/LF-6900	3.05	—	3.35	—	ns
		MachXO3L/LF-9400	3.06	—	3.37	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.83	—	–0.83	—	ns
		MachXO3L/LF-2100	–0.83	—	–0.83	—	ns
		MachXO3L/LF-4300	–0.87	—	–0.87	—	ns
		MachXO3L/LF-6900	–0.91	—	–0.91	—	ns
		MachXO3L/LF-9400	–0.93	—	–0.93	—	ns

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[8, 9]							
t_{DVB}	Output Data Valid Before CLK Output	MachXO3L/LF devices, top side only	0.455	—	0.570	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	400	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[8, 9]							
t_{DIB}	Output Data Invalid Before CLK Output	MachXO3L/LF devices, top side only	—	0.160	—	0.180	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_TX.ECLK.Centered[10, 11, 12]							
t_{DVB}	Output Data Valid Before CLK Output	All MachXO3L/LF devices, top side only	0.200	—	0.200	—	UI
t_{DVA}	Output Data Valid After CLK Output		0.200	—	0.200	—	UI
f_{DATA}[14]	MIPI D-PHY Output Data Speed		—	900	—	900	Mbps
f_{DDRX4}[14]	MIPI D-PHY ECLK Frequency (minimum limited by PLL)		—	450	—	450	MHz
f_{SCLK}[14]	SCLK Frequency		—	112.5	—	112.5	MHz

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
5. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03\ ns)/2$.
6. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
7. This number for general purpose usage. Duty cycle tolerance is +/–10%.
8. Duty cycle is +/– 5% for system usage.
9. Performance is calculated with 0.225 UI.
10. Performance is calculated with 0.20 UI.
11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.
12. Performance for Industrial devices and –5 devices are not modeled in the Diamond design tool.
13. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
14. Above 800 Mbps is only supported with WLCSP and csfBGA packages
15. Between 800 Mbps to 900 Mbps:
    a. VIDTH exceeds the MIPI D-PHY Input DC Conditions Table 3-4 and can be calculated with the equation tSU or tH = -0.0005*VIDTH + 0.3284
    b. Example calculations
        i. tSU and tHO = 0.28 with VIDTH = 100 mV
        ii. tSU and tHO = 0.25 with VIDTH = 170 mV
        iii. tSU and tHO = 0.20 with VIDTH = 270 mV

	MachXO3L/LF-4300						
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank							
Bank 0	29	24	50	71	50	71	83
Bank 1	0	26	52	62	52	68	84
Bank 2	20	26	52	72	52	72	84
Bank 3	7	7	16	22	16	24	28
Bank 4	0	7	16	14	16	16	24
Bank 5	7	10	20	27	20	28	32
Total General Purpose Single Ended IO	63	100	206	268	206	279	335
Differential IO per Bank							
Bank 0	15	12	25	36	25	36	42
Bank 1	0	13	26	30	26	34	42
Bank 2	10	13	26	36	26	36	42
Bank 3	3	3	8	10	8	12	14
Bank 4	0	3	8	6	8	8	12
Bank 5	3	5	10	13	10	14	16
Total General Purpose Differential IO	31	49	103	131	103	140	168
Dual Function IO	25	37	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21
High-speed Differential Outputs							
Bank 0	10	7	18	18	18	18	21
VCCIO Pins							
Bank 0	3	1	4	4	4	4	5
Bank 1	0	1	3	4	4	4	5
Bank 2	2	1	4	4	4	4	5
Bank 3	1	1	2	2	1	2	2
Bank 4	0	1	2	2	2	2	2
Bank 5	1	1	2	2	1	2	2
VCC	4	4	8	8	8	10	10
GND	6	10	24	16	24	16	33
NC	0	0	0	13	1	0	0
Reserved for Configuration	1	1	1	1	1	1	1
Total Count of Bonded Pins	**81**	**121**	**256**	**324**	**256**	**324**	**400**

	MachXO3L/LF-6900				
	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank					
Bank 0	50	73	50	71	83
Bank 1	52	68	52	68	84
Bank 2	52	72	52	72	84
Bank 3	16	24	16	24	28
Bank 4	16	16	16	16	24
Bank 5	20	28	20	28	32
Total General Purpose Single Ended IO	206	281	206	279	335
Differential IO per Bank					
Bank 0	25	36	25	36	42
Bank 1	26	34	26	34	42
Bank 2	26	36	26	36	42
Bank 3	8	12	8	12	14
Bank 4	8	8	8	8	12
Bank 5	10	14	10	14	16
Total General Purpose Differential IO	103	140	103	140	168
Dual Function IO	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes					
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	21	20	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	21	20	21	21
High-speed Differential Outputs					
Bank 0	20	21	20	21	21
VCCIO Pins					
Bank 0	4	4	4	4	5
Bank 1	3	4	4	4	5
Bank 2	4	4	4	4	5
Bank 3	2	2	1	2	2
Bank 4	2	2	2	2	2
Bank 5	2	2	1	2	2
VCC	8	8	8	10	10
GND	24	16	24	16	33
NC	0	0	1	0	0
Reserved for Configuration	1	1	1	1	1
Total Count of Bonded Pins	**256**	**324**	**256**	**324**	**400**

	MachXO3L/LF-9400C			
	CSFBGA256	CABGA256	CABGA400	CABGA484
General Purpose IO per Bank				
Bank 0	50	50	83	95
Bank 1	52	52	84	96
Bank 2	52	52	84	96
Bank 3	16	16	28	36
Bank 4	16	16	24	24
Bank 5	20	20	32	36
Total General Purpose Single Ended IO	206	206	335	383
Differential IO per Bank				
Bank 0	25	25	42	48
Bank 1	26	26	42	48
Bank 2	26	26	42	48
Bank 3	8	8	14	18
Bank 4	8	8	12	12
Bank 5	10	10	16	18
Total General Purpose Differential IO	103	103	168	192
Dual Function IO	37	37	37	45
Number 7:1 or 8:1 Gearboxes				
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	20	22	24
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	20	22	24
High-speed Differential Outputs				
Bank 0	20	20	21	24
VCCIO Pins				
Bank 0	4	4	5	9
Bank 1	3	4	5	9
Bank 2	4	4	5	9
Bank 3	2	1	2	3
Bank 4	2	2	2	3
Bank 5	2	1	2	3
VCC	8	8	10	12
GND	24	24	33	52
NC	0	1	0	0
Reserved for Configuration	1	1	1	1
Total Count of Bonded Pins	**256**	**256**	**400**	**484**

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Date	Version	Section	Change Summary
June 2014	1.0	—	Product name/trademark adjustment.
		Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Changed fcCSP packages to csfBGA. Adjusted 121-ball csfBGA arrow.
			Introduction section general update.
		Architecture	General update.
		DC and Switching Characteristics	Updated sysIO Recommended Operating Conditions section. Removed V_{REF} (V) column. Added standards.
			Updated Maximum sysIO Buffer Performance section. Added MIPI I/O standard.
			Updated MIPI D-PHY Emulation section. Changed Low Speed to Low Power. Updated Table 3-4, MIPI DC Conditions.
			Updated Table 3-5, MIPI D-PHY Output DC Conditions.
			Updated Maximum sysIO Buffer Performance section.
			Updated MachXO3L External Switching Characteristics – C/E Device section.
May 2014	00.3	Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Moved 121-ball fcCSP arrow.
			General update of Introduction section.
		Architecture	General update.
		Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
		Ordering Information	Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
			Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers.
February 2014	00.2	DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.
	00.1	—	Initial release.