# Lattice Semiconductor Corporation - LCMXO3L-9400E-6BG400C Datasheet



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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

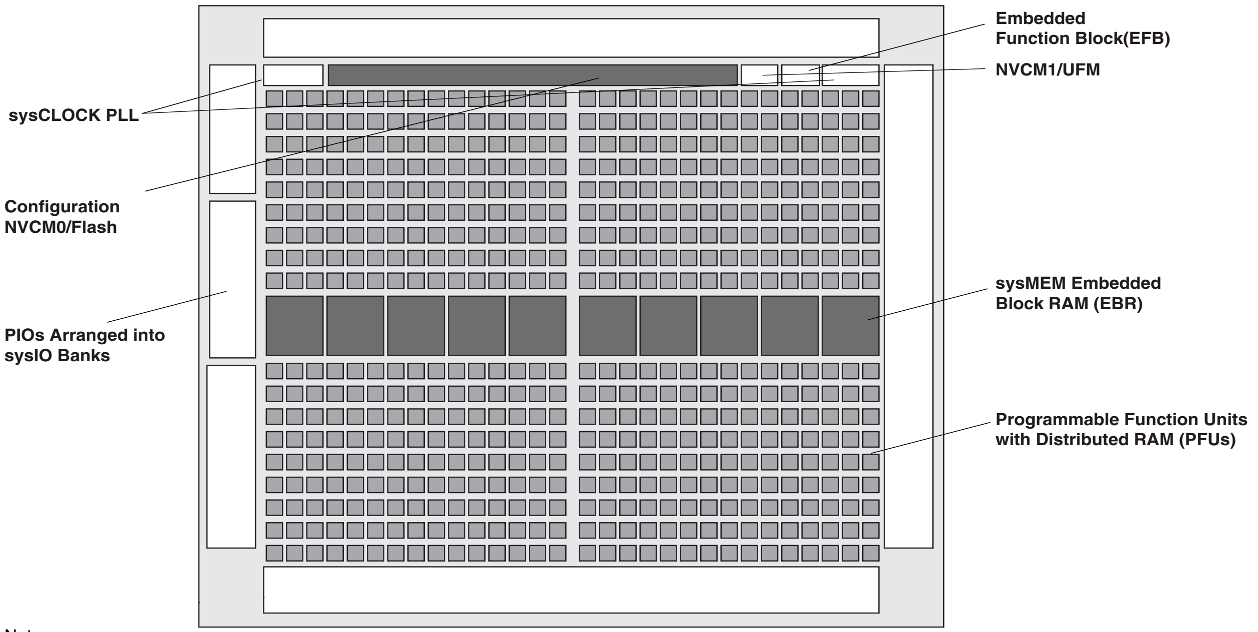
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1175 |
| Number of Logic Elements/Cells | 9400 |
| Total RAM Bits | 442368 |
| Number of I/O | 335 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 400-LFBGA |
| Supplier Device Package | 400-CABGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-9400e-6bg400c |

*Figure 2-2. Top View of the MachXO3L/LF-4300 Device*




Notes:
- MachXO3L/LF-1300, MachXO3L/LF-2100, MachXO3L/LF-6900 and MachXO3L/LF-9400 are similar to MachXO3L/LF-4300. MachXO3L/LF-1300 has a lower LUT count, one PLL, and seven EBR blocks. MachXO3L/LF-2100 has a lower LUT count, one PLL, and eight EBR blocks. MachXO3L/LF-6900 has a higher LUT count, two PLLs, and 26 EBR blocks. MachXO3L/LF-9400 has a higher LUT count, two PLLs, and 48 EBR blocks.
- MachXO3L devices have NVCM, MachXO3LF devices have Flash.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO3L/LF family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO3L/LF registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO3L/LF architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. These blocks are located at the ends of the on-chip NVCM/Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO3L/LF devices provide commonly used hardened functions such as SPI controller, I$^2$C controller and timer/counter.

MachXO3LF devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I$^2$C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO3L/LF devices are available for operation from 3.3 V, 2.5 V and 1.2 V power sup-plies, providing easy integration into the overall system.

*Table 2-4. PLL Signal Descriptions (Continued)*

| Port Name | I/O | Description |
|---|---|---|
| CLKOP | O | Primary PLL output clock (with phase shift adjustment) |
| CLKOS | O | Secondary PLL output clock (with phase shift adjust) |
| CLKOS2 | O | Secondary PLL output clock2 (with phase shift adjust) |
| CLKOS3 | O | Secondary PLL output clock3 (with phase shift adjust) |
| LOCK | O | PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed-back signals. |
| DPHSRC | O | Dynamic Phase source – ports or WISHBONE is active |
| STDBY | I | Standby signal to power down the PLL |
| RST | I | PLL reset without resetting the M-divider. Active high reset. |
| RESETM | I | PLL reset - includes resetting the M-divider. Active high reset. |
| RESETC | I | Reset for CLKOS2 output divider only. Active high reset. |
| RESETD | I | Reset for CLKOS3 output divider only. Active high reset. |
| ENCLKOP | I | Enable PLL output CLKOP |
| ENCLKOS | I | Enable PLL output CLKOS when port is active |
| ENCLKOS2 | I | Enable PLL output CLKOS2 when port is active |
| ENCLKOS3 | I | Enable PLL output CLKOS3 when port is active |
| PLLCLK | I | PLL data bus clock input signal |
| PLLRST | I | PLL data bus reset. This resets only the data bus not any register values. |
| PLLSTB | I | PLL data bus strobe signal |
| PLLWE | I | PLL data bus write enable signal |
| PLLADDR [4:0] | I | PLL data bus address |
| PLLDATI [7:0] | I | PLL data bus data input |
| PLLDATO [7:0] | O | PLL data bus data output |
| PLLACK | O | PLL data bus acknowledge signal |

## sysMEM Embedded Block RAM Memory

The MachXO3L/LF devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.

## Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

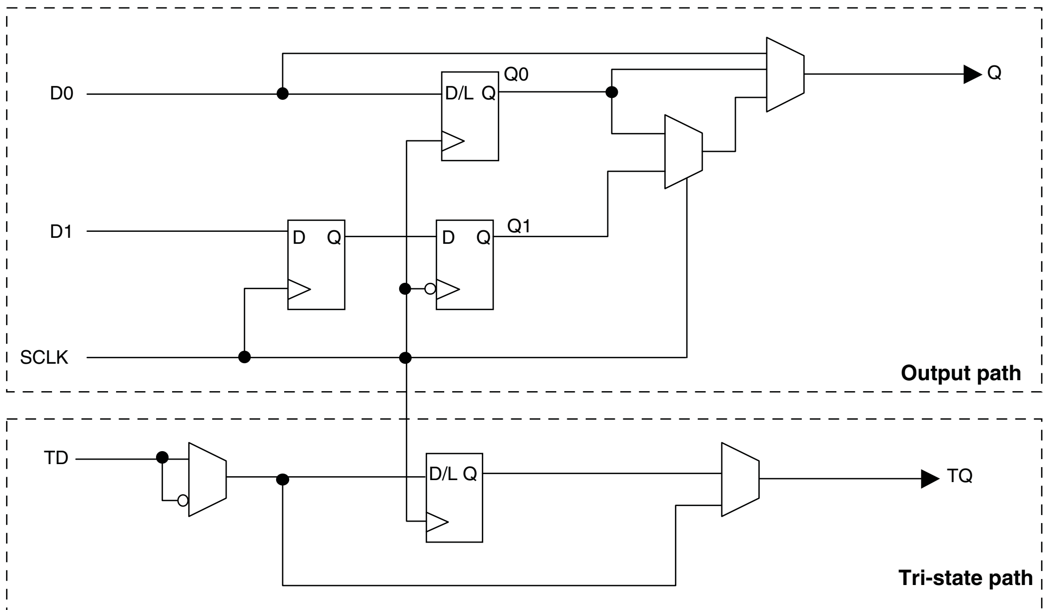
**Left, Top, Bottom Edges**

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-12 shows the output register block on the left, top and bottom edges.

***Figure 2-12. MachXO3L/LF Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)***




## Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

## Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
  - — Watchdog timer
  - — Clear timer on compare match
  - — Fast PWM
  - — Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

***Figure 2-20. Timer/Counter Block Diagram***

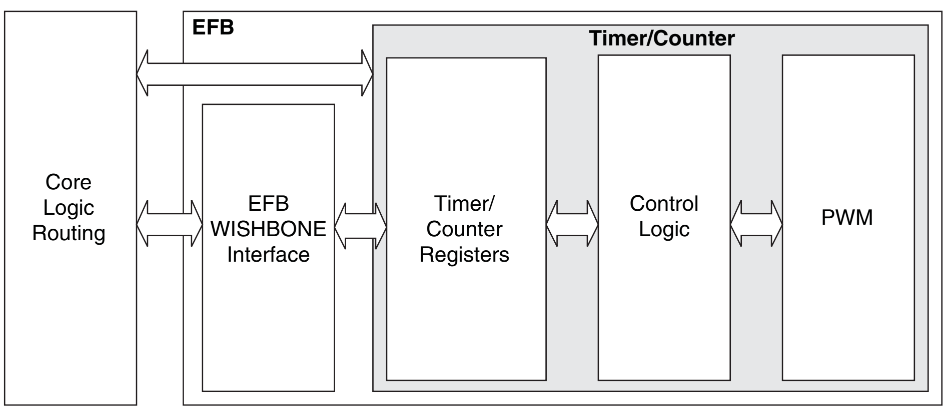



***Table 2-16. Timer/Counter Signal Description***

| Port | I/O | Description |
|---|---|---|
| tc_clki | I | Timer/Counter input clock signal |
| tc_rstn | I | Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled |
| tc_ic | I | Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping. |
| tc_int | O | Without WISHBONE – Can be used as overflow flag<br>With WISHBONE – Controlled by three IRQ registers |
| tc_oc | O | Timer counter output signal |

*Table 2-17. MachXO3L/LF Power Saving Features Description*

| Device Subsystem | Feature Description |
|---|---|
| Bandgap | The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices. |
| Power-On-Reset (POR) | The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe $V_{CC}$ drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable. |
| On-Chip Oscillator | The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode. |
| PLL | Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off. |
| I/O Bank Controller | Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection. |
| Dynamic Clock Enable for Primary Clock Nets | Each primary clock net can be dynamically disabled to save power. |
| Power Guard | Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources. |

For more details on the standby mode refer to TN1289, Power Estimation and Management for MachXO3 Devices.

## Power On Reset

MachXO3L/LF devices have power-on reset circuitry to monitor $V_{CCINT}$ and $V_{CCIO}$ voltage levels during power-up and operation. At power-up, the POR circuitry monitors $V_{CCINT}$ and $V_{CCIO0}$ (controls configuration) voltage levels. It then triggers download from the on-chip configuration NVCM/Flash memory after reaching the $V_{PORUP}$ level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For "E" devices without voltage regulators, $V_{CCINT}$ is the same as the $V_{CC}$ supply voltage. For "C" devices with voltage regulators, $V_{CCINT}$ is regulated from the $V_{CC}$ supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as NVCM/Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration. Note that for "C" devices, a separate POR circuit monitors external $V_{CC}$ voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor $V_{CCINT}$ levels. If $V_{CCINT}$ drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the $V_{CCINT}$ and $V_{CCIO}$ voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once an "E" device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a mini-mal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the $V_{CC}$ supply dropping below $V_{CC}$ (min) they should not shut down the bandgap or POR circuit.

## Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with $V_{CCIO}$ Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

### Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through $I^2C$ or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

1. Internal NVCM/Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard $I^2C$ Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, MachXO3 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

**TransFR (Transparent Field Reconfiguration)**

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

### Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and NVCM/Flash spaces is allowed.

2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

### Password

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to TN1313, Using Password Security with MachXO3 Devices.

### Dual Boot

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

### Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1292, MachXO3 Soft Error Detection Usage Guide.

### Soft Error Correction

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to TN1292, MachXO3 Soft Error Detection (SED)/Correction (SEC) Usage Guide.

## sysIO Single-Ended DC Electrical Characteristics[1, 2]

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$ Max.[4] (mA) | $I_{OH}$ Max.[4] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V)[3] | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 LVTTL | –0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 4 | –4 |
| | | | | | | | 8 | –8 |
| | | | | | | | 12 | –12 |
| | | | | | | | 16 | –16 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS 2.5 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 4 | –4 |
| | | | | | | | 8 | –8 |
| | | | | | | | 12 | –12 |
| | | | | | | | 16 | –16 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS 1.8 | –0.3 | 0.35$V_{CCIO}$ | 0.65$V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 4 | –4 |
| | | | | | | | 8 | –8 |
| | | | | | | | 12 | –12 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS 1.5 | –0.3 | 0.35$V_{CCIO}$ | 0.65$V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 4 | –4 |
| | | | | | | | 8 | –8 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS 1.2 | –0.3 | 0.35$V_{CCIO}$ | 0.65$V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 4 | –2 |
| | | | | | | | 8 | –6 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| LVCMOS25R33 | –0.3 | VREF–0.1 | VREF+0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS18R33 | –0.3 | VREF–0.1 | VREF+0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS18R25 | –0.3 | VREF–0.1 | VREF+0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS15R33 | –0.3 | VREF–0.1 | VREF+0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS15R25 | –0.3 | VREF–0.1 | VREF+0.1 | 3.6 | NA | NA | NA | NA |
| LVCMOS12R33 | –0.3 | VREF–0.1 | VREF+0.1 | 3.6 | 0.40 | NA Open Drain | 24, 16, 12, 8, 4 | NA Open Drain |
| LVCMOS12R25 | –0.3 | VREF–0.1 | VREF+0.1 | 3.6 | 0.40 | NA Open Drain | 16, 12, 8, 4 | NA Open Drain |
| LVCMOS10R33 | –0.3 | VREF–0.1 | VREF+0.1 | 3.6 | 0.40 | NA Open Drain | 24, 16, 12, 8, 4 | NA Open Drain |
| LVCMOS10R25 | -0.3 | VREF-0.1 | VREF+0.1 | 3.6 | 0.40 | NA Open Drain | 16, 12, 8, 4 | NA Open Drain |

1. MachXO3L/LF devices allow LVCMOS inputs to be placed in I/O banks where $V_{CCIO}$ is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO3L/LF devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO3L/LF devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1280, MachXO3 sysIO Usage Guide.
3. The dual function $I^2C$ pins SCL and SDA are limited to a $V_{IL}$ min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.

## sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

### LVDS

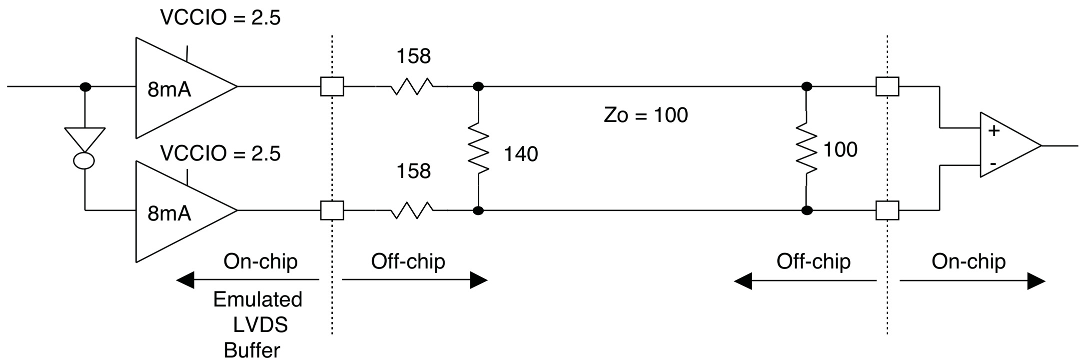
**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$ = 3.3 V | 0 | — | 2.605 | V |
| | | $V_{CCIO}$ = 2.5 V | 0 | — | 2.05 | V |
| $V_{THD}$ | Differential Input Threshold | | ±100 | — | | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$ = 3.3 V | 0.05 | — | 2.6 | V |
| | | $V_{CCIO}$ = 2.5 V | 0.05 | — | 2.0 | V |
| $I_{IN}$ | Input current | Power on | — | — | ±10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | — | 1.375 | — | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | 0.90 | 1.025 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ohm | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ - $V_{OM}$)/2, $R_T$ = 100 Ohm | 1.125 | 1.20 | 1.395 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{OSD}$ | Output short circuit current | $V_{OD}$ = 0 V driver outputs shorted | — | — | 24 | mA |

## LVDS Emulation

MachXO3L/LF devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

*Figure 3-1. LVDS Using External Resistors (LVDS25E)*




Note: All resistors are ±1%.

*Table 3-1. LVDS25E DC Conditions*

**Over Recommended Operating Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 158 | Ohms |
| $R_P$ | Driver parallel resistor | 140 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ohms |
| $I_{DC}$ | DC output current | 6.03 | mA |

## MIPI D-PHY Emulation

MachXO3L/LF devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed IOs use the LVDS25E buffer and Low Power IOs use the LVCMOS buffers. The scheme shown in Figure 3-4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3-5 is one possible solution for MIPI D-PHY Transmitter implementation.

***Figure 3-4. MIPI D-PHY Input Using External Resistors***

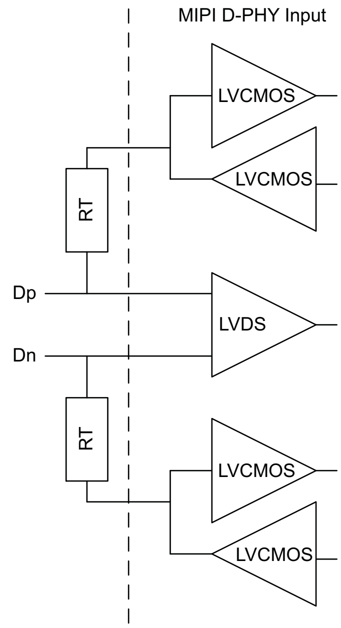



***Table 3-4. MIPI DC Conditions[1]***

| | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Receiver** | | | | | |
| **External Termination** | | | | | |
| RT | 1% external resistor with VCCIO=2.5 V | — | 50 | — | Ohms |
| | 1% external resistor with VCCIO=3.3 V | — | 50 | — | Ohms |
| **High Speed** | | | | | |
| VCCIO | VCCIO of the Bank with LVDS Emulated input buffer | — | 2.5 | — | V |
| | VCCIO of the Bank with LVDS Emulated input buffer | — | 3.3 | — | V |
| VCMRX | Common-mode voltage HS receive mode | 150 | 200 | 250 | mV |
| VIDTH | Differential input high threshold | — | — | 100 | mV |
| VIDTL | Differential input low threshold | –100 | — | — | mV |
| VIHHS | Single-ended input high voltage | — | — | 300 | mV |
| VILHS | Single-ended input low voltage | 100 | — | — | mV |
| ZID | Differential input impedance | 80 | 100 | 120 | Ohms |

*Table 3-5. MIPI D-PHY Output DC Conditions*[1]

| | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Transmitter** | | | | | |
| **External Termination** | | | | | |
| RL | 1% external resistor with VCCIO = 2.5 V | — | 50 | — | Ohms |
| | 1% external resistor with VCCIO = 3.3 V | — | 50 | — | |
| RH | 1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V | — | 330 | — | Ohms |
| | 1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V | — | 464 | — | Ohms |
| **High Speed** | | | | | |
| VCCIO | VCCIO of the Bank with LVDS Emulated output buffer | — | 2.5 | — | V |
| | VCCIO of the Bank with LVDS Emulated output buffer | — | 3.3 | — | V |
| VCMTX | HS transmit static common mode voltage | 150 | 200 | 250 | mV |
| VOD | HS transmit differential voltage | 140 | 200 | 270 | mV |
| VOHHS | HS output high voltage | — | — | 360 | V |
| ZOS | Single ended output impedance | — | 50 | — | Ohms |
| ΔZOS | Single ended output impedance mismatch | — | — | 10 | % |
| **Low Power** | | | | | |
| VCCIO | VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer | — | 1.2 | — | V |
| VOH | Output high level | 1.1 | 1.2 | 1.3 | V |
| VOL | Output low level | –50 | 0 | 50 | mV |
| ZOLP | Output impedance of LP transmitter | 110 | — | — | Ohms |

1. Over Recommended Operating Conditions

| Parameter | Description | Device | –6 Min. | –6 Max. | –5 Min. | –5 Max. | Units |
|---|---|---|---|---|---|---|---|
| **General I/O Pin Parameters (Using Edge Clock without PLL)** | | | | | | | |
| $t_{COE}$ | Clock to Output - PIO Output Register | MachXO3L/LF-1300 | — | 7.53 | — | 7.76 | ns |
| | | MachXO3L/LF-2100 | — | 7.53 | — | 7.76 | ns |
| | | MachXO3L/LF-4300 | — | 7.45 | — | 7.68 | ns |
| | | MachXO3L/LF-6900 | — | 7.53 | — | 7.76 | ns |
| | | MachXO3L/LF-9400 | — | 8.93 | — | 9.35 | ns |
| $t_{SUE}$ | Clock to Data Setup - PIO Input Register | MachXO3L/LF-1300 | –0.19 | — | –0.19 | — | ns |
| | | MachXO3L/LF-2100 | –0.19 | — | –0.19 | — | ns |
| | | MachXO3L/LF-4300 | –0.16 | — | –0.16 | — | ns |
| | | MachXO3L/LF-6900 | –0.19 | — | –0.19 | — | ns |
| | | MachXO3L/LF-9400 | –0.20 | — | –0.20 | — | ns |
| $t_{HE}$ | Clock to Data Hold - PIO Input Register | MachXO3L/LF-1300 | 1.97 | — | 2.24 | — | ns |
| | | MachXO3L/LF-2100 | 1.97 | — | 2.24 | — | ns |
| | | MachXO3L/LF-4300 | 1.89 | — | 2.16 | — | ns |
| | | MachXO3L/LF-6900 | 1.97 | — | 2.24 | — | ns |
| | | MachXO3L/LF-9400 | 1.98 | — | 2.25 | — | ns |
| $t_{SU\_DELE}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | MachXO3L/LF-1300 | 1.56 | — | 1.69 | — | ns |
| | | MachXO3L/LF-2100 | 1.56 | — | 1.69 | — | ns |
| | | MachXO3L/LF-4300 | 1.74 | — | 1.88 | — | ns |
| | | MachXO3L/LF-6900 | 1.66 | — | 1.81 | — | ns |
| | | MachXO3L/LF-9400 | 1.71 | — | 1.85 | — | ns |
| $t_{H\_DELE}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | MachXO3L/LF-1300 | –0.23 | — | –0.23 | — | ns |
| | | MachXO3L/LF-2100 | –0.23 | — | –0.23 | — | ns |
| | | MachXO3L/LF-4300 | –0.34 | — | –0.34 | — | ns |
| | | MachXO3L/LF-6900 | –0.29 | — | –0.29 | — | ns |
| | | MachXO3L/LF-9400 | –0.30 | — | –0.30 | — | ns |
| **General I/O Pin Parameters (Using Primary Clock with PLL)** | | | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | MachXO3L/LF-1300 | — | 5.98 | — | 6.01 | ns |
| | | MachXO3L/LF-2100 | — | 5.98 | — | 6.01 | ns |
| | | MachXO3L/LF-4300 | — | 5.99 | — | 6.02 | ns |
| | | MachXO3L/LF-6900 | — | 6.02 | — | 6.06 | ns |
| | | MachXO3L/LF-9400 | — | 5.55 | — | 6.13 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | MachXO3L/LF-1300 | 0.36 | — | 0.36 | — | ns |
| | | MachXO3L/LF-2100 | 0.36 | — | 0.36 | — | ns |
| | | MachXO3L/LF-4300 | 0.35 | — | 0.35 | — | ns |
| | | MachXO3L/LF-6900 | 0.34 | — | 0.34 | — | ns |
| | | MachXO3L/LF-9400 | 0.33 | — | 0.33 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | MachXO3L/LF-1300 | 0.42 | — | 0.49 | — | ns |
| | | MachXO3L/LF-2100 | 0.42 | — | 0.49 | — | ns |
| | | MachXO3L/LF-4300 | 0.43 | — | 0.50 | — | ns |
| | | MachXO3L/LF-6900 | 0.46 | — | 0.54 | — | ns |
| | | MachXO3L/LF-9400 | 0.47 | — | 0.55 | — | ns |

*Figure 3-6. Receiver GDDR71_RX. Waveforms*

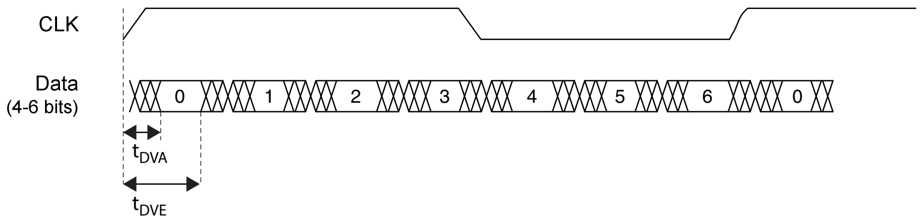
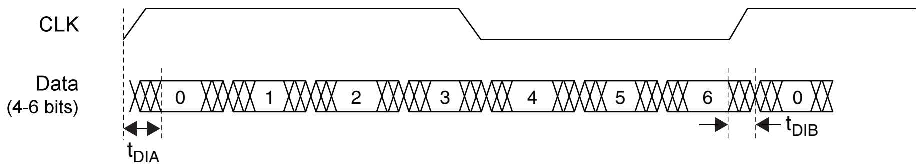



*Figure 3-7. Transmitter GDDR71_TX. Waveforms*



## NVCM/Flash Download Time[1, 2]

| Symbol | Parameter | Device | Typ. | Units |
|---|---|---|---|---|
| $t_{REFRESH}$ | POR to Device I/O Active | LCMXO3L/LF-640 | 1.9 | ms |
| | | LCMXO3L/LF-1300 | 1.9 | ms |
| | | LCMXO3L/LF-1300 256-Ball Package | 1.4 | ms |
| | | LCMXO3L/LF-2100 | 1.4 | ms |
| | | LCMXO3L/LF-2100 324-Ball Package | 2.4 | ms |
| | | LCMXO3L/LF-4300 | 2.4 | ms |
| | | LCMXO3L/LF-4300 400-Ball Package | 3.8 | ms |
| | | LCMXO3L/LF-6900 | 3.8 | ms |
| | | LCMXO3L/LF-9400C | 5.2 | ms |

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.
2. The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.

# Pin Information Summary

| | MachXO3L/LF -640 | MachXO3L/LF-1300 | | | |
|---|---|---|---|---|---|
| | CSFBGA121 | WLCSP36 | CSFBGA121 | CSFBGA256 | CABGA256 |
| **General Purpose IO per Bank** | | | | | |
| Bank 0 | 24 | 15 | 24 | 50 | 50 |
| Bank 1 | 26 | 0 | 26 | 52 | 52 |
| Bank 2 | 26 | 9 | 26 | 52 | 52 |
| Bank 3 | 24 | 4 | 24 | 16 | 16 |
| Bank 4 | 0 | 0 | 0 | 16 | 16 |
| Bank 5 | 0 | 0 | 0 | 20 | 20 |
| **Total General Purpose Single Ended IO** | 100 | 28 | 100 | 206 | 206 |
| **Differential IO per Bank** | | | | | |
| Bank 0 | 12 | 8 | 12 | 25 | 25 |
| Bank 1 | 13 | 0 | 13 | 26 | 26 |
| Bank 2 | 13 | 4 | 13 | 26 | 26 |
| Bank 3 | 11 | 2 | 11 | 8 | 8 |
| Bank 4 | 0 | 0 | 0 | 8 | 8 |
| Bank 5 | 0 | 0 | 0 | 10 | 10 |
| **Total General Purpose Differential IO** | 49 | 14 | 49 | 103 | 103 |
| **Dual Function IO** | 33 | 25 | 33 | 33 | 33 |
| **Number 7:1 or 8:1 Gearboxes** | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 7 | 3 | 7 | 14 | 14 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 7 | 2 | 7 | 14 | 14 |
| **High-speed Differential Outputs** | | | | | |
| Bank 0 | 7 | 3 | 7 | 14 | 14 |
| **VCCIO Pins** | | | | | |
| Bank 0 | 1 | 1 | 1 | 4 | 4 |
| Bank 1 | 1 | 0 | 1 | 3 | 4 |
| Bank 2 | 1 | 1 | 1 | 4 | 4 |
| Bank 3 | 3 | 1 | 3 | 2 | 1 |
| Bank 4 | 0 | 0 | 0 | 2 | 2 |
| Bank 5 | 0 | 0 | 0 | 2 | 1 |
| **VCC** | 4 | 2 | 4 | 8 | 8 |
| **GND** | 10 | 2 | 10 | 24 | 24 |
| **NC** | 0 | 0 | 0 | 0 | 1 |
| **Reserved for Configuration** | 1 | 1 | 1 | 1 | 1 |
| **Total Count of Bonded Pins** | **121** | **36** | **121** | **256** | **256** |

| | MachXO3L/LF-6900 | | | | |
|---|---|---|---|---|---|
| | CSFBGA256 | CSFBGA324 | CABGA256 | CABGA324 | CABGA400 |
| **General Purpose IO per Bank** | | | | | |
| Bank 0 | 50 | 73 | 50 | 71 | 83 |
| Bank 1 | 52 | 68 | 52 | 68 | 84 |
| Bank 2 | 52 | 72 | 52 | 72 | 84 |
| Bank 3 | 16 | 24 | 16 | 24 | 28 |
| Bank 4 | 16 | 16 | 16 | 16 | 24 |
| Bank 5 | 20 | 28 | 20 | 28 | 32 |
| **Total General Purpose Single Ended IO** | 206 | 281 | 206 | 279 | 335 |
| **Differential IO per Bank** | | | | | |
| Bank 0 | 25 | 36 | 25 | 36 | 42 |
| Bank 1 | 26 | 34 | 26 | 34 | 42 |
| Bank 2 | 26 | 36 | 26 | 36 | 42 |
| Bank 3 | 8 | 12 | 8 | 12 | 14 |
| Bank 4 | 8 | 8 | 8 | 8 | 12 |
| Bank 5 | 10 | 14 | 10 | 14 | 16 |
| **Total General Purpose Differential IO** | 103 | 140 | 103 | 140 | 168 |
| **Dual Function IO** | 37 | 37 | 37 | 37 | 37 |
| **Number 7:1 or 8:1 Gearboxes** | | | | | |
| Number of 7:1 or 8:1 Output Gearbox Available (Bank 0) | 20 | 21 | 20 | 21 | 21 |
| Number of 7:1 or 8:1 Input Gearbox Available (Bank 2) | 20 | 21 | 20 | 21 | 21 |
| **High-speed Differential Outputs** | | | | | |
| Bank 0 | 20 | 21 | 20 | 21 | 21 |
| **VCCIO Pins** | | | | | |
| Bank 0 | 4 | 4 | 4 | 4 | 5 |
| Bank 1 | 3 | 4 | 4 | 4 | 5 |
| Bank 2 | 4 | 4 | 4 | 4 | 5 |
| Bank 3 | 2 | 2 | 1 | 2 | 2 |
| Bank 4 | 2 | 2 | 2 | 2 | 2 |
| Bank 5 | 2 | 2 | 1 | 2 | 2 |
| **VCC** | 8 | 8 | 8 | 10 | 10 |
| **GND** | 24 | 16 | 24 | 16 | 33 |
| **NC** | 0 | 0 | 1 | 0 | 0 |
| **Reserved for Configuration** | 1 | 1 | 1 | 1 | 1 |
| **Total Count of Bonded Pins** | **256** | **324** | **256** | **324** | **400** |

## MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Speed | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO3L-640E-5MG121C | 640 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3L-640E-6MG121C | 640 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3L-640E-5MG121I | 640 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3L-640E-6MG121I | 640 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | IND |

| Part Number | LUTs | Supply Voltage | Speed | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO3L-1300E-5UWG36CTR | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | COM |
| LCMXO3L-1300E-5UWG36CTR50 | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | COM |
| LCMXO3L-1300E-5UWG36CTR1K | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | COM |
| LCMXO3L-1300E-5UWG36ITR | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | IND |
| LCMXO3L-1300E-5UWG36ITR50 | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | IND |
| LCMXO3L-1300E-5UWG36ITR1K | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | IND |
| LCMXO3L-1300E-5MG121C | 1300 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3L-1300E-6MG121C | 1300 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3L-1300E-5MG121I | 1300 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3L-1300E-6MG121I | 1300 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3L-1300E-5MG256C | 1300 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3L-1300E-6MG256C | 1300 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3L-1300E-5MG256I | 1300 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3L-1300E-6MG256I | 1300 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3L-1300C-5BG256C | 1300 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 256 | COM |
| LCMXO3L-1300C-6BG256C | 1300 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 256 | COM |
| LCMXO3L-1300C-5BG256I | 1300 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 256 | IND |
| LCMXO3L-1300C-6BG256I | 1300 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | Speed | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO3L-2100E-5UWG49CTR | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | COM |
| LCMXO3L-2100E-5UWG49CTR50 | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | COM |
| LCMXO3L-2100E-5UWG49CTR1K | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | COM |
| LCMXO3L-2100E-5UWG49ITR | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | IND |
| LCMXO3L-2100E-5UWG49ITR50 | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | IND |
| LCMXO3L-2100E-5UWG49ITR1K | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | IND |
| LCMXO3L-2100E-5MG121C | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3L-2100E-6MG121C | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3L-2100E-5MG121I | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3L-2100E-6MG121I | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3L-2100E-5MG256C | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3L-2100E-6MG256C | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3L-2100E-5MG256I | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3L-2100E-6MG256I | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3L-2100E-5MG324C | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 324 | COM |
| LCMXO3L-2100E-6MG324C | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 324 | COM |
| LCMXO3L-2100E-5MG324I | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 324 | IND |

## MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Speed | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO3LF-640E-5MG121C | 640 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3LF-640E-6MG121C | 640 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3LF-640E-5MG121I | 640 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3LF-640E-6MG121I | 640 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | IND |

| Part Number | LUTs | Supply Voltage | Speed | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO3LF-1300E-5UWG36CTR | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | COM |
| LCMXO3LF-1300E-5UWG36CTR50 | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | COM |
| LCMXO3LF-1300E-5UWG36CTR1K | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | COM |
| LCMXO3LF-1300E-5UWG36ITR | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | IND |
| LCMXO3LF-1300E-5UWG36ITR50 | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | IND |
| LCMXO3LF-1300E-5UWG36ITR1K | 1300 | 1.2 V | 5 | Halogen-Free WLCSP | 36 | IND |
| LCMXO3LF-1300E-5MG121C | 1300 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3LF-1300E-6MG121C | 1300 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3LF-1300E-5MG121I | 1300 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3LF-1300E-6MG121I | 1300 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3LF-1300E-5MG256C | 1300 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3LF-1300E-6MG256C | 1300 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3LF-1300E-5MG256I | 1300 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3LF-1300E-6MG256I | 1300 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3LF-1300C-5BG256C | 1300 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 256 | COM |
| LCMXO3LF-1300C-6BG256C | 1300 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 256 | COM |
| LCMXO3LF-1300C-5BG256I | 1300 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 256 | IND |
| LCMXO3LF-1300C-6BG256I | 1300 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 256 | IND |

| Part Number | LUTs | Supply Voltage | Speed | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO3LF-2100E-5UWG49CTR | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | COM |
| LCMXO3LF-2100E-5UWG49CTR50 | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | COM |
| LCMXO3LF-2100E-5UWG49CTR1K | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | COM |
| LCMXO3LF-2100E-5UWG49ITR | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | IND |
| LCMXO3LF-2100E-5UWG49ITR50 | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | IND |
| LCMXO3LF-2100E-5UWG49ITR1K | 2100 | 1.2 V | 5 | Halogen-Free WLCSP | 49 | IND |
| LCMXO3LF-2100E-5MG121C | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3LF-2100E-6MG121C | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | COM |
| LCMXO3LF-2100E-5MG121I | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3LF-2100E-6MG121I | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 121 | IND |
| LCMXO3LF-2100E-5MG256C | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3LF-2100E-6MG256C | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3LF-2100E-5MG256I | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3LF-2100E-6MG256I | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3LF-2100E-5MG324C | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 324 | COM |
| LCMXO3LF-2100E-6MG324C | 2100 | 1.2 V | 6 | Halogen-Free csfBGA | 324 | COM |
| LCMXO3LF-2100E-5MG324I | 2100 | 1.2 V | 5 | Halogen-Free csfBGA | 324 | IND |

| Part Number | LUTs | Supply Voltage | Speed | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO3LF-6900E-5MG256C | 6900 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3LF-6900E-6MG256C | 6900 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3LF-6900E-5MG256I | 6900 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3LF-6900E-6MG256I | 6900 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3LF-6900E-5MG324C | 6900 | 1.2 V | 5 | Halogen-Free csfBGA | 324 | COM |
| LCMXO3LF-6900E-6MG324C | 6900 | 1.2 V | 6 | Halogen-Free csfBGA | 324 | COM |
| LCMXO3LF-6900E-5MG324I | 6900 | 1.2 V | 5 | Halogen-Free csfBGA | 324 | IND |
| LCMXO3LF-6900E-6MG324I | 6900 | 1.2 V | 6 | Halogen-Free csfBGA | 324 | IND |
| LCMXO3LF-6900C-5BG256C | 6900 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 256 | COM |
| LCMXO3LF-6900C-6BG256C | 6900 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 256 | COM |
| LCMXO3LF-6900C-5BG256I | 6900 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 256 | IND |
| LCMXO3LF-6900C-6BG256I | 6900 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 256 | IND |
| LCMXO3LF-6900C-5BG324C | 6900 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 324 | COM |
| LCMXO3LF-6900C-6BG324C | 6900 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 324 | COM |
| LCMXO3LF-6900C-5BG324I | 6900 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 324 | IND |
| LCMXO3LF-6900C-6BG324I | 6900 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 324 | IND |
| LCMXO3LF-6900C-5BG400C | 6900 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 400 | COM |
| LCMXO3LF-6900C-6BG400C | 6900 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 400 | COM |
| LCMXO3LF-6900C-5BG400I | 6900 | 2.5 V / 3.3 V | 5 | Halogen-Free caBGA | 400 | IND |
| LCMXO3LF-6900C-6BG400I | 6900 | 2.5 V / 3.3 V | 6 | Halogen-Free caBGA | 400 | IND |

| Part Number | LUTs | Supply Voltage | Speed | Package | Leads | Temp. |
|---|---|---|---|---|---|---|
| LCMXO3LF-9400E-5MG256C | 9400 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3LF-9400E-6MG256C | 9400 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | COM |
| LCMXO3LF-9400E-5MG256I | 9400 | 1.2 V | 5 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3LF-9400E-6MG256I | 9400 | 1.2 V | 6 | Halogen-Free csfBGA | 256 | IND |
| LCMXO3LF-9400C-5BG256C | 9400 | 2.5 V/3.3 V | 5 | Halogen-Free caBGA | 256 | COM |
| LCMXO3LF-9400C-6BG256C | 9400 | 2.5 V/3.3 V | 6 | Halogen-Free caBGA | 256 | COM |
| LCMXO3LF-9400C-5BG256I | 9400 | 2.5 V/3.3 V | 5 | Halogen-Free caBGA | 256 | IND |
| LCMXO3LF-9400C-6BG256I | 9400 | 2.5 V/3.3 V | 6 | Halogen-Free caBGA | 256 | IND |
| LCMXO3LF-9400C-5BG400C | 9400 | 2.5 V/3.3 V | 5 | Halogen-Free caBGA | 400 | COM |
| LCMXO3LF-9400C-6BG400C | 9400 | 2.5 V/3.3 V | 6 | Halogen-Free caBGA | 400 | COM |
| LCMXO3LF-9400C-5BG400I | 9400 | 2.5 V/3.3 V | 5 | Halogen-Free caBGA | 400 | IND |
| LCMXO3LF-9400C-6BG400I | 9400 | 2.5 V/3.3 V | 6 | Halogen-Free caBGA | 400 | IND |
| LCMXO3LF-9400C-5BG484C | 9400 | 2.5 V/3.3 V | 5 | Halogen-Free caBGA | 484 | COM |
| LCMXO3LF-9400C-6BG484C | 9400 | 2.5 V/3.3 V | 6 | Halogen-Free caBGA | 484 | COM |
| LCMXO3LF-9400C-5BG484I | 9400 | 2.5 V/3.3 V | 5 | Halogen-Free caBGA | 484 | IND |
| LCMXO3LF-9400C-6BG484I | 9400 | 2.5 V/3.3 V | 6 | Halogen-Free caBGA | 484 | IND |