E · / Fattice Semiconductor Corporation - <u>LCMXO3L-9400E-6BG400I Datasheet</u>



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1175
Number of Logic Elements/Cells	9400
Total RAM Bits	442368
Number of I/O	335
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3l-9400e-6bg400i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Table 1-1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900	9400
Distributed R/	AM (kbits)	5	10	16	34	54	73
EBR SRAM (I	kbits)	64	64	74	92	240	432
Number of PLLs		1	1	1	2	2	2
Hardened	l ² C	2	2	2	2	2	2
Functions:	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY S	Support	Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Pr NVCM	ogrammable	MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400
Packages				ΙΟ			
36-ball WLCS (2.5 mm x 2.5	6P ¹ 6 mm, 0.4 mm)		28				
49-ball WLCS (3.2 mm x 3.2	P ¹ mm, 0.4 mm)			38			
81-ball WLCS (3.8 mm x 3.8	P ¹ mm, 0.4 mm)				63		
121-ball csfB0 (6 mm x 6 mm	GA ¹ n, 0.5 mm)	100	100	100	100		
256-ball csfB (9 mm x 9 mn	GA ¹ n, 0.5 mm)		206	206	206	206	206
324-ball csfB (10 mm x 10	GA ¹ mm, 0.5 mm)		2	268	268	281	
256-ball caBC (14 mm x 14 i	àA² mm, 0.8 mm)		206	206	206	206	206
324-ball caBC (15 mm x 15 i	àA² mm, 0.8 mm)			279	279	279	
400-ball caB0 (17 mm x 17 i	àA² mm, 0.8 mm)				335	335	335
484-ball caBC (19 mm x 19	3A² mm, 0.8 mm)						384

1. Package is only available for E=1.2 V devices.

2. Package is only available for C=2.5 V/3.3 V devices.

Introduction

MachXO3[™] device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I²C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs



Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO3L/LF devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO3L/LF devices, please see TN1290, Memory Usage Guide for MachXO3 Devices.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16x4	PDPR 16x4			
Number of slices	3	3			
Note: SPR = Single Port RAM_PDPR = Pseudo Dual Port RAM					

ote: SPR = Single Port RAM, PDPR = Pseudo Dual



ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

Routing

There are many resources provided in the MachXO3L/LF devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO3L/LF device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO3L/LF architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO3L/LF devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3L/LF devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3L/LF External Switching Characteristics table.

Primary clock signals for the MachXO3L/LF-1300 and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sys-CLOCK PLL outputs.



Figure 2-6. Secondary High Fanout Nets for MachXO3L/LF Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO3L/LF devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO3L/LF sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO3L/LF clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.



Figure 2-8. sysMEM Memory Primitives





Figure 2-11. Group of Four Programmable I/O Cells





Figure 2-18. PC Core Block Diagram



Table 2-14 describes the signals interfacing with the I²C cores.

 Table 2-14. PC Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I ² C core. The signal is an output if the I ² C core is in master mode. The signal is an input if the I ² C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO3L/LF device.
i2c_sda	Bi-directional	Bi-directional data line of the l^2C core. The signal is an output when data is transmitted from the l^2C core. The signal is an input when data is received into the l^2C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of l^2C ports in each MachXO3L/LF device.
i2c_irqo	Output	Interrupt request output signal of the I ² C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I ² C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.

Hardened SPI IP Core

Every MachXO3L/LF device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO3L/LF devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface



There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology (Appendix B)
- TN1293, Using Hardened Control Functions in MachXO3 Devices

Figure 2-19. SPI Core Block Diagram



Table 2-15 describes the signals interfacing with the SPI cores.

Table 2-15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	0	Master	SPI master chip-select output
spi_csn[17]	0	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	0	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Con- figuration Logic.
cfg_stdby	0	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.
cfg_wake	0	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, SPI Tab.



For more details on these embedded functions, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

User Flash Memory (UFM)

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

Standby Mode and Power Saving Options

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the E devices operate at 1.2 V V_{CC}.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I²C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned "off" or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.



Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I²C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

- 1. Internal NVCM/Flash Download
- 2. JTAG
- 3. Standard Serial Peripheral Interface (Master SPI mode) interface to boot PROM memory
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Standard I²C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, MachXO3 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/ LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.



Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

- 1. Unlocked Readback of the SRAM configuration and NVCM/Flash spaces is allowed.
- 2. Permanently Locked The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

Password

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to TN1313, Using Password Security with MachXO3 Devices.

Dual Boot

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1292, MachXO3 Soft Error Detection Usage Guide.

Soft Error Correction

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to TN1292, MachXO3 Soft Error Detection (SED)/Correction (SEC) Usage Guide.



MachXO3 Family Data Sheet DC and Switching Characteristics

February 2017

Advance Data Sheet DS1047

Absolute Maximum Ratings^{1, 2, 3}

	MachXO3L/LF E (1.2 V)	MachXO3L/LF C (2.5 V/3.3 V)
Supply Voltage V _{CC}	\ldots .–0.5 V to 1.32 V \ldots .	–0.5 V to 3.75 V
Output Supply Voltage V _{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied ^{4, 5}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied ⁴	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T ₁)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

4. Overshoot and undershoot of -2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

5. The dual function I^2C pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Units
V _{CC} ¹	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V _{CCIO} ^{1, 2, 3}	I/O Driver Supply Voltage	1.14	3.465	V
t _{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t _{JIND}	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.

2. See recommended voltages by I/O standard in subsequent table.

3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates¹

	iyp.	wax.	Units
t _{RAMP} Power supply ramp rates for all power supplies. 0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

^{© 2017} Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example



Table 3-2. BLVDS DC Conditions¹

Over Recommended	Operating	Conditions
	operating	oonantions

		Noi		
Symbol	Description	Zo = 45	Zo = 90	Units
Z _{OUT}	Output impedance	20	20	Ohms
R _S	Driver series resistance	80	80	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.376	1.480	V
V _{OL}	Output low voltage	1.124	1.020	V
V _{OD}	Output differential voltage	0.253	0.459	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.



MachXO3L/LF External Switching Characteristics – C/E Devices^{1, 2, 3, 4, 5, 6, 10}

			-6 -5			$\neg \neg \neg$	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
Clocks							
Primary Clo	cks						-
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	All MachXO3L/LF devices	_	388	_	323	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO3L/LF devices	0.5		0.6		ns
		MachXO3L/LF-1300		867	_	897	ps
		MachXO3L/LF-2100		867		897	ps
t _{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO3L/LF-4300	_	865	_	892	ps
		MachXO3L/LF-6900	_	902	-	942	ps
		MachXO3L/LF-9400	_	908	-	950	ps
Edge Clock							
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	MachXO3L/LF		400	_	333	MHz
Pin-LUT-Pin	Propagation Delay						
t _{PD}	Best case propagation delay through one LUT-4	All MachXO3L/LF devices		6.72		6.96	ns
General I/O	Pin Parameters (Using Primary Clock with	out PLL)					
		MachXO3L/LF-1300	—	7.46	—	7.66	ns
		MachXO3L/LF-2100	_	7.46	_	7.66	ns
t _{CO}	Clock to Output - PIO Output Register	MachXO3L/LF-4300	_	7.51		7.71	ns
		MachXO3L/LF-6900	_	7.54		7.75	ns
		MachXO3L/LF-9400	_	7.53		7.83	ns
		MachXO3L/LF-1300	-0.20	_	-0.20		ns
		MachXO3L/LF-2100	-0.20	_	-0.20		ns
t _{SU}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-4300	-0.23	_	-0.23		ns
		MachXO3L/LF-6900	-0.23		-0.23		ns
		MachXO3L/LF-9400	-0.24		-0.24		ns
		MachXO3L/LF-1300	1.89		2.13		ns
		MachXO3L/LF-2100	1.89	_	2.13		ns
t _H	Clock to Data Hold - PIO Input Register	MachXO3L/LF-4300	1.94	_	2.18		ns
		MachXO3L/LF-6900	1.98	_	2.23		ns
		MachXO3L/LF-9400	1.99	_	2.24		ns
		MachXO3L/LF-1300	1.61	_	1.76		ns
		MachXO3L/LF-2100	1.61	_	1.76		ns
t _{SU DEL}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-4300	1.66	_	1.81		ns
	with Data input Delay	MachXO3L/LF-6900	1.53	_	1.67		ns
		MachXO3L/LF-9400	1.65	_	1.80		ns
		MachXO3L/LF-1300	-0.23	_	-0.23		ns
		MachXO3L/LF-2100	-0.23	—	-0.23	_	ns
^t H DEL	Clock to Data Hold - PIO Input Register with	MachXO3L/LF-4300	-0.25	_	-0.25	_	ns
	Input Data Delay	MachXO3L/LF-6900	-0.21	_	-0.21	_	ns
		MachXO3L/LF-9400	-0.24	_	-0.24	_	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO3L/LF devices	—	388	—	323	MHz

Over Recommended Operating Conditions



			_	6	I _	5	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
MIPI D-PHY	Inputs with Clock and Data Centered at F	Pin Using PCLK Pin for Clo	ck Input	-			<u> </u>
GDDRX4_R	K.ECLK.Centered ^{10, 11, 12}		1	1	1	1	T
t _{SU} ¹⁵	Input Data Setup Before ECLK		0.200		0.200	—	UI
t _{HO} ¹⁵	Input Data Hold After ECLK	All MachXO3L/LE	0.200	—	0.200	—	UI
f _{DATA} ¹⁴	MIPI D-PHY Input Data Speed	devices, bottom side only		900	—	900	Mbps
f _{DDRX4} ¹⁴	MIPI D-PHY ECLK Frequency		—	450	—	450	MHz
f _{SCLK} ¹⁴	SCLK Frequency		_	112.5	-	112.5	MHz
Generic DD	R Outputs with Clock and Data Aligned at	Pin Using PCLK Pin for Clo	ck Input	– GDDF	RX1_TX.	SCLK.A	ligned ⁸
t _{DIA}	Output Data Invalid After CLK Output		—	0.520	—	0.550	ns
t _{DIB}	Output Data Invalid Before CLK Output	All MachXO3L/LF		0.520	—	0.550	ns
f _{DATA}	DDRX1 Output Data Speed	all sides		300	—	250	Mbps
f _{DDRX1}	DDRX1 SCLK frequency			150	—	125	MHz
Generic DDF	Outputs with Clock and Data Centered at	Pin Using PCLK Pin for Clo	ck Input	– GDDR	X1_TX.9	SCLK.Ce	entered ⁸
t _{DVB}	Output Data Valid Before CLK Output		1.210		1.510	—	ns
t _{DVA}	Output Data Valid After CLK Output	All MachXO3L/LF	1.210		1.510	—	ns
f _{DATA}	DDRX1 Output Data Speed	devices,	_	300	—	250	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)	- all sides	_	150	_	125	MHz
Generic DDF	X2 Outputs with Clock and Data Aligned a	at Pin Using PCLK Pin for Clo	ock Inpu	t – GDD	RX2_TX	ECLK.A	
t _{DIA}	Output Data Invalid After CLK Output		<u> </u>	0.200	—	0.215	ns
t _{DIB}	Output Data Invalid Before CLK Output	_		0.200	_	0.215	ns
f _{DATA}	DDRX2 Serial Output Data Speed	MachXO3L/LF devices,		664	_	554	Mbps
foogy2	DDRX2 ECLK frequency	top side only		332	_	277	MHz
fsci k	SCLK Frequency			166	_	139	MHz
Generic DD	RX2 Outputs with Clock and Data Center	ed at Pin Using PCLK Pin fo	or Clock	Input –			
GDDRX2_T	(.ECLK.Centered ^{8, 9}	0		•			
t _{DVB}	Output Data Valid Before CLK Output		0.535	—	0.670	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	ns
f _{DATA}	DDRX2 Serial Output Data Speed	MachXO3L/LF devices,		664	—	554	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)	top side only	_	332	—	277	MHz
f _{SCLK}	SCLK Frequency			166	—	139	MHz
Generic DD GDDRX4_TX	RX4 Outputs with Clock and Data Aligned	d at Pin Using PCLK Pin for	Clock I	nput –			
t _{DIA}	Output Data Invalid After CLK Output		_	0.200	_	0.215	ns
t _{DIB}	Output Data Invalid Before CLK Output	7		0.200	_	0.215	ns
f _{DATA}	DDRX4 Serial Output Data Speed	MachXO3L/LF devices,	_	800	_	630	Mbps
f _{DDBX4}	DDRX4 ECLK Frequency		<u> </u>	400	_	315	MHz
fscik	SCLK Frequency		<u> </u>	100		79	MHz



NVCM/Flash Download Time^{1, 2}

Symbol	Parameter	Device	Тур.	Units
t _{REFRESH}	POR to Device I/O Active	LCMXO3L/LF-640	1.9	ms
		LCMXO3L/LF-1300	1.9	ms
		LCMXO3L/LF-1300 256-Ball Package	1.4	ms
		LCMXO3L/LF-2100	1.4	ms
		LCMXO3L/LF-2100 324-Ball Package	2.4	ms
		LCMXO3L/LF-4300	2.4	ms
		LCMXO3L/LF-4300 400-Ball Package	3.8	ms
		LCMXO3L/LF-6900	3.8	ms
		LCMXO3L/LF-9400C	5.2	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Mo	odes				
t _{PRGM}	PROGRAMN low p	PROGRAMN low pulse accept			ns
t _{PRGMJ}	PROGRAMN low p	ulse rejection	_	25	ns
t _{INITL}	INITN low time	LCMXO3L/LF-640/ LCMXO3L/LF-1300	—	55	us
		LCMXO3L/LF-1300 256-Ball Package/ LCMXO3L/LF-2100	_	70	us
		LCMXO3L/LF-2100 324-Ball Package/ LCMXO3-4300	_	105	us
		LCMXO3L/LF-4300 400-Ball Package/ LCMXO3-6900	_	130	us
		LCMXO3L/LF-9400C	_	175	us
t _{DPPINIT}	PROGRAMN low to	NITN low	_	150	ns
t _{DPPDONE}	PROGRAMN low to	DONE low	_	150	ns
t _{IODISS}	PROGRAMN low to	o I/O disable	_	120	ns
Slave SPI					
f _{MAX}	CCLK clock frequer	псу		66	MHz
t _{CCLKH}	CCLK clock pulse v	CCLK clock pulse width high			ns
t _{CCLKL}	CCLK clock pulse v	vidth low	7.5	—	ns
t _{STSU}	CCLK setup time		2	_	ns
t _{STH}	CCLK hold time		0	_	ns
t _{STCO}	CCLK falling edge t	o valid output	—	10	ns
t _{STOZ}	CCLK falling edge t	o valid disable	—	10	ns
t _{STOV}	CCLK falling edge t	o valid enable	—	10	ns
t _{SCS}	Chip select high tim	ne	25	—	ns
t _{SCSS}	Chip select setup ti	me	3	—	ns
t _{SCSH}	Chip select hold tim	ne	3	—	ns
Master SPI					
f _{MAX}	MCLK clock freque	ncy	_	133	MHz
t _{MCLKH}	MCLK clock pulse v	MCLK clock pulse width high		_	ns
t _{MCLKL}	MCLK clock pulse v	width low	3.75	—	ns
t _{STSU}	MCLK setup time		5	—	ns
t _{STH}	MCLK hold time		1	—	ns
t _{CSSPI}	INITN high to chip s	select low	100	200	ns
t _{MCLK}	INITN high to first M	ICLK edge	0.75	1	US



Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions				
Configuration (Dual function pins used during sysCONFIG)						
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.				
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.				
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.				
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.				
SN	I	Slave SPI active low chip select input.				
CSSPIN	I/O	Master SPI active low chip select output.				
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.				
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.				
SCL	I/O	Slave I ² C clock input and master I ² C clock output.				
SDA	I/O	Slave I ² C data input and master I ² C data output.				



	MachXO3L/LF-4300						
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank							
Bank 0	29	24	50	71	50	71	83
Bank 1	0	26	52	62	52	68	84
Bank 2	20	26	52	72	52	72	84
Bank 3	7	7	16	22	16	24	28
Bank 4	0	7	16	14	16	16	24
Bank 5	7	10	20	27	20	28	32
Total General Purpose Single Ended IO	63	100	206	268	206	279	335
Differential IO per Bank							
Bank 0	15	12	25	36	25	36	42
Bank 1	0	13	26	30	26	34	42
Bank 2	10	13	26	36	26	36	42
Bank 3	3	3	8	10	8	12	14
Bank 4	0	3	8	6	8	8	12
Bank 5	3	5	10	13	10	14	16
Total General Purpose Differential IO	31	49	103	131	103	140	168
Dual Function IO	25	37	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21
High-speed Differential Outputs							
Bank 0	10	7	18	18	18	18	21
VCCIO Pins							
Bank 0	3	1	4	4	4	4	5
Bank 1	0	1	3	4	4	4	5
Bank 2	2	1	4	4	4	4	5
Bank 3	1	1	2	2	1	2	2
Bank 4	0	1	2	2	2	2	2
Bank 5	1	1	2	2	1	2	2
VCC	4	4	8	8	8	10	10
GND	6	10	24	16	24	16	33
NC	0	0	0	13	1	0	0
Reserved for Configuration	1	1	1	1	1	1	1
Total Count of Bonded Pins	81	121	256	324	256	324	400



MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-640E-5MG121I	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3L-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3L-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-1300E-5MG1211	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-1300E-6MG1211	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-1300C-5BG256C	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-6BG256C	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-1300C-5BG256I	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-1300C-6BG256I	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3L-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3L-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-2100E-6MG1211	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND