E.) Crattice Semiconductor Corporation - <u>LCMXO3LF-1300E-5MG121I Datasheet</u>



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	100
Number of Gates	·
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	121-VFBGA, CSPBGA
Supplier Device Package	121-CSFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-1300e-5mg121i

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MachXO3 Family Data Sheet Architecture

February 2017

Advance Data Sheet DS1047

Architecture Overview

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK[™] PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.





Notes:

MachXO3L/LF-640 is similar to MachXO3L/LF-1300. MachXO3L/LF-640 has a lower LUT count.

MachXO3L devices have NVCM, MachXO3LF devices have Flash.

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 Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the NVCM or Configuration Flash.

MachXO3LF EBR initialization data can also be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO3LF devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2-8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.



Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE ¹	Output Clock Enable	Active High
RST	Reset	Active High
BE ¹	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	
DI	Data In	_
DO	Data Out	_
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	_
FF	FIFO RAM Full Flag	_
AEF	FIFO RAM Almost Empty Flag	_
EF	FIFO RAM Empty Flag	_
RPRST	FIFO RAM Read Pointer Reset	_

Table 2-6. EBR Signal Descriptions

1. Optional signals.

2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.

3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.

4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).

In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port clock, CSR is the read port clock.

The EBR memory supports three forms of write behavior for single or dual port operation:

- 1. **Normal** Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- 2. Write Through A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
- 3. Read-Before-Write When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2 ^N -1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset



Figure 2-11. Group of Four Programmable I/O Cells





sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, PCI, LVDS, BLVDS, MLVDS and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO3L/LF devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS and PCI), differential (LVDS) input buffers are powered using I/O supply voltage (V_{CCIO}). Each sysIO bank has its own V_{CCIO} .

MachXO3L/LF devices contain three types of sysIO buffer pairs.

1. Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential input buffers.

2. Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential input buffers. Only the I/Os on the bottom banks have programmable PCI clamps and differential input termination. The PCI clamp is enabled after V_{CC} and V_{CCIO} are at valid operating levels and the device has been configured.

3. Top sysIO Buffer Pairs

The sysIO buffer pairs in the top bank of the device consist of two single-ended output drivers and two singleended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential I/O buffers. Half of the sysIO buffer pairs on the top edge have true differential outputs. The sysIO buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached V_{PORUP} level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pulldown to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins will maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached V_{PORUP} levels at which time the I/Os will take on the user-configured settings only after a proper download/configuration.

There are various ways a user can ensure that there are no spurious signals on critical outputs as the device powers up. These are discussed in more detail in TN1280, MachXO3 sysIO Usage Guide.

Supported Standards

The MachXO3L/LF sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL, and PCI. The buffer supports the LVTTL, PCI, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO3L/LF devices support on-chip LVDS output buffers on approximately 50% of the I/Os on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO3L/LF devices. PCI support is provided in the bottom bank of the MachXO3L/LF devices. Table 2-11 summarizes the I/O characteristics of the MachXO3L/LF PLDs.



Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, Boundary Scan Testability with Lattice sysIO Capability and TN1087, Minimizing System Interruption During Configuration Using TransFR Technology.

Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I²C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

- 1. Internal NVCM/Flash Download
- 2. JTAG
- 3. Standard Serial Peripheral Interface (Master SPI mode) interface to boot PROM memory
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Standard I²C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, MachXO3 Programming and Configuration Usage Guide for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/ LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.



MachXO3 Family Data Sheet DC and Switching Characteristics

February 2017

Advance Data Sheet DS1047

Absolute Maximum Ratings^{1, 2, 3}

	MachXO3L/LF E (1.2 V)	MachXO3L/LF C (2.5 V/3.3 V)
Supply Voltage V _{CC}	\ldots .–0.5 V to 1.32 V \ldots .	–0.5 V to 3.75 V
Output Supply Voltage V _{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied ^{4, 5}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied ⁴	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T ₁)	–40 °C to 125 °C	–40 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

2. Compliance with the Lattice Thermal Management document is required.

3. All voltages referenced to GND.

4. Overshoot and undershoot of -2 V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

5. The dual function I^2C pins SCL and SDA are limited to -0.25 V to 3.75 V or to -0.3 V with a duration of <20 ns.

Recommended Operating Conditions¹

Symbol	Parameter		Max.	Units
Vaa ¹	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
VCC	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V _{CCIO} ^{1, 2, 3}	V _{CCIO} ^{1, 2, 3} I/O Driver Supply Voltage		3.465	V
t _{JCOM} Junction Temperature Commercial Operation		0	85	°C
t _{JIND}	Junction Temperature Industrial Operation	-40	100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.

2. See recommended voltages by I/O standard in subsequent table.

3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

Power Supply Ramp Rates¹

	iyp.	wax.	Units
t _{RAMP} Power supply ramp rates for all power supplies. 0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

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sysIO Single-Ended DC Electrical Characteristics^{1, 2}

Input/Output	V	'IL	v	н	Voi Max.	Vou Min.	lo, Max,⁴	ו _{סם} Max.⁴	
Standard	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)	(V)	(V)	(mA)	(mA)	
				0.4				4	-4
					0.4	V 0.4	8	-8	
	-0.3	0.8	2.0	3.6	0.4	VCCIO - 0.4	12	-12	
							16	-16	
					0.2	V _{CCIO} - 0.2	0.1	-0.1	
							4	-4	
					0.4	V 0.4	8	-8	
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	VCCIO - 0.4	12	-12	
							16	-16	
					0.2	V _{CCIO} - 0.2	0.1	-0.1	
	–0.3 0.35V _{CCIO}						4	-4	
		0.251/	0.651/	26	0.4	V _{CCIO} - 0.4	8	-8	
LVCIMOS 1.8		-0.3	0.35VCCIO	0.05V _{CCIO}	0100 V COLO	3.0			12
					0.2	V _{CCIO} - 0.2	0.1	-0.1	
LVCMOS 1.5	-0.3		0.65V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4 V _{CCIO} - 0.2	4	-4	
		0.35V _{CCIO}					8	-8	
					0.2		0.1	-0.1	
			0.65V _{CCIO} 3.6		3.6 0.4	0.4	V 0.4	4	-2
LVCMOS 1.2	-0.3	0.35V _{CCIO}		3.6		VCCIO - 0.4	8	-6	
					0.2	V _{CCIO} - 0.2	0.1	-0.1	
LVCMOS25R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA	
LVCMOS18R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA	
LVCMOS18R25	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA	
LVCMOS15R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA	
LVCMOS15R25	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA	
LVCMOS12R33	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain	
LVCMOS12R25	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain	
LVCMOS10R33	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain	
LVCMOS10R25	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain	

 MachXO3L/LF devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO3L/LF devices do not meet the relevant JEDEC specification are documented in the table below.

2. MachXO3L/LF devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1280, MachXO3 sysIO Usage Guide.

3. The dual function I²C pins SCL and SDA are limited to a V_{IL} min of -0.25 V or to -0.3 V with a duration of <10 ns.

4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. "n" is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.



sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V V	Input Voltage	V _{CCIO} = 3.3 V	0	_	2.605	V
VINP VINM		V _{CCIO} = 2.5 V	0	_	2.05	V
V _{THD}	Differential Input Threshold		±100	_		mV
V	Input Common Mode Voltage	V _{CCIO} = 3.3 V	0.05	_	2.6	V
V ^{CM}	input Common Mode Voltage	V _{CCIO} = 2.5 V	0.05	_	2.0	V
I _{IN}	Input current	Power on	_	_	±10	μA
V _{OH}	Output high voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.375	_	V
V _{OL}	Output low voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.90	1.025	_	V
V _{OD}	Output voltage differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} between high and low		_	_	50	mV
V _{OS}	Output voltage offset	(V _{OP} - V _{OM})/2, R _T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V _{OS} between H and L		—	—	50	mV
IOSD	Output short circuit current	V _{OD} = 0 V driver outputs shorted	_	_	24	mA

Over Recommended Operating Conditions



LVPECL

The MachXO3L/LF family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL



Table 3-3. LVPECL DC Conditions¹

Symbol	Description	Nominal	Units
Z _{OUT}	Output impedance	20	Ohms
R _S	Driver series resistor	93	Ohms
R _P	Driver parallel resistor	196	Ohms
R _T	Receiver termination	100	Ohms
V _{OH}	Output high voltage	2.05	V
V _{OL}	Output low voltage	1.25	V
V _{OD}	Output differential voltage	0.80	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	100.5	Ohms
I _{DC}	DC output current	12.11	mA

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.



MIPI D-PHY Emulation

MachXO3L/LF devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed IOs use the LVDS25E buffer and Low Power IOs use the LVCMOS buffers. The scheme shown in Figure 3-4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3-5 is one possible solution for MIPI D-PHY Transmitter implementation.

Figure 3-4. MIPI D-PHY Input Using External Resistors



Table 3-4. MIPI DC Conditions¹

	Description	Min.	Тур.	Max.	Units		
Receiver							
External Terminatio	n						
RT	1% external resistor with VCCIO=2.5 V		50	—	Ohms		
	1% external resistor with VCCIO=3.3 V	—	50	—	Ohms		
High Speed							
VCCIO	VCCIO of the Bank with LVDS Emulated input buffer	—	2.5	—	V		
	VCCIO of the Bank with LVDS Emulated input buffer	—	3.3	—	V		
VCMRX	Common-mode voltage HS receive mode	150	200	250	mV		
VIDTH	Differential input high threshold		—	100	mV		
VIDTL	Differential input low threshold		—	—	mV		
VIHHS	Single-ended input high voltage		—	300	mV		
VILHS	Single-ended input low voltage	100	—	—	mV		
ZID	Differential input impedance	80	100	120	Ohms		



Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
MIPI	450	MHz
LVDS25	400	MHz
LVDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz



		-6 -5					
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
Generic DDF GDDRX1_RX	RX1 Inputs with Clock and Data Aligned at K.SCLK.Aligned ^{8,9}	Pin Using PCLK Pin for Clo	ock Inpu	t –		1	
t _{DVA}	Input Data Valid After CLK			0.317	—	0.344	UI
t _{DVE}	Input Data Hold After CLK	All MachXO3L/LF	0.742		0.702		UI
f _{DATA}	DDRX1 Input Data Speed	-devices, all sides		300	—	250	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency			150	—	125	MHz
Generic DD GDDRX1_R	RX1 Inputs with Clock and Data Centered X.SCLK.Centered ^{8, 9}	at Pin Using PCLK Pin fo	or Clock	Input –		1	1
t _{SU}	Input Data Setup Before CLK		0.566		0.560		ns
t _{HO}	Input Data Hold After CLK	All MachXO3L/LF	0.778		0.879		ns
f _{DATA}	DDRX1 Input Data Speed	-devices, all sides		300	—		Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		_	150	—	125	MHz
Generic DD GDDRX2_R	RX2 Inputs with Clock and Data Aligned at X.ECLK.Aligned ^{8, 9}	Pin Using PCLK Pin for C	lock Inp	out –	I	I	I
t _{DVA}	Input Data Valid After CLK		—	0.316	—	0.342	UI
t _{DVE}	Input Data Hold After CLK	-	0.710		0.675		UI
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO3L/LF devices,		664	—	554	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only		332	—	277	MHz
f _{SCLK}	SCLK Frequency			166	—	139	MHz
Generic DD GDDRX2_R	RX2 Inputs with Clock and Data Centered X.ECLK.Centered ^{8,9}	at Pin Using PCLK Pin for	Clock I	nput –			1
t _{SU}	Input Data Setup Before CLK		0.233		0.219		ns
t _{HO}	Input Data Hold After CLK	-	0.287	—	0.287		ns
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO3L/LF devices,		664	—	554	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only		332	—	277	MHz
f _{SCLK}	SCLK Frequency	-		166	—	139	MHz
Generic DDI	R4 Inputs with Clock and Data Aligned at P	in Using PCLK Pin for Cloo	k Input	- GDDR	X4_RX.	ECLK.A	ligned ⁸
t _{DVA}	Input Data Valid After ECLK			0.307	_	0.320	UI
t _{DVE}	Input Data Hold After ECLK	-	0.782	—	0.699		UI
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO3L/LF devices,		800	—	630	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only		400	—	315	MHz
f _{SCLK}	SCLK Frequency			100	—	79	MHz
Generic DDF	A4 Inputs with Clock and Data Centered at P	in Using PCLK Pin for Cloc	k Input	GDDR	X4_RX.E	CLK.Ce	entered ⁸
t _{SU}	Input Data Setup Before ECLK		0.233	—	0.219	—	ns
t _{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	ns
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO3L/LF devices,		800	—	630	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only		400	—	315	MHz
f _{SCLK}	SCLK Frequency			100	—	79	MHz
7:1 LVDS In	outs (GDDR71_RX.ECLK.7:1) ⁹			1	I	1	
t _{DVA}	Input Data Valid After ECLK		—	0.290	—	0.320	UI
t _{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	UI
f _{DATA}	DDR71 Serial Input Data Speed	MachXO3L/LF devices,	—	756	—	630	Mbps
f _{DDR71}	DDR71 ECLK Frequency	bottom side only	—	378	—	315	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (mini- mum limited by PLL)		_	108	—	90	MHz



DC and Switching Characteristics MachXO3 Family Data Sheet

		-6		-5		
Description	Device	Min.	Max.	Min.	Max.	Units
RX4 Outputs with Clock and Data Centere (.ECLK.Centered ^{8, 9}	d at Pin Using PCLK Pin fo	or Clock	Input –			
Output Data Valid Before CLK Output		0.455		0.570		ns
Output Data Valid After CLK Output		0.455	—	0.570	_	ns
DDRX4 Serial Output Data Speed	MachXO3L/LF devices,	—	800	—	630	Mbps
DDRX4 ECLK Frequency (minimum limited by PLL)	top side only	_	400	_	315	MHz
SCLK Frequency	-		100		79	MHz
Itputs – GDDR71_TX.ECLK.7:1 ^{8, 9}						
Output Data Invalid Before CLK Output			0.160	_	0.180	ns
Output Data Invalid After CLK Output			0.160		0.180	ns
DDR71 Serial Output Data Speed	MachXO3L/LF devices,		756		630	Mbps
DDR71 ECLK Frequency	top side only	_	378	—	315	MHz
7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL)		_	108	_	90	MHz
Outputs with Clock and Data Centered at P (.ECLK.Centered ^{10, 11, 12}	in Using PCLK Pin for Clo	ck Input	-			
Output Data Valid Before CLK Output		0.200	—	0.200	_	UI
Output Data Valid After CLK Output		0.200	—	0.200	_	UI
MIPI D-PHY Output Data Speed	All MachXO3L/LF	_	900	_	900	Mbps
MIPI D-PHY ECLK Frequency (minimum limited by PLL)	devices, top side only	_	450	_	450	MHz
SCLK Frequency	<u> </u>	—	112.5	—	112.5	MHz
	Description RX4 Outputs with Clock and Data Centered CECLK.Centered ^{8, 9} Output Data Valid Before CLK Output Output Data Valid After CLK Output DDRX4 Serial Output Data Speed DDRX4 ECLK Frequency (minimum limited by PLL) SCLK Frequency ttputs – GDDR71_TX.ECLK.7:1 ^{8, 9} Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed DDR71 ECLK Frequency 7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL) Outputs with Clock and Data Centered at P C.ECLK.Centered ^{10, 11, 12} Output Data Valid Before CLK Output Output Data Valid After CLK Output MIPI D-PHY Output Data Speed MIPI D-PHY ECLK Frequency (minimum limited by PLL) SCLK Frequency	DescriptionDeviceRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for C.ECLK.Centered ^{8, 9} In Using PCLK Pin for C.ECLK.Centered ^{8, 9} Output Data Valid Before CLK OutputMachXO3L/LF devices, top side onlyDDRX4 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side onlySCLK FrequencyOutput Data Invalid Before CLK OutputOutput Data Invalid After CLK OutputMachXO3L/LF devices, top side onlyOutput Data Invalid After CLK OutputMachXO3L/LF devices, top side onlyDDR71 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDDR71 ECLK Frequency 7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL)MachXO3L/LF devices, top side onlyOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputAll MachXO3L/LF devices, top side onlyOutput Data Valid After CLK OutputAll MachXO3L/LF devices, top side onlyMIPI D-PHY Output Data SpeedAll MachXO3L/LF devices, top side onlyMIPI D-PHY ECLK Frequency (minimum limited by PLL)All MachXO3L/LF devices, top side onlySCLK FrequencyAll MachXO3L/LF devices, top side only	Description Device Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock (LECLK.Centered ^{8,9}) 0.455 Output Data Valid Before CLK Output 0.455 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only SCLK Frequency Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed MachXO3L/LF devices, top side only DDR71 ECLK Frequency Output Clock Frequency (SCLK) (minimum limited by PLL) Output Data Valid After CLK Output Output Data Valid Before CLK Output Output Data Valid After CLK Output 0.200 0.200 0.200 Output Data Valid After CLK Out	-6Min.Max.RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - CLECLK.Centered ^{8, 9} Output Data Valid Before CLK Output0.455Output Data Valid After CLK OutputMachXO3L/LF devices, top side only0.455DDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side only800SCLK Frequency (minimum limited by PLL)100400Output Data Invalid Before CLK Output0.160Output Data Invalid After CLK Output0.160DDR71 Serial Output Data Speed DDR71 Serial Output Data SpeedMachXO3L/LF devices, top side only108Output Swith Clock and Data Centered at Pin Using PCLK Pin for Clock Input - t.ECLK.Centered ^{10, 11, 12} 0.200Output Data Valid Before CLK Output DDR71 Serial Output Data SpeedAll MachXO3L/LF devices, top side only0.200Output Data Valid After CLK Output Mup PLL)All MachXO3L/LF devices, top side only0.200MIPI D-PHY Output Data Speed MIPI D-PHY CLK Frequency (minimum limited by PLL)All MachXO3L/LF devices, top side only450MIPI D-PHY ECLK Frequency (minimum limited by PLL)450450	Description Image: Description Image: Description Max. Min. Max. Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{8, 9} 0.455 - 0.570 Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only - 800 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 400 - SCLK Frequency - 0.160 -	Description Device Min. Max. Min. Max. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{9,9} 0.455 - 0.570 - Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 800 - 630 SCLK Frequency - 0.160 - 916 - 916 Output Data Invalid Before CLK Output MachXO3L/LF devices, top side only - 0.160 - 0.180 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 108 - 90 Output Data Valid After CLK Output MachXO3L/LF

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

5. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.

6. The t_{SU DEL} and t_{H DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).

7. This number for general purpose usage. Duty cycle tolerance is +/-10%.

8. Duty cycle is $\pm -5\%$ for system usage.

9. Performance is calculated with 0.225 UI.

10. Performance is calculated with 0.20 UI.

11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.

12. Performance for Industrial devices and -5 devices are not modeled in the Diamond design tool.

13. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

14. Above 800 Mbps is only supported with WLCSP and csfBGA packages

15. Between 800 Mbps to 900 Mbps:

a. VIDTH exceeds the MIPI D-PHY Input DC Conditions Table 3-4 and can be calculated with the equation tSU or tH = -0.0005*VIDTH + 0.3284

b. Example calculations

i. tSU and tHO = 0.28 with VIDTH = 100 mV

ii. tSU and tHO = 0.25 with VIDTH = 170 mV

iii. tSU and tHO = 0.20 with VIDTH = 270 mV



sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS)		1.5625	400	MHz
f _{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f _{VCO}	PLL VCO Frequency		200	800	MHz
f _{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteri	stics	·			
t _{DT}	Output Clock Duty Cycle	Without duty trim selected ³	45	55	%
t _{DT_TRIM} ⁷	Edge Duty Trim Accuracy		-75	75	%
t _{PH} ⁴	Output Phase Accuracy		-6	6	%
	Output Cleak Pariad littar	f _{OUT} > 100 MHz	—	150	ps p-p
		f _{OUT} < 100 MHz	—	0.007	UIPP
topjit ^{1, 8}		f _{OUT} > 100 MHz	—	180	ps p-p
		f _{OUT} < 100 MHz	—	0.009	UIPP
	Output Clock Phase litter	f _{PFD} > 100 MHz	—	160	ps p-p
	Output Clock Phase Jitter	f _{PFD} < 100 MHz	—	0.011	UIPP
	Output Clask Davied Litter (Eventional N)	f _{OUT} > 100 MHz	—	230	ps p-p
		f _{OUT} < 100 MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter	f _{OUT} > 100 MHz	—	230	ps p-p
(Fractional-N)		f _{OUT} < 100 MHz	—	0.12	UIPP
t _{SPO}	Static Phase Offset	Divider ratio = integer	-120	120	ps
t _W	Output Clock Pulse Width	At 90% or 10% ³	0.9	—	ns
tLOCK ^{2, 5}	PLL Lock-in Time		—	15	ms
t _{UNLOCK}	PLL Unlock Time		—	50	ns
• 6	Innut Cleak Davied Litter	f _{PFD} ≥ 20 MHz	—	1,000	ps p-p
'IPJIT		f _{PFD} < 20 MHz	—	0.02	UIPP
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t _{STABLE} ⁵	STANDBY High to PLL Stable		—	15	ms
t _{RST}	RST/RESETM Pulse Width		1	_	ns
t _{RSTREC}	RST Recovery Time		1		ns
t _{RST DIV}	RESETC/D Pulse Width		10		ns
t _{RSTREC} DIV	RESETC/D Recovery Time		1		ns
t _{ROTATE-SETUP}	PHASESTEP Setup Time		10		ns
t _{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

Over Recommended Operating Conditions

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide for more details.

5. At minimum $\rm f_{PFD}$ As the $\rm f_{PFD}$ increases the time will decrease to approximately 60% the value listed.

6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.

7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.

8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.



I²C Port Timing Specifications^{1, 2}

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCL clock frequency		400	kHz

1. MachXO3L/LF supports the following modes:

• Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)

• Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)

2. Refer to the I^2C specification for timing requirements.

SPI Port Timing Specifications¹

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCK clock frequency		45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-9. Output Test Load, LVTTL and LVCMOS Standards



Table 3-6. Test Fixture Required Components	, Non-Terminated Interfaces
---	-----------------------------

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)			LVTTL, LVCMOS 3.3 = 1.5 V	_
			LVCMOS 2.5 = $V_{CCIO}/2$	_
	∞	0pF	LVCMOS 1.8 = $V_{CCIO}/2$	
	LVCMOS 1.5 = $V_{CCIO}/2$		LVCMOS 1.5 = $V_{CCIO}/2$	_
			LVCMOS 1.2 = $V_{CCIO}/2$	_
LVTTL and LVCMOS 3.3 (Z -> H)			1.5	V _{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V _{OH}
Other LVCMOS (Z -> H)	188	0nE	V _{CCIO} /2	V _{OL}
Other LVCMOS (Z -> L)	100	орі	V _{CCIO} /2	V _{OH}
LVTTL + LVCMOS (H -> Z)			V _{OH} - 0.15	V _{OL}
LVTTL + LVCMOS (L -> Z)			V _{OL} - 0.15	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.



			MachXO3	L/LF-2100		
	WLCSP49	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324
General Purpose IO per Bank		•	•			•
Bank 0	19	24	50	71	50	71
Bank 1	0	26	52	62	52	68
Bank 2	13	26	52	72	52	72
Bank 3	0	7	16	22	16	24
Bank 4	0	7	16	14	16	16
Bank 5	6	10	20	27	20	28
Total General Purpose Single Ended IO	38	100	206	268	206	279
Differential IO per Bank						
Bank 0	10	12	25	36	25	36
Bank 1	0	13	26	30	26	34
Bank 2	6	13	26	36	26	36
Bank 3	0	3	8	10	8	12
Bank 4	0	3	8	6	8	8
Bank 5	3	5	10	13	10	14
Total General Purpose Differential IO	19	49	103	131	103	140
Dual Function IO	25	33	33	37	33	37
Number 7:1 or 8:1 Gearboxes						•
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	5	7	14	18	14	18
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	13	14	18	14	18
High-speed Differential Outputs						•
Bank 0	5	7	14	18	14	18
VCCIO Pins		•	•			•
Bank 0	2	1	4	4	4	4
Bank 1	0	1	3	4	4	4
Bank 2	1	1	4	4	4	4
Bank 3	0	1	2	2	1	2
Bank 4	0	1	2	2	2	2
Bank 5	1	1	2	2	1	2
VCC	2	4	8	8	8	10
GND	4	10	24	16	24	16
NC	0	0	0	13	1	0
Reserved for Configuration	1	1	1	1	1	1
Total Count of Bonded Pins	49	121	256	324	256	324



			Ма	chXO3L/LF	-4300		
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank							
Bank 0	29	24	50	71	50	71	83
Bank 1	0	26	52	62	52	68	84
Bank 2	20	26	52	72	52	72	84
Bank 3	7	7	16	22	16	24	28
Bank 4	0	7	16	14	16	16	24
Bank 5	7	10	20	27	20	28	32
Total General Purpose Single Ended IO	63	100	206	268	206	279	335
Differential IO per Bank							
Bank 0	15	12	25	36	25	36	42
Bank 1	0	13	26	30	26	34	42
Bank 2	10	13	26	36	26	36	42
Bank 3	3	3	8	10	8	12	14
Bank 4	0	3	8	6	8	8	12
Bank 5	3	5	10	13	10	14	16
Total General Purpose Differential IO	31	49	103	131	103	140	168
Dual Function IO	25	37	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21
High-speed Differential Outputs							
Bank 0	10	7	18	18	18	18	21
VCCIO Pins							
Bank 0	3	1	4	4	4	4	5
Bank 1	0	1	3	4	4	4	5
Bank 2	2	1	4	4	4	4	5
Bank 3	1	1	2	2	1	2	2
Bank 4	0	1	2	2	2	2	2
Bank 5	1	1	2	2	1	2	2
VCC	4	4	8	8	8	10	10
GND	6	10	24	16	24	16	33
NC	0	0	0	13	1	0	0
Reserved for Configuration	1	1	1	1	1	1	1
Total Count of Bonded Pins	81	121	256	324	256	324	400



LCMXO3L-9400C-6BG484I

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND
	Γ		I	Γ	I	I
Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-5BG4001	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND

2.5 V/3.3 V

6

Halogen-Free caBGA

484

IND

9400



MachXO3 Family Data Sheet Supplemental Information

January 2016

Advance Data Sheet DS1047

For Further Information

A variety of technical notes for the MachXO3 family are available on the Lattice web site.

- TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide
- TN1281, Implementing High-Speed Interfaces with MachXO3 Devices
- TN1280, MachXO3 sysIO Usage Guide
- TN1279, MachXO3 Programming and Configuration Usage Guide
- TN1074, PCB Layout Recommendations for BGA Packages
- TN1087, Minimizing System Interruption During Configuration Using TransFR Technology
- AN8066, Boundary Scan Testability with Lattice sysIO Capability
- MachXO3 Device Pinout Files
- Thermal Management document
- Lattice design tools

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