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Details	
Product Status	Active
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	121-VFBGA, CSPBGA
Supplier Device Package	121-CSFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-1300e-6mg121c

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MachXO3 Family Data Sheet Architecture

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Architecture Overview

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK[™] PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.





Notes:

MachXO3L/LF-640 is similar to MachXO3L/LF-1300. MachXO3L/LF-640 has a lower LUT count.

MachXO3L devices have NVCM, MachXO3LF devices have Flash.

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This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the $t_{I,OCK}$ parameter has been satisfied.

The MachXO3L/LF also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO3L/LF PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.



Figure 2-7. PLL Diagram

Table 2-4 provides signal descriptions of the PLL block.

Table 2-4	. PLL	Signal	Descriptions
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Port Name	I/O	Description			
CLKI	Ι	Input clock to PLL			
CLKFB	I	Feedback clock			
PHASESEL[1:0]	Ι	Select which output is affected by Dynamic Phase adjustment ports			
PHASEDIR	I	Dynamic Phase adjustment direction			
PHASESTEP	Ι	Dynamic Phase step – toggle shifts VCO phase adjust by one step.			



If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to TN1290, Memory Usage Guide for MachXO3 Devices.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. On the MachXO3L/LF devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO3L/LF devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

All PIO pairs can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these devices have on-chip differential termination and also provide PCI support.



PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Pin Name	I/О Туре	Description			
CE	Input	Clock Enable			
D	Input	Pin input from sysIO buffer.			
INDD	Output	Register bypassed input.			
INCK	Output	Clock input			
Q0	Output	DDR positive edge input			
Q1	Output	Registered input/DDR negative edge input			
D0	Input	Output signal from the core (SDR and DDR)			
D1	Input	Output signal from the core (DDR)			
TD	Input	Tri-state signal from the core			
Q	Output	Data output signals to sysIO Buffer			
TQ	Output	Tri-state output signals to sysIO Buffer			
SCLK	Input	System clock for input and output/tri-state blocks.			
RST	Input	Local set reset signal			

Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.



Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-13 shows a block diagram of the input gearbox.



Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-14 shows the output gearbox block diagram.



Table 2-12. Supported Output Standards

Output Standard	V _{CCIO} (Typ.)				
Single-Ended Interfaces					
LVTTL	3.3				
LVCMOS33	3.3				
LVCMOS25	2.5				
LVCMOS18	1.8				
LVCMOS15	1.5				
LVCMOS12	1.2				
LVCMOS33, Open Drain	_				
LVCMOS25, Open Drain	_				
LVCMOS18, Open Drain	—				
LVCMOS15, Open Drain	_				
LVCMOS12, Open Drain	_				
PCI33	3.3				
Differential Interfaces					
LVDS ¹	2.5, 3.3				
BLVDS, MLVDS, RSDS 1	2.5				
LVPECL ¹	3.3				
MIPI ¹	2.5				
LVTTLD	3.3				
LVCMOS33D	3.3				
LVCMOS25D	2.5				
LVCMOS18D	1.8				

1. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO3L/LF-1300 in the 256 Ball packages and the MachXO3L/LF-2100 and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO3L/LF-1300 and lower density devices have four banks (one bank per side). Figures 2-15 and 2-16 show the sysIO banks and their associated supplies for all devices.



Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
 - Watchdog timer
 - Clear timer on compare match
 - Fast PWM
 - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

Figure 2-20. Timer/Counter Block Diagram



Table 2-16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



Table 2-17. MachXO3L/LF Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1289, Power Estimation and Management for MachXO3 Devices.

Power On Reset

MachXO3L/LF devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO} (controls configuration) voltage levels. It then triggers download from the on-chip configuration NVCM/Flash memory after reaching the V_{PORUP} level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For "E" devices without voltage regulators, V_{CCINT} is the same as the V_{CC} supply voltage. For "C" devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as NVCM/Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration. Note that for "C" devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once an "E" device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a mini-mal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min) they should not shut down the bandgap or POR circuit.



sysIO Single-Ended DC Electrical Characteristics^{1, 2}

Input/Output	V _{IL}		VIH		V _{OL} Max. V _{OH} Min.		lo, Max,⁴	ו _{סם} Max.⁴
Standard	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)	(V)	(V)	(mA)	(mA)
						V 0.4	4	-4
					0.4		8	-8
	-0.3	0.8	2.0	3.6	0.4	VCCIO - 0.4	12	-12
							16	-16
					0.2	V _{CCIO} - 0.2	0.1	-0.1
							4	-4
					0.4	V 0.4	8	-8
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	VCCIO - 0.4	12	-12
							16	-16
					0.2	V _{CCIO} - 0.2	0.1	-0.1
							4	-4
	0.2	0.251/	0.651/	26	0.4	V _{CCIO} - 0.4	8	-8
	-0.3	0.35VCCIO	0.03 V CCIO	3.0			12	-12
					0.2 V _{CCIO} - 0.2	0.1	-0.1	
		-0.3 0.35V _{CCIO}	0.65V _{CCIO}	3.6 0.4 0.2	0.4	V _{CCIO} - 0.4	4	-4
LVCMOS 1.5	-0.3						8	-8
					V _{CCIO} - 0.2	0.1	-0.1	
					0.4		4	-2
LVCMOS 1.2	-0.3	0.35V _{CCIO}	0.65V _{CCIO}	3.6	0.4	VCCIO - 0.4	8	-6
					0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS25R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	-0.3	VREF-0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS10R25	-0.3	VREF-0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

 MachXO3L/LF devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO3L/LF devices do not meet the relevant JEDEC specification are documented in the table below.

2. MachXO3L/LF devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1280, MachXO3 sysIO Usage Guide.

3. The dual function I²C pins SCL and SDA are limited to a V_{IL} min of -0.25 V or to -0.3 V with a duration of <10 ns.

4. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive VCCIO or GND pad connections, or between the last VCCIO or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of n * 8 mA. "n" is the number of I/O pads between the two consecutive bank VCCIO or GND connections or between the last VCCIO and GND in a bank and the end of a bank. IO Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Diamond software.



Typical Building Block Function Performance – C/E Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	–6 Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

 The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.



Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
MIPI	450	MHz
LVDS25	400	MHz
LVDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz



			-6			-5		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units	
Generic DDF GDDRX1_RX	RX1 Inputs with Clock and Data Aligned at K.SCLK.Aligned ^{8,9}	Pin Using PCLK Pin for Clo	ock Inpu	t –				
t _{DVA}	Input Data Valid After CLK			0.317	—	0.344	UI	
t _{DVE}	Input Data Hold After CLK	All MachXO3L/LF	0.742		0.702		UI	
f _{DATA}	DDRX1 Input Data Speed	-devices, all sides		300	—	250	Mbps	
f _{DDRX1}	DDRX1 SCLK Frequency			150	—	125	MHz	
Generic DD GDDRX1_R	RX1 Inputs with Clock and Data Centered X.SCLK.Centered ^{8, 9}	at Pin Using PCLK Pin fo	or Clock	Input –		1	1	
t _{SU}	Input Data Setup Before CLK		0.566		0.560		ns	
t _{HO}	Input Data Hold After CLK	All MachXO3L/LF	0.778		0.879		ns	
f _{DATA}	DDRX1 Input Data Speed	-devices, all sides		300	—		Mbps	
f _{DDRX1}	DDRX1 SCLK Frequency		_	150	—	125	MHz	
Generic DD GDDRX2_R	RX2 Inputs with Clock and Data Aligned at X.ECLK.Aligned ^{8, 9}	Pin Using PCLK Pin for C	lock Inp	out –				
t _{DVA}	Input Data Valid After CLK		—	0.316	—	0.342	UI	
t _{DVE}	Input Data Hold After CLK	-	0.710		0.675		UI	
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO3L/LF devices,		664	—	554	Mbps	
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only		332	—	277	MHz	
f _{SCLK}	SCLK Frequency			166	—	139	MHz	
Generic DD GDDRX2_R	Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input –							
t _{SU}	Input Data Setup Before CLK		0.233		0.219		ns	
t _{HO}	Input Data Hold After CLK	-	0.287	—	0.287		ns	
f _{DATA}	DDRX2 Serial Input Data Speed	MachXO3L/LF devices,		664	—	554	Mbps	
f _{DDRX2}	DDRX2 ECLK Frequency	bottom side only		332	—	277	MHz	
f _{SCLK}	SCLK Frequency	-		166	—	139	MHz	
Generic DDI	R4 Inputs with Clock and Data Aligned at P	in Using PCLK Pin for Cloo	k Input	- GDDR	X4_RX.	ECLK.A	ligned ⁸	
t _{DVA}	Input Data Valid After ECLK		—	0.307	—	0.320	UI	
t _{DVE}	Input Data Hold After ECLK	-	0.782	—	0.699	—	UI	
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO3L/LF devices,		800	—	630	Mbps	
f _{DDRX4}	DDRX4 ECLK Frequency	bottom side only		400	—	315	MHz	
f _{SCLK}	SCLK Frequency			100	—	79	MHz	
Generic DDF	A4 Inputs with Clock and Data Centered at P	in Using PCLK Pin for Cloc	k Input	- GDDR	X4_RX.E	CLK.Ce	entered ⁸	
t _{SU}	Input Data Setup Before ECLK		0.233	—	0.219	—	ns	
t _{HO}	Input Data Hold After ECLK		0.287	—	0.287		ns	
f _{DATA}	DDRX4 Serial Input Data Speed	MachXO3L/LF devices,	_	800	—	630	Mbps	
f _{DDRX4}	DDRX4 ECLK Frequency		_	400	—	315	MHz	
f _{SCLK}	SCLK Frequency			100	—	79	MHz	
7:1 LVDS In	outs (GDDR71_RX.ECLK.7:1) ⁹							
t _{DVA}	Input Data Valid After ECLK		—	0.290	—	0.320	UI	
t _{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	UI	
f _{DATA}	DDR71 Serial Input Data Speed	MachXO3L/LF devices,	—	756	—	630	Mbps	
f _{DDR71}	DDR71 ECLK Frequency	bottom side only	—	378	—	315	MHz	
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (mini- mum limited by PLL)]		108	—	90	MHz	



JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	TCK clock frequency	—	25	MHz
t _{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t _{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t _{BTS}	TCK [BSCAN] setup time	10	—	ns
t _{BTH}	TCK [BSCAN] hold time	8	—	ns
t _{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t _{BTCODIS}	TAP controller falling edge of clock to valid disable	—	10	ns
t _{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t _{BTCRS}	BSCAN test capture register setup time	8	—	ns
t _{BTCRH}	BSCAN test capture register hold time	20	—	ns
t _{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t _{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable		25	ns
t _{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-8. JTAG Port Timing Waveforms





I²C Port Timing Specifications^{1, 2}

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCL clock frequency		400	kHz

1. MachXO3L/LF supports the following modes:

• Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)

• Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)

2. Refer to the I^2C specification for timing requirements.

SPI Port Timing Specifications¹

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCK clock frequency		45	MHz

1. Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-9. Output Test Load, LVTTL and LVCMOS Standards



Table 3-6. Test Fixture Required Components	, Non-Terminated Interfaces
---------------------------------------------	-----------------------------

Test Condition	R1	CL	Timing Ref.	VT
	œ		LVTTL, LVCMOS 3.3 = 1.5 V	_
		0pF	LVCMOS 2.5 = $V_{CCIO}/2$	_
LVTTL and LVCMOS settings (L -> H, H -> L)			LVCMOS 1.8 = $V_{CCIO}/2$	
			LVCMOS 1.5 = $V_{CCIO}/2$	_
			LVCMOS 1.2 = $V_{CCIO}/2$	_
LVTTL and LVCMOS 3.3 (Z -> H)			1.5	V _{OL}
LVTTL and LVCMOS 3.3 (Z -> L)	100	0.5	1.5	V _{OH}
Other LVCMOS (Z -> H)			V _{CCIO} /2	V _{OL}
Other LVCMOS (Z -> L) LVTTL + LVCMOS (H -> Z)	100	орі	V _{CCIO} /2	V _{OH}
			V _{OH} - 0.15	V _{OL}
LVTTL + LVCMOS (L -> Z)			V _{OL} - 0.15	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.



Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions				
Configuration (Dual fu	Configuration (Dual function pins used during sysCONFIG)					
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.				
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.				
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.				
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.				
SN	I	Slave SPI active low chip select input.				
CSSPIN	I/O	Master SPI active low chip select output.				
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.				
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.				
SCL	I/O	Slave I ² C clock input and master I ² C clock output.				
SDA	I/O	Slave I ² C data input and master I ² C data output.				



	MachXO3L/LF-6900					
	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400	
General Purpose IO per Bank		•	•		•	
Bank 0	50	73	50	71	83	
Bank 1	52	68	52	68	84	
Bank 2	52	72	52	72	84	
Bank 3	16	24	16	24	28	
Bank 4	16	16	16	16	24	
Bank 5	20	28	20	28	32	
Total General Purpose Single Ended IO	206	281	206	279	335	
Differential IO per Bank		•	•		•	
Bank 0	25	36	25	36	42	
Bank 1	26	34	26	34	42	
Bank 2	26	36	26	36	42	
Bank 3	8	12	8	12	14	
Bank 4	8	8	8	8	12	
Bank 5	10	14	10	14	16	
Total General Purpose Differential IO	103	140	103	140	168	
Dual Function IO	37	37	37	37	37	
Number 7:1 or 8:1 Gearboxes		•	•			
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	21	20	21	21	
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	21	20	21	21	
High-speed Differential Outputs		•	•			
Bank 0	20	21	20	21	21	
VCCIO Pins		•	•		•	
Bank 0	4	4	4	4	5	
Bank 1	3	4	4	4	5	
Bank 2	4	4	4	4	5	
Bank 3	2	2	1	2	2	
Bank 4	2	2	2	2	2	
Bank 5	2	2	1	2	2	
VCC	8	8	8	10	10	
GND	24	16	24	16	33	
NC	0	0	1	0	0	
Reserved for Configuration	1	1	1	1	1	
Total Count of Bonded Pins	256	324	256	324	400	



MachXO3 Family Data Sheet Revision History

February 2017

Advance Data Sheet DS1047

Date	Version	Section	Change Summary
February 2017	1.8	Architecture	Updated Supported Standards section. Corrected "MDVS" to "MLDVS" in Table 2-11, Supported Input Standards.
		DC and Switching Characteristics	Updated ESD Performance section. Added reference to the MachXO2 Product Family Qualification Summary document.
			Updated Static Supply Current – C/E Devices section. Added footnote 7.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. — Populated values for MachXO3L/LF-9400. — Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, corrected "t _{DVB} " to "t _{DIB} " and "t _{DVA} " to "t _{DIA} " and revised their descriptions. — Added Figure 3-6, Receiver GDDR71_RX Waveforms and Figure 3-7, Transmitter GDDR71_TX Waveforms.
		Pinout Information	Updated the Pin Information Summary section. Added MachXO3L/LF- 9600C packages.
May 2016	1.7	DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Modified I/O Tri-state Volt- age Applied and Dedicated Input Voltage Applied footnotes.
			Updated sysIO Recommended Operating Conditions section. — Added standards. — Added V _{REF} (V) — Added footnote 4.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Added I/O standards.
		Ordering Information	Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.

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Date	Version	Section	Change Summary
September 2015	1.5	DC and Switching Characteristics	Updated the MIPI D-PHY Emulation section. Revised Table 3-5, MIPI D- PHY Output DC Conditions. — Revised RL Typ. value. — Revised RH description and values.
			Updated the Maximum sysIO Buffer Performance section. Revised MIPI Max. Speed value.
			Updated the MachXO3L/LF External Switching Characteristics – C/E Devices section. Added footnotes 14 and 15.
August 2015	1.4	Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.
		Ordering Information	Updated the top side markings section to indicate the use of LMXO3LF for the LCMXO3LF device.
March 2015	1.3	All	General update. Added MachXO3LF devices.
October 2014	1.2	Introduction	Updated Table 1-1, MachXO3L Family Selection Guide. Revised XO3L- 2100 and XO3L-4300 IO for 324-ball csfBGA package.
		Architecture	Updated the Dual Boot section. Corrected information on where the pri- mary bitstream and the golden image must reside.
		Pinout Information	Updated the Pin Information Summary section.
			Changed General Purpose IO Bank 5 values for MachXO3L-2100 and MachXO3L-4300 CSFBGA 324 package.
			Changed Number 7:1 or 8:1 Gearboxes for MachXO3L-640 and MachXO3L-1300.
			Removed DQS Groups (Bank 1) section.
			Changed VCCIO Pins Bank 1 values for MachXO3L-1300, MachXO3L- 2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.
			Changed GND values for MachXO3L-1300, MachXO3L-2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.
			Changed NC values for MachXO3L-2100 and MachXO3L-4300 CSF- BGA 324 package.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	1.1	DC and Switching Characteristics	Updated the Static Supply Current – C/E Devices section. Added devices.
			Updated the Programming and Erase Supply Current – C/E Device section. Added devices.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Revised footnote 4.
			Added the NVCM Download Time section.
			Updated the Typical Building Block Function Performance – C/E Devices section. Added information to footnote.
		Pinout Information	Updated the Pin Information Summary section.
		Ordering Information	Updated the MachXO3L Part Number Description section. Added packages.
			Updated the Ordering Information section. General update.





Date	Version	Section	Change Summary
June 2014	1.0	—	Product name/trademark adjustment.
		Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Changed fcCSP packages to csfBGA. Adjusted 121-ball csfBGA arrow.
			Introduction section general update.
		Architecture	General update.
		DC and Switching Characteristics	Updated sysIO Recommended Operating Conditions section. Removed V _{REF} (V) column. Added standards.
			Updated Maximum sysIO Buffer Performance section. Added MIPI I/O standard.
			Updated MIPI D-PHY Emulation section. Changed Low Speed to Low Power. Updated Table 3-4, MIPI DC Conditions.
			Updated Table 3-5, MIPI D-PHY Output DC Conditions.
			Updated Maximum sysIO Buffer Performance section.
			Updated MachXO3L External Switching Characteristics – C/E Device section.
May 2014	00.3	Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Moved 121-ball fcCSP arrow.
			General update of Introduction section.
		Architecture	General update.
		Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
		Ordering Information	Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
			Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers.
February 2014	00.2	DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.
	00.1		Initial release.