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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

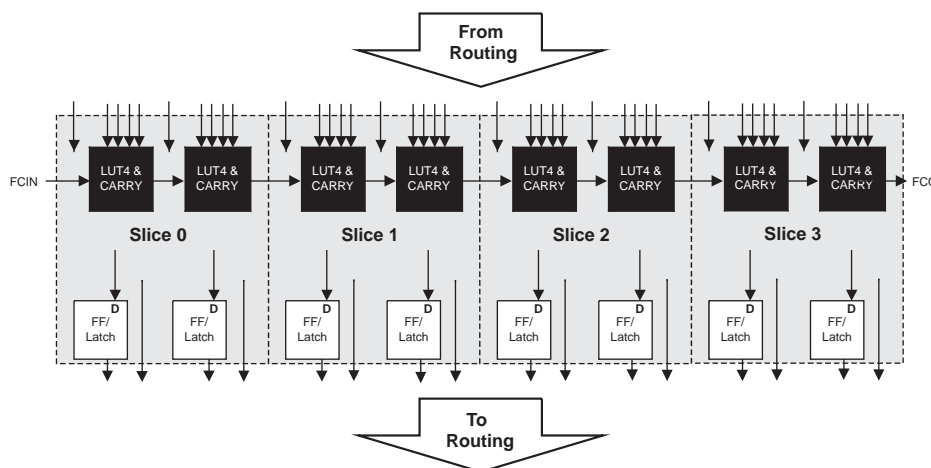
### Details

Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	206
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-CABGA (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-2100c-6bg256c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-2100c-6bg256c</a>

## PFU Blocks

The core of the MachXO3L/LF device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

**Figure 2-3. PFU Block Diagram**



## Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

**Table 2-1. Resources and Modes Available per Slice**

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the  $t_{LOCK}$  parameter has been satisfied.

The MachXO3L/LF also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the [sysCLOCK PLL Timing](#) table.

The MachXO3L/LF PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the  $t_{LOCK}$  parameter has been satisfied. The timing parameters for the PLL are shown in the [sysCLOCK PLL Timing](#) table.

For more details on the PLL and the WISHBONE interface, see TN1282, [MachXO3 sysCLOCK PLL Design and Usage Guide](#).

**Figure 2-7. PLL Diagram**

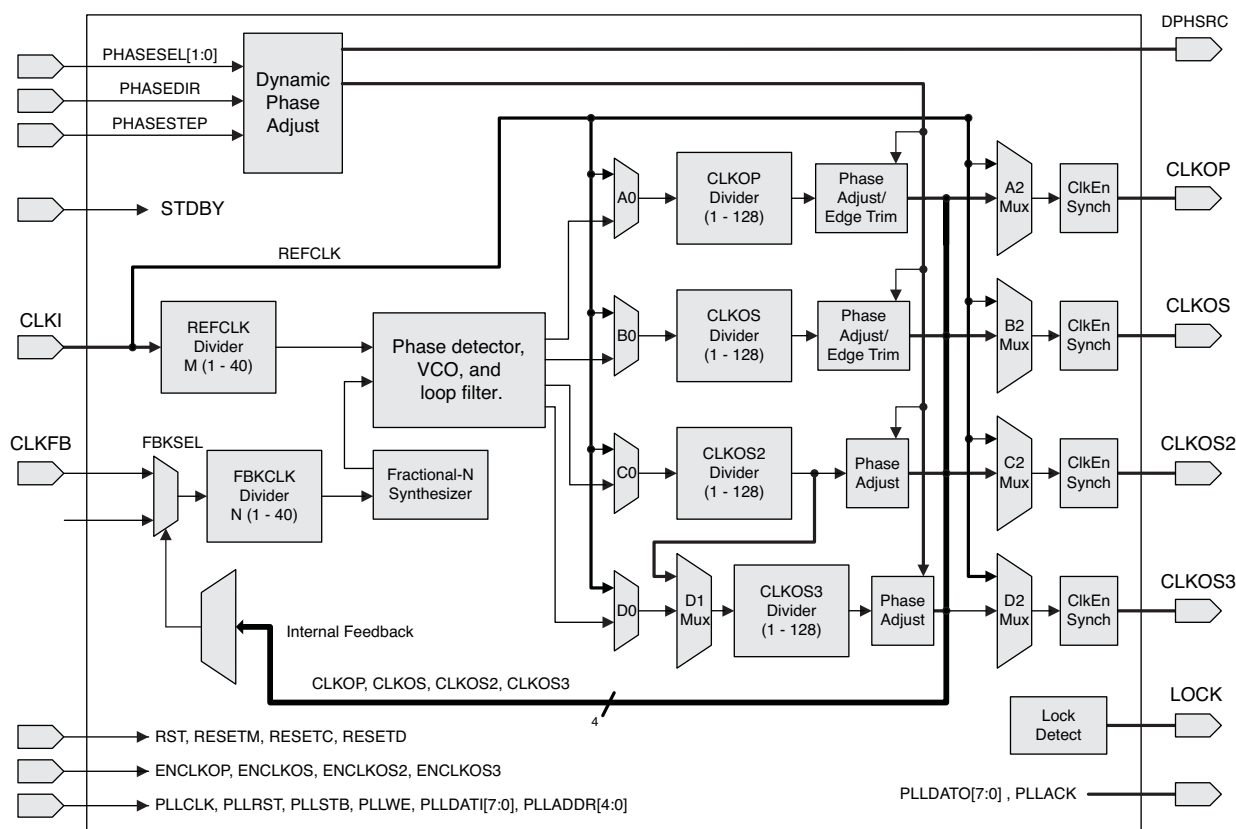


Table 2-4 provides signal descriptions of the PLL block.

**Table 2-4. PLL Signal Descriptions**

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.

Table 2-11 shows the I/O standards (together with their supply and reference voltages) supported by the MachXO3L/LF devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1280, [MachXO3 sysIO Usage Guide](#).

**Table 2-11. Supported Input Standards**

Input Standard	VCCIO (Typ.)				
	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V
<b>Single-Ended Interfaces</b>					
LVTTTL	Yes				
LVC MOS33	Yes				
LVC MOS25		Yes			
LVC MOS18			Yes		
LVC MOS15				Yes	
LVC MOS12					Yes
PCI	Yes				
<b>Differential Interfaces</b>					
LVDS	Yes	Yes			
BLVDS, MLVDS, LVPECL, RSDS	Yes	Yes			
MIPI <sup>1</sup>	Yes	Yes			
LVTTL D	Yes				
LVC MOS33D	Yes				
LVC MOS25D		Yes			
LVC MOS18D			Yes		

1. These interfaces can be emulated with external resistors in all devices.

For more details on these embedded functions, please refer to TN1293, [Using Hardened Control Functions in MachXO3 Devices](#).

## User Flash Memory (UFM)

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, [Using Hardened Control Functions in MachXO3 Devices](#).

## Standby Mode and Power Saving Options

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V  $V_{CC}$  and 3.3 V  $V_{CC}$  while the E devices operate at 1.2 V  $V_{CC}$ .

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I<sup>2</sup>C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

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## Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V<sub>CCIO</sub> Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

### Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

1. Internal NVCM/Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, [MachXO3 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, [MachXO3 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, [MachXO3 Programming and Configuration Usage Guide](#).

### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

### Power-On-Reset Voltage Levels<sup>1, 2, 3, 4, 5</sup>

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{PORUP}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring $V_{CCINT}$ and $V_{CCIO0}$ )	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external $V_{CC}$ power supply)	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CCINT}$ )	0.75	—	0.93	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring $V_{CC}$ )	0.98	—	1.33	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{CCINT}$ )	—	0.6	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring $V_{CC}$ )	—	0.96	—	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. For devices without voltage regulators  $V_{CCINT}$  is the same as the  $V_{CC}$  supply voltage. For devices with voltage regulators,  $V_{CCINT}$  is regulated from the  $V_{CC}$  supply voltage.
3. Note that  $V_{PORUP}$  (min.) and  $V_{PORDNBG}$  (max.) are in different process corners. For any given process corner  $V_{PORDNBG}$  (max.) is always 12.0 mV below  $V_{PORUP}$  (min.).
4.  $V_{PORUPEXT}$  is for C devices only. In these devices a separate POR circuit monitors the external  $V_{CC}$  power supply.
5.  $V_{CCIO0}$  does not have a Power-On-Reset ramp down trip point.  $V_{CCIO0}$  must remain within the Recommended Operating Conditions to ensure proper operation.

### Hot Socketing Specifications<sup>1, 2, 3</sup>

Symbol	Parameter	Condition	Max.	Units
$I_{DK}$	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	+/-1000	$\mu A$

1. Insensitive to sequence of  $V_{CC}$  and  $V_{CCIO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$  and  $V_{CCIO}$ .
2.  $0 < V_{CC} < V_{CC}$  (MAX),  $0 < V_{CCIO} < V_{CCIO}$  (MAX).
3.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PD}$  or  $I_{BH}$ .

### ESD Performance

Please refer to the [MachXO2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

## sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

### LVDS

#### Over Recommended Operating Conditions

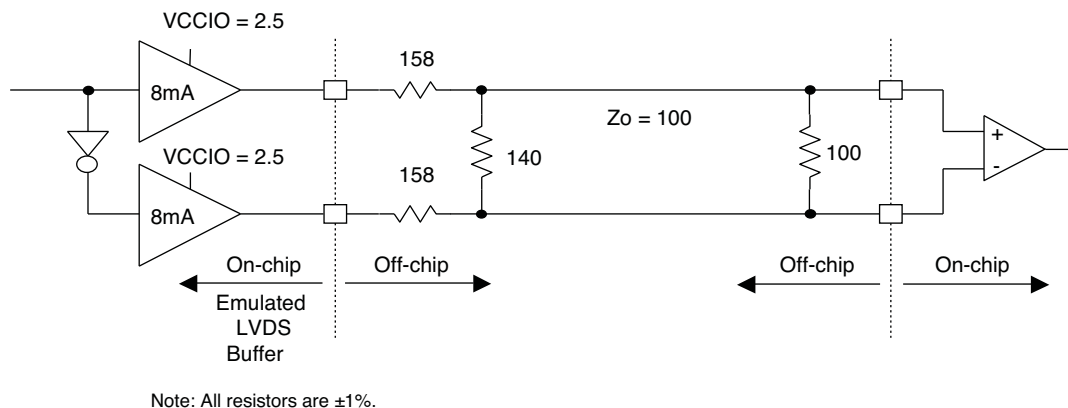
Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}$ $V_{INM}$	Input Voltage	$V_{CCIO} = 3.3\text{ V}$	0	—	2.605	V
		$V_{CCIO} = 2.5\text{ V}$	0	—	2.05	V
$V_{THD}$	Differential Input Threshold		$\pm 100$	—		mV
$V_{CM}$	Input Common Mode Voltage	$V_{CCIO} = 3.3\text{ V}$	0.05	—	2.6	V
		$V_{CCIO} = 2.5\text{ V}$	0.05	—	2.0	V
$I_{IN}$	Input current	Power on	—	—	$\pm 10$	$\mu\text{A}$
$V_{OH}$	Output high voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\text{ Ohm}$	—	1.375	—	V
$V_{OL}$	Output low voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\text{ Ohm}$	0.90	1.025	—	V
$V_{OD}$	Output voltage differential	$(V_{OP} - V_{OM})$ , $R_T = 100\text{ Ohm}$	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between high and low		—	—	50	mV
$V_{OS}$	Output voltage offset	$(V_{OP} - V_{OM})/2$ , $R_T = 100\text{ Ohm}$	1.125	1.20	1.395	V
$\Delta V_{OS}$	Change in $V_{OS}$ between H and L		—	—	50	mV
$I_{OSD}$	Output short circuit current	$V_{OD} = 0\text{ V}$ driver outputs shorted	—	—	24	mA



### LVDS Emulation

MachXO3L/LF devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

**Figure 3-1. LVDS Using External Resistors (LVDS25E)**



**Table 3-1. LVDS25E DC Conditions**

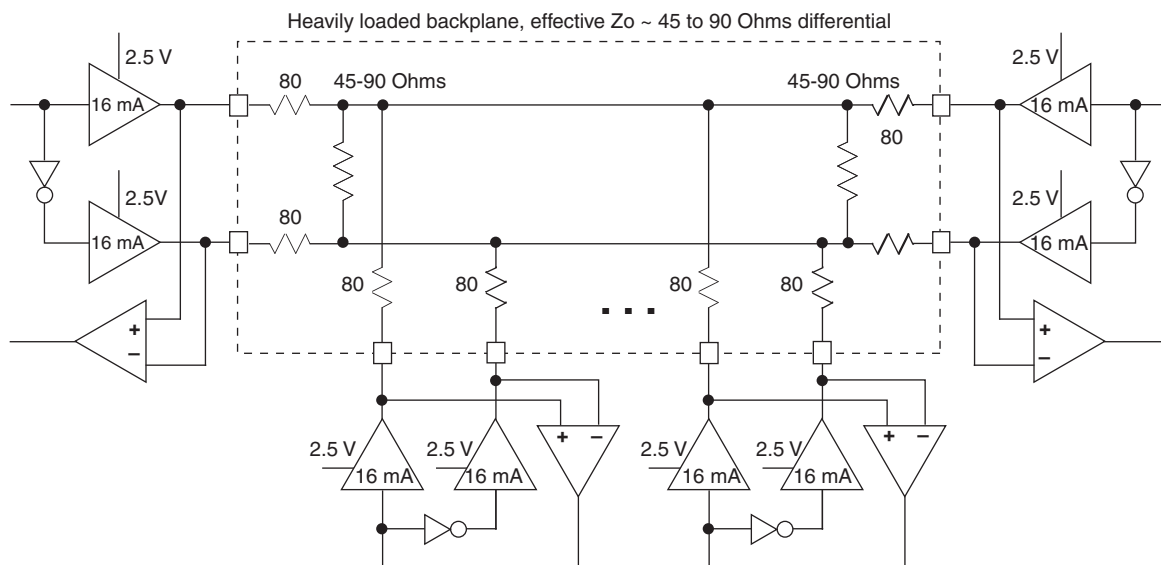
#### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	158	Ohms
$R_P$	Driver parallel resistor	140	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.35	V
$V_{CM}$	Output common mode voltage	1.25	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	6.03	mA

### BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

**Figure 3-2. BLVDS Multi-point Output Example**



**Table 3-2. BLVDS DC Conditions<sup>1</sup>**

#### Over Recommended Operating Conditions

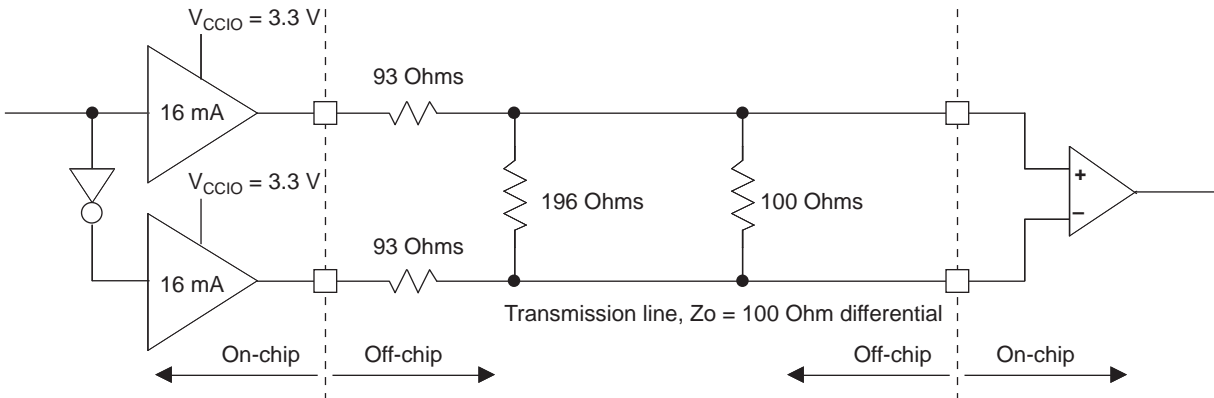
Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z <sub>OUT</sub>	Output impedance	20	20	Ohms
R <sub>S</sub>	Driver series resistance	80	80	Ohms
R <sub>TLEFT</sub>	Left end termination	45	90	Ohms
R <sub>TRIGHT</sub>	Right end termination	45	90	Ohms
V <sub>OH</sub>	Output high voltage	1.376	1.480	V
V <sub>OL</sub>	Output low voltage	1.124	1.020	V
V <sub>OD</sub>	Output differential voltage	0.253	0.459	V
V <sub>CM</sub>	Output common mode voltage	1.250	1.250	V
I <sub>DC</sub>	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

## LVPECL

The MachXO3L/LF family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

**Figure 3-3. Differential LVPECL**



**Table 3-3. LVPECL DC Conditions<sup>1</sup>**

### Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	93	Ohms
$R_P$	Driver parallel resistor	196	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	2.05	V
$V_{OL}$	Output low voltage	1.25	V
$V_{OD}$	Output differential voltage	0.80	V
$V_{CM}$	Output common mode voltage	1.65	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

## Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
MIPI	450	MHz
LVDS25	400	MHz
LVDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVC MOS33	150	MHz
LVC MOS33D	150	MHz
LVC MOS25	150	MHz
LVC MOS25D	150	MHz
LVC MOS18	150	MHz
LVC MOS18D	150	MHz
LVC MOS15	150	MHz
LVC MOS15D	150	MHz
LVC MOS12	91	MHz
LVC MOS12D	91	MHz

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_TX.ECLK.Centered <sup>8, 9</sup>							
t <sub>DVB</sub>	Output Data Valid Before CLK Output	MachXO3L/LF devices, top side only	0.455	—	0.570	—	ns
t <sub>DVA</sub>	Output Data Valid After CLK Output		0.455	—	0.570	—	ns
f <sub>DATA</sub>	DDRX4 Serial Output Data Speed		—	800	—	630	Mbps
f <sub>DDRX4</sub>	DDRX4 ECLK Frequency (minimum limited by PLL)		—	400	—	315	MHz
f <sub>SCLK</sub>	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1 <sup>8, 9</sup>							
t <sub>DIB</sub>	Output Data Invalid Before CLK Output	MachXO3L/LF devices, top side only	—	0.160	—	0.180	ns
t <sub>DIA</sub>	Output Data Invalid After CLK Output		—	0.160	—	0.180	ns
f <sub>DATA</sub>	DDR71 Serial Output Data Speed		—	756	—	630	Mbps
f <sub>DDR71</sub>	DDR71 ECLK Frequency		—	378	—	315	MHz
f <sub>CLKOUT</sub>	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDR4_TX.ECLK.Centered <sup>10, 11, 12</sup>							
t <sub>DVB</sub>	Output Data Valid Before CLK Output	All MachXO3L/LF devices, top side only	0.200	—	0.200	—	UI
t <sub>DVA</sub>	Output Data Valid After CLK Output		0.200	—	0.200	—	UI
f <sub>DATA</sub> <sup>14</sup>	MIPI D-PHY Output Data Speed		—	900	—	900	Mbps
f <sub>DDRX4</sub> <sup>14</sup>	MIPI D-PHY ECLK Frequency (minimum limited by PLL)		—	450	—	450	MHz
f <sub>SCLK</sub> <sup>14</sup>	SCLK Frequency		—	112.5	—	112.5	MHz

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pF load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode t<sub>SU</sub> = t<sub>HO</sub> = (t<sub>DVE</sub> - t<sub>DVA</sub> - 0.03 ns)/2.
- The t<sub>SU\_DEL</sub> and t<sub>H\_DEL</sub> values use the SCLK\_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).
- This number for general purpose usage. Duty cycle tolerance is +/-10%.
- Duty cycle is +/- 5% for system usage.
- Performance is calculated with 0.225 UI.
- Performance is calculated with 0.20 UI.
- Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.
- Performance for Industrial devices and -5 devices are not modeled in the Diamond design tool.
- The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.
- Above 800 Mbps is only supported with WLCSP and csfBGA packages
- Between 800 Mbps to 900 Mbps:
  - VIDTH exceeds the MIPI D-PHY Input DC Conditions Table 3-4 and can be calculated with the equation t<sub>SU</sub> or t<sub>H</sub> = -0.0005\*VIDTH + 0.3284
  - Example calculations
    - t<sub>SU</sub> and t<sub>HO</sub> = 0.28 with VIDTH = 100 mV
    - t<sub>SU</sub> and t<sub>HO</sub> = 0.25 with VIDTH = 170 mV
    - t<sub>SU</sub> and t<sub>HO</sub> = 0.20 with VIDTH = 270 mV

**NVCM/Flash Download Time<sup>1, 2</sup>**

Symbol	Parameter	Device	Typ.	Units
t <sub>REFRESH</sub>	POR to Device I/O Active	LCMXO3L/LF-640	1.9	ms
		LCMXO3L/LF-1300	1.9	ms
		LCMXO3L/LF-1300 256-Ball Package	1.4	ms
		LCMXO3L/LF-2100	1.4	ms
		LCMXO3L/LF-2100 324-Ball Package	2.4	ms
		LCMXO3L/LF-4300	2.4	ms
		LCMXO3L/LF-4300 400-Ball Package	3.8	ms
		LCMXO3L/LF-6900	3.8	ms
		LCMXO3L/LF-9400C	5.2	ms

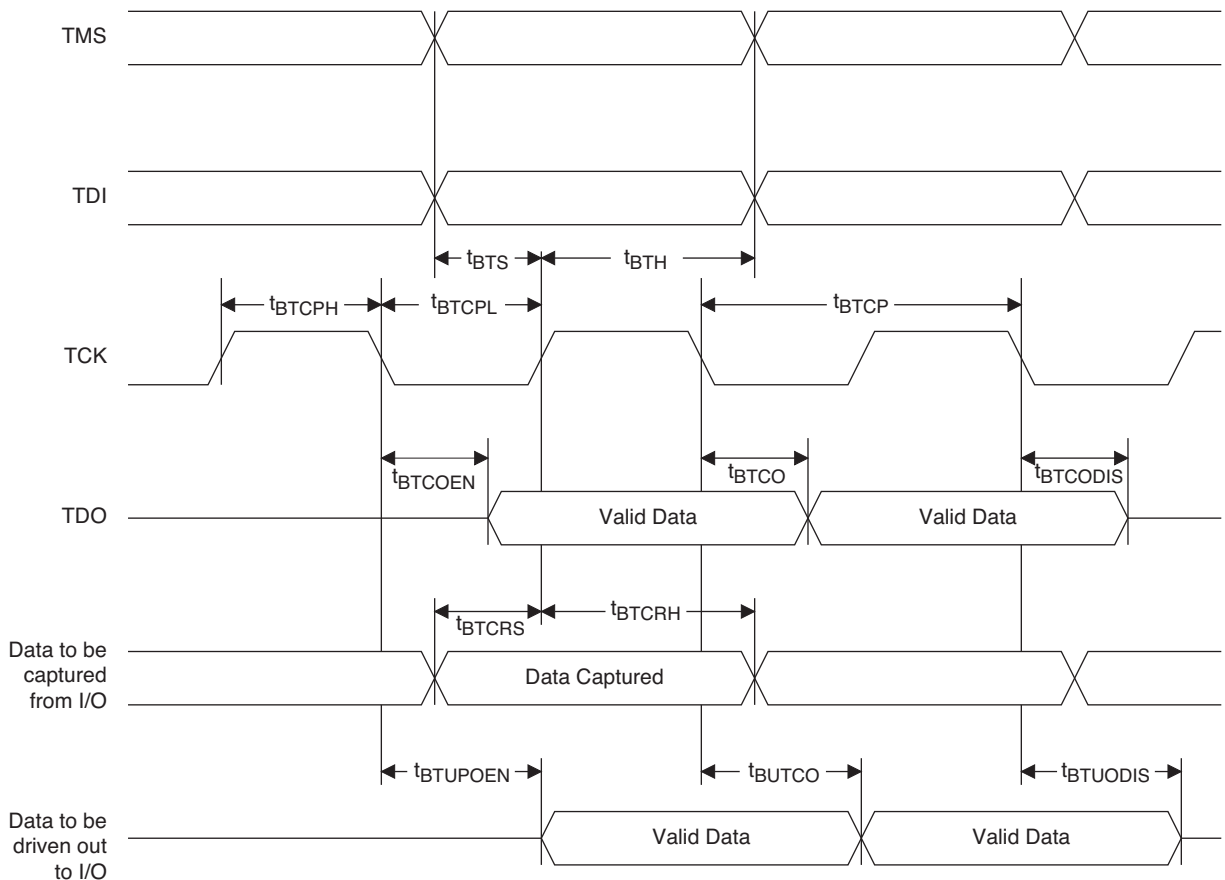
1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.

### JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
$f_{MAX}$	TCK clock frequency	—	25	MHz
$t_{BTCPH}$	TCK [BSCAN] clock pulse width high	20	—	ns
$t_{BTCPL}$	TCK [BSCAN] clock pulse width low	20	—	ns
$t_{BTS}$	TCK [BSCAN] setup time	10	—	ns
$t_{BTH}$	TCK [BSCAN] hold time	8	—	ns
$t_{BTCO}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
$t_{BTCOEN}$	TAP controller falling edge of clock to valid enable	—	10	ns
$t_{BTCRS}$	BSCAN test capture register setup time	8	—	ns
$t_{BTCRH}$	BSCAN test capture register hold time	20	—	ns
$t_{BUTCO}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

**Figure 3-8. JTAG Port Timing Waveforms**



### Signal Descriptions

Signal Name	I/O	Descriptions
<b>General Purpose</b>		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B/C/D] indicates the PIO within the group to which the pad is connected.</p> <p>Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/Os for user logic.</p> <p>During configuration of the user-programmable I/Os, the user has an option to tri-state the I/Os and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/Os to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/Os will be tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/Os with pull-up resistors enabled when the device is erased.</p>
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
VCC	—	V <sub>CC</sub> – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIOx	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.
<b>PLL and Clock Functions</b> (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
<b>Test and Programming</b> (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	<p>Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then:</p> <p>If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O.</p> <p>If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.</p> <p>For more details, refer to TN1279, <a href="#">MachXO3 Programming and Configuration Usage Guide</a>.</p>



## Pin Information Summary

	MachXO3L/LF-640	MachXO3L/LF-1300			
	CSFBGA121	WLCSP36	CSFBGA121	CSFBGA256	CABGA256
<b>General Purpose IO per Bank</b>					
Bank 0	24	15	24	50	50
Bank 1	26	0	26	52	52
Bank 2	26	9	26	52	52
Bank 3	24	4	24	16	16
Bank 4	0	0	0	16	16
Bank 5	0	0	0	20	20
<b>Total General Purpose Single Ended IO</b>	100	28	100	206	206
<b>Differential IO per Bank</b>					
Bank 0	12	8	12	25	25
Bank 1	13	0	13	26	26
Bank 2	13	4	13	26	26
Bank 3	11	2	11	8	8
Bank 4	0	0	0	8	8
Bank 5	0	0	0	10	10
<b>Total General Purpose Differential IO</b>	49	14	49	103	103
<b>Dual Function IO</b>	33	25	33	33	33
<b>Number 7:1 or 8:1 Gearboxes</b>					
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	7	3	7	14	14
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	7	2	7	14	14
<b>High-speed Differential Outputs</b>					
Bank 0	7	3	7	14	14
<b>VCCIO Pins</b>					
Bank 0	1	1	1	4	4
Bank 1	1	0	1	3	4
Bank 2	1	1	1	4	4
Bank 3	3	1	3	2	1
Bank 4	0	0	0	2	2
Bank 5	0	0	0	2	1
<b>VCC</b>	4	2	4	8	8
<b>GND</b>	10	2	10	24	24
<b>NC</b>	0	0	0	0	1
<b>Reserved for Configuration</b>	1	1	1	1	1
<b>Total Count of Bonded Pins</b>	121	36	121	256	256

	MachXO3L/LF-4300						
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
<b>General Purpose IO per Bank</b>							
Bank 0	29	24	50	71	50	71	83
Bank 1	0	26	52	62	52	68	84
Bank 2	20	26	52	72	52	72	84
Bank 3	7	7	16	22	16	24	28
Bank 4	0	7	16	14	16	16	24
Bank 5	7	10	20	27	20	28	32
<b>Total General Purpose Single Ended IO</b>	63	100	206	268	206	279	335
<b>Differential IO per Bank</b>							
Bank 0	15	12	25	36	25	36	42
Bank 1	0	13	26	30	26	34	42
Bank 2	10	13	26	36	26	36	42
Bank 3	3	3	8	10	8	12	14
Bank 4	0	3	8	6	8	8	12
Bank 5	3	5	10	13	10	14	16
<b>Total General Purpose Differential IO</b>	31	49	103	131	103	140	168
<b>Dual Function IO</b>	25	37	37	37	37	37	37
<b>Number 7:1 or 8:1 Gearboxes</b>							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21
<b>High-speed Differential Outputs</b>							
Bank 0	10	7	18	18	18	18	21
<b>VCCIO Pins</b>							
Bank 0	3	1	4	4	4	4	5
Bank 1	0	1	3	4	4	4	5
Bank 2	2	1	4	4	4	4	5
Bank 3	1	1	2	2	1	2	2
Bank 4	0	1	2	2	2	2	2
Bank 5	1	1	2	2	1	2	2
<b>VCC</b>	4	4	8	8	8	10	10
<b>GND</b>	6	10	24	16	24	16	33
<b>NC</b>	0	0	0	13	1	0	0
<b>Reserved for Configuration</b>	1	1	1	1	1	1	1
<b>Total Count of Bonded Pins</b>	<b>81</b>	<b>121</b>	<b>256</b>	<b>324</b>	<b>256</b>	<b>324</b>	<b>400</b>

	MachXO3L/LF-9400C			
	CSFBGA256	CABGA256	CABGA400	CABGA484
<b>General Purpose IO per Bank</b>				
Bank 0	50	50	83	95
Bank 1	52	52	84	96
Bank 2	52	52	84	96
Bank 3	16	16	28	36
Bank 4	16	16	24	24
Bank 5	20	20	32	36
<b>Total General Purpose Single Ended IO</b>	<b>206</b>	<b>206</b>	<b>335</b>	<b>383</b>
<b>Differential IO per Bank</b>				
Bank 0	25	25	42	48
Bank 1	26	26	42	48
Bank 2	26	26	42	48
Bank 3	8	8	14	18
Bank 4	8	8	12	12
Bank 5	10	10	16	18
<b>Total General Purpose Differential IO</b>	<b>103</b>	<b>103</b>	<b>168</b>	<b>192</b>
<b>Dual Function IO</b>	<b>37</b>	<b>37</b>	<b>37</b>	<b>45</b>
<b>Number 7:1 or 8:1 Gearboxes</b>				
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	20	22	24
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	20	22	24
<b>High-speed Differential Outputs</b>				
Bank 0	20	20	21	24
<b>VCCIO Pins</b>				
Bank 0	4	4	5	9
Bank 1	3	4	5	9
Bank 2	4	4	5	9
Bank 3	2	1	2	3
Bank 4	2	2	2	3
Bank 5	2	1	2	3
<b>VCC</b>	<b>8</b>	<b>8</b>	<b>10</b>	<b>12</b>
<b>GND</b>	<b>24</b>	<b>24</b>	<b>33</b>	<b>52</b>
<b>NC</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>0</b>
<b>Reserved for Configuration</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>
<b>Total Count of Bonded Pins</b>	<b>256</b>	<b>256</b>	<b>400</b>	<b>484</b>

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3LF-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3LF-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

## For Further Information

A variety of technical notes for the MachXO3 family are available on the Lattice web site.

- TN1282, [MachXO3 sysCLOCK PLL Design and Usage Guide](#)
- TN1281, [Implementing High-Speed Interfaces with MachXO3 Devices](#)
- TN1280, [MachXO3 sysIO Usage Guide](#)
- TN1279, [MachXO3 Programming and Configuration Usage Guide](#)
- TN1074, [PCB Layout Recommendations for BGA Packages](#)
- TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#)
- AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#)
- [MachXO3 Device Pinout Files](#)
- [Thermal Management](#) document
- [Lattice design tools](#)