E ·) (Fattice Semiconductor Corporation - LCMXO3LF-2100E-6MG324I Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	264
Number of Logic Elements/Cells	2112
Total RAM Bits	75776
Number of I/O	268
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	324-VFBGA
Supplier Device Package	324-CSFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-2100e-6mg324i

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MachXO3 Family Data Sheet Introduction

January 2016

Features

Solutions

- Smallest footprint, lowest power, high data throughput bridging solutions for mobile applications
- Optimized footprint, logic density, IO count, IO performance devices for IO management and logic applications
- High IO/logic, lowest cost/IO, high IO devices for IO expansion applications

■ Flexible Architecture

- Logic Density ranging from 640 to 9.4K LUT4
- High IO to LUT ratio with up to 384 IO pins

Advanced Packaging

- 0.4 mm pitch: 1K to 4K densities in very small footprint WLCSP (2.5 mm x 2.5 mm to 3.8 mm x 3.8 mm) with 28 to 63 IOs
- 0.5 mm pitch: 640 to 6.9K LUT densities in 6 mm x 6 mm to 10 mm x 10 mm BGA packages with up to 281 IOs
- 0.8 mm pitch: 1K to 9.4K densities with up to 384 IOs in BGA packages

Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRx2, DDRx4

High Performance, Flexible I/O Buffer

- Programmable sysIO[™] buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTL
 - LVDS, Bus-LVDS, MLVDS, LVPECL
 - MIPI D-PHY Emulated
 - Schmitt trigger inputs, up to 0.5 V hysteresis
- Ideal for IO bridging applications
- I/Os support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

■ Flexible On-Chip Clocking

- · Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
 - Wide input frequency range (7 MHz to 400 MHz)
- Non-volatile, Multi-time Programmable
 - Instant-on
 - Powers up in microseconds
 - · Optional dual boot with external SPI memory
 - Single-chip, secure solution
 - Programmable through JTAG, SPI or I²C
 - MachXO3L includes multi-time programmable NVCM
 - MachXO3LF infinitely reconfigurable Flash

 Supports background programming of non-volatile memory

TransFR Reconfiguration

In-field logic update while IO holds the system state

Enhanced System Level Support

- On-chip hardened functions: SPI, I²C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

Applications

- Consumer Electronics
- Compute and Storage
- Wireless Communications
- Industrial Control Systems
- Automotive System

Low Cost Migration Path

- Migration from the Flash based MachXO3LF to the NVCM based MachXO3L
- · Pin compatible and equivalent timing

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Advance Data Sheet DS1047



PFU Blocks

The core of the MachXO3L/LF device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Block Diagram



Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

	PFU Block			
Slice	Resources	Modes		
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM		
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM		

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.



ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

Routing

There are many resources provided in the MachXO3L/LF devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO3L/LF device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO3L/LF architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO3L/LF devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3L/LF devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3L/LF External Switching Characteristics table.

Primary clock signals for the MachXO3L/LF-1300 and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sys-CLOCK PLL outputs.



This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the $t_{I,OCK}$ parameter has been satisfied.

The MachXO3L/LF also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO3L/LF PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see TN1282, MachXO3 sysCLOCK PLL Design and Usage Guide.



Figure 2-7. PLL Diagram

Table 2-4 provides signal descriptions of the PLL block.

Table 2-4	. PLL	Signal	Descriptions
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Port Name	I/O	Description
CLKI	Ι	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	Ι	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	Ι	Dynamic Phase step – toggle shifts VCO phase adjust by one step.



Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-14 shows the output gearbox block diagram.



Table 2-11 shows the I/O standards (together with their supply and reference voltages) supported by the MachXO3L/LF devices. For further information on utilizing the sysIO buffer to support a variety of standards please see TN1280, MachXO3 sysIO Usage Guide.

Table 2-11. Supported Input Standards

	VCCIO (Typ.)					
Input Standard	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V	
Single-Ended Interfaces						
LVTTL	Yes					
LVCMOS33	Yes					
LVCMOS25		Yes				
LVCMOS18			Yes			
LVCMOS15				Yes		
LVCMOS12					Yes	
PCI	Yes					
Differential Interfaces						
LVDS	Yes	Yes				
BLVDS, MLVDS, LVPECL, RSDS	Yes	Yes				
MIPI ¹	Yes	Yes				
LVTTLD	Yes					
LVCMOS33D	Yes					
LVCMOS25D		Yes				
LVCMOS18D			Yes			

1. These interfaces can be emulated with external resistors in all devices.



Table 2-12. Supported Output Standards

Output Standard	V _{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	_
LVCMOS25, Open Drain	_
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	_
LVCMOS12, Open Drain	_
PCI33	3.3
Differential Interfaces	
LVDS ¹	2.5, 3.3
BLVDS, MLVDS, RSDS 1	2.5
LVPECL ¹	3.3
MIPI ¹	2.5
LVTTLD	3.3
LVCMOS33D	3.3
LVCMOS25D	2.5
LVCMOS18D	1.8

1. These interfaces can be emulated with external resistors in all devices.

sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO3L/LF-1300 in the 256 Ball packages and the MachXO3L/LF-2100 and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO3L/LF-1300 and lower density devices have four banks (one bank per side). Figures 2-15 and 2-16 show the sysIO banks and their associated supplies for all devices.



Embedded Hardened IP Functions

All MachXO3L/LF devices provide embedded hardened functions such as SPI, I²C and Timer/Counter. MachXO3LF devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-17.

Figure 2-17. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO3L/LF device contains two I^2C IP cores. These are the primary and secondary I^2C IP cores. Either of the two cores can be configured either as an I^2C master or as an I^2C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I^2C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I^2C Master. The I^2C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface



Figure 2-18. PC Core Block Diagram



Table 2-14 describes the signals interfacing with the I²C cores.

 Table 2-14. PC Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I ² C core. The signal is an output if the I ² C core is in master mode. The signal is an input if the I ² C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I ² C ports in each MachXO3L/LF device.
i2c_sda	Bi-directional	Bi-directional data line of the l^2C core. The signal is an output when data is transmitted from the l^2C core. The signal is an input when data is received into the l^2C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of l^2C ports in each MachXO3L/LF device.
i2c_irqo	Output	Interrupt request output signal of the I ² C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I ² C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO3L/LF device. The signal is enabled only if the "Wakeup Enable" feature has been set within the EFB GUI, I^2C Tab.

Hardened SPI IP Core

Every MachXO3L/LF device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it will be able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device will be able to interface to an external SPI master. The SPI IP core on MachXO3L/LF devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface



Hardened Timer/Counter

MachXO3L/LF devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bi-directional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
 - Watchdog timer
 - Clear timer on compare match
 - Fast PWM
 - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller.
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- · Stand-alone mode with preloaded control registers and direct reset input

Figure 2-20. Timer/Counter Block Diagram



Table 2-16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal will be detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	0	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	0	Timer counter output signal



TraceID

Each MachXO3L/LF device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I²C, or JTAG interfaces.

Density Shifting

The MachXO3L/LF family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO3 migration files.



DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
		Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)			+175	μΑ
		Clamp OFF and $V_{IN} = V_{CCIO}$	-10	—	10	μΑ
I _{IL} , I _{IH} ^{1, 4}	Input or I/O Leakage	Clamp OFF and V _{CCIO} - 0.97 V < V _{IN} < V _{CCIO}	-175	_	—	μA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} - 0.97 V	_		10	μΑ
		Clamp OFF and V _{IN} = GND	_		10	μΑ
		Clamp ON and 0 V < V_{IN} < V_{CCIO}			10	μΑ
I _{PU}	I/O Active Pull-up Current	0 < V _{IN} < 0.7 V _{CCIO}	-30		-309	μΑ
I _{PD}	I/O Active Pull-down Current	V _{IL} (MAX) < V _{IN} < V _{CCIO}	30	—	305	μA
I _{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I _{BHHS}	Bus Hold High sustaining current	V _{IN} = 0.7V _{CCIO}	-30	_	_	μΑ
I _{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	_	—	305	μΑ
І _{внно}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	_	_	-309	μΑ
V _{BHT} ³	Bus Hold Trip Points		V _{IL} (MAX)	—	V _{IH} (MIN)	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)$	3	5	9	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)$	3	5.5	7	pf
		V _{CCIO} = 3.3 V, Hysteresis = Large	_	450	—	mV
		V _{CCIO} = 2.5 V, Hysteresis = Large		250	—	mV
		V _{CCIO} = 1.8 V, Hysteresis = Large		125	—	mV
V	Hysteresis for Schmitt	V _{CCIO} = 1.5 V, Hysteresis = Large	_	100	_	mV
VHYST	Trigger Inputs⁵	V _{CCIO} = 3.3 V, Hysteresis = Small	_	250	_	mV
		V _{CCIO} = 2.5 V, Hysteresis = Small	_	150	_	mV
		V _{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	mV
		V _{CCIO} = 1.5 V, Hysteresis = Small	_	40	—	mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25 °C, f = 1.0 MHz.

3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.

 When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6mA can occur on the high-tolow transition. For true LVDS output pins in MachXO3L/LF devices, V_{IH} must be less than or equal to V_{CCIO}.

5. With bus keeper circuit turned on. For more details, refer to TN1280, MachXO3 sysIO Usage Guide.



sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP} , V _{INM}	Input Voltage	V _{CCIO} = 3.3 V	0	_	2.605	V
		V _{CCIO} = 2.5 V	0	_	2.05	V
V _{THD}	Differential Input Threshold		±100	_		mV
V	Input Common Mode Voltage	V _{CCIO} = 3.3 V	0.05	_	2.6	V
VCM	Input Common Mode Voltage	V _{CCIO} = 2.5 V	0.05	_	2.0	V
I _{IN}	Input current	Power on	_	_	±10	μA
V _{OH}	Output high voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.375	_	V
V _{OL}	Output low voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.90	1.025	_	V
V _{OD}	Output voltage differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} between high and low		_	_	50	mV
V _{OS}	Output voltage offset	(V _{OP} - V _{OM})/2, R _T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V _{OS} between H and L		—	—	50	mV
IOSD	Output short circuit current	V _{OD} = 0 V driver outputs shorted	_	_	24	mA

Over Recommended Operating Conditions



BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example



Table 3-2. BLVDS DC Conditions¹

Over Recommended	Operating	Conditions
	operating	Contaitions

		Noi		
Symbol	Description	Zo = 45	Zo = 90	Units
Z _{OUT}	Output impedance	20	20	Ohms
R _S	Driver series resistance	80	80	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.376	1.480	V
V _{OL}	Output low voltage	1.124	1.020	V
V _{OD}	Output differential voltage	0.253	0.459	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.



Typical Building Block Function Performance – C/E Devices¹

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	–6 Timing	Units
Basic Functions	•	
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

 The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.



MachXO3L/LF External Switching Characteristics – C/E Devices^{1, 2, 3, 4, 5, 6, 10}

			-6		_	5	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Units
Clocks							
Primary Clo	cks						-
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	All MachXO3L/LF devices	_	388	_	323	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO3L/LF devices	0.5		0.6		ns
		MachXO3L/LF-1300		867	_	897	ps
		MachXO3L/LF-2100		867		897	ps
t _{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO3L/LF-4300	_	865	_	892	ps
		MachXO3L/LF-6900	_	902	_	942	ps
		MachXO3L/LF-9400	_	908	_	950	ps
Edge Clock							
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	MachXO3L/LF		400	_	333	MHz
Pin-LUT-Pin	Propagation Delay						
t _{PD}	Best case propagation delay through one LUT-4	All MachXO3L/LF devices		6.72		6.96	ns
General I/O	Pin Parameters (Using Primary Clock with	out PLL)					
		MachXO3L/LF-1300	—	7.46	—	7.66	ns
		MachXO3L/LF-2100	_	7.46	_	7.66	ns
t _{CO}	Clock to Output - PIO Output Register	MachXO3L/LF-4300	_	7.51		7.71	ns
		MachXO3L/LF-6900	_	7.54		7.75	ns
		MachXO3L/LF-9400	_	7.53		7.83	ns
		MachXO3L/LF-1300	-0.20	_	-0.20		ns
	Clock to Data Setup - PIO Input Register	MachXO3L/LF-2100	-0.20	_	-0.20		ns
t _{SU}		MachXO3L/LF-4300	-0.23	_	-0.23		ns
		MachXO3L/LF-6900	-0.23		-0.23		ns
		MachXO3L/LF-9400	-0.24		-0.24		ns
		MachXO3L/LF-1300	1.89		2.13		ns
		MachXO3L/LF-2100	1.89	_	2.13		ns
t _H	Clock to Data Hold - PIO Input Register	MachXO3L/LF-4300	1.94	_	2.18		ns
		MachXO3L/LF-6900	1.98	_	2.23		ns
		MachXO3L/LF-9400	1.99	_	2.24		ns
		MachXO3L/LF-1300	1.61	_	1.76		ns
		MachXO3L/LF-2100	1.61	_	1.76		ns
t _{SU DEL}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-4300	1.66	_	1.81		ns
	with Data input Delay	MachXO3L/LF-6900	1.53	_	1.67		ns
		MachXO3L/LF-9400	1.65	_	1.80		ns
		MachXO3L/LF-1300	-0.23	_	-0.23		ns
		MachXO3L/LF-2100	-0.23	_	-0.23		ns
^t H DEL	Clock to Data Hold - PIO Input Register with	MachXO3L/LF-4300	-0.25	_	-0.25	_	ns
	Input Data Delay	MachXO3L/LF-6900	-0.21	_	-0.21	_	ns
		MachXO3L/LF-9400	-0.24	_	-0.24	_	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO3L/LF devices	—	388	—	323	MHz

Over Recommended Operating Conditions



DC and Switching Characteristics MachXO3 Family Data Sheet

		-6		-5			
Description	Device	Min.	Max.	Min.	Max.	Units	
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered ^{8, 9}							
Output Data Valid Before CLK Output	-	0.455		0.570		ns	
Output Data Valid After CLK Output		0.455	—	0.570	_	ns	
DDRX4 Serial Output Data Speed	MachXO3L/LF devices,	—	800	—	630	Mbps	
DDRX4 ECLK Frequency (minimum limited by PLL)	top side only	_	400	_	315	MHz	
SCLK Frequency	-		100		79	MHz	
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1 ^{8,9}							
Output Data Invalid Before CLK Output			0.160	_	0.180	ns	
Output Data Invalid After CLK Output			0.160		0.180	ns	
DDR71 Serial Output Data Speed	MachXO3L/LF devices,		756		630	Mbps	
DDR71 ECLK Frequency	top side only	_	378	—	315	MHz	
7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL)		_	108	_	90	MHz	
Outputs with Clock and Data Centered at P (.ECLK.Centered ^{10, 11, 12}	in Using PCLK Pin for Clo	ck Input	-				
Output Data Valid Before CLK Output		0.200	—	0.200	_	UI	
Output Data Valid After CLK Output		0.200	—	0.200	_	UI	
MIPI D-PHY Output Data Speed	All MachXO3L/LF devices, top side only	_	900	_	900	Mbps	
MIPI D-PHY ECLK Frequency (minimum limited by PLL)		_	450	_	450	MHz	
SCLK Frequency		—	112.5	—	112.5	MHz	
	Description RX4 Outputs with Clock and Data Centered CECLK.Centered ^{8, 9} Output Data Valid Before CLK Output Output Data Valid After CLK Output DDRX4 Serial Output Data Speed DDRX4 ECLK Frequency (minimum limited by PLL) SCLK Frequency ttputs – GDDR71_TX.ECLK.7:1 ^{8, 9} Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed DDR71 ECLK Frequency 7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL) Outputs with Clock and Data Centered at P C.ECLK.Centered ^{10, 11, 12} Output Data Valid Before CLK Output Output Data Valid After CLK Output MIPI D-PHY Output Data Speed MIPI D-PHY ECLK Frequency (minimum limited by PLL) SCLK Frequency	DescriptionDeviceRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for C.ECLK.Centered ^{8, 9} In Using PCLK Pin for C.ECLK.Centered ^{8, 9} Output Data Valid Before CLK OutputMachXO3L/LF devices, top side onlyDDRX4 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side onlySCLK FrequencyOutput Data Invalid Before CLK OutputOutput Data Invalid After CLK OutputMachXO3L/LF devices, top side onlyOutput Data Invalid After CLK OutputMachXO3L/LF devices, top side onlyDDR71 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDDR71 ECLK Frequency 7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL)MachXO3L/LF devices, top side onlyOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputAll MachXO3L/LF devices, top side onlyOutput Data Valid After CLK OutputAll MachXO3L/LF devices, top side onlyMIPI D-PHY Output Data SpeedAll MachXO3L/LF devices, top side onlyMIPI D-PHY ECLK Frequency (minimum limited by PLL)All MachXO3L/LF devices, top side onlySCLK FrequencyAll MachXO3L/LF devices, top side only	Description Device Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock (LECLK.Centered ^{8,9}) 0.455 Output Data Valid Before CLK Output 0.455 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only SCLK Frequency Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed MachXO3L/LF devices, top side only DDR71 ECLK Frequency Output Clock Frequency (SCLK) (minimum limited by PLL) Output Data Valid After CLK Output Output Data Valid Before CLK Output Output Data Valid After CLK Output 0.200 0.200 0.200 Output Data Valid After CLK Out	-6Min.Max.RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - CLECLK.Centered ^{8, 9} Output Data Valid Before CLK Output0.455Output Data Valid After CLK OutputMachXO3L/LF devices, top side only0.455DDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side only800SCLK Frequency (minimum limited by PLL)100400Output Data Invalid Before CLK Output0.160Output Data Invalid After CLK Output0.160DDR71 Serial Output Data Speed DDR71 Serial Output Data SpeedMachXO3L/LF devices, top side only108Output Swith Clock and Data Centered at Pin Using PCLK Pin for Clock Input - t.ECLK.Centered ^{10, 11, 12} 0.200Output Data Valid Before CLK Output DDR71 Serial Output Data SpeedAll MachXO3L/LF devices, top side only0.200Output Data Valid After CLK Output Mup PLL)All MachXO3L/LF devices, top side only0.200MIPI D-PHY Output Data Speed MIPI D-PHY CLK Frequency (minimum limited by PLL)All MachXO3L/LF devices, top side only450MIPI D-PHY ECLK Frequency (minimum limited by PLL)450450	Description Image: Description Image: Description Max. Min. Max. Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{8, 9} 0.455 - 0.570 Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only - 800 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 400 - SCLK Frequency - 0.160 -	Description Device Min. Max. Min. Max. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{9,9} 0.455 - 0.570 - Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 800 - 630 SCLK Frequency - 0.160 - 916 - 916 Output Data Invalid Before CLK Output MachXO3L/LF devices, top side only - 0.160 - 0.180 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 108 - 90 Output Data Valid After CLK Output MachXO3L/LF	

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

5. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.

6. The t_{SU DEL} and t_{H DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).

7. This number for general purpose usage. Duty cycle tolerance is +/-10%.

8. Duty cycle is $\pm -5\%$ for system usage.

9. Performance is calculated with 0.225 UI.

10. Performance is calculated with 0.20 UI.

11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.

12. Performance for Industrial devices and -5 devices are not modeled in the Diamond design tool.

13. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

14. Above 800 Mbps is only supported with WLCSP and csfBGA packages

15. Between 800 Mbps to 900 Mbps:

a. VIDTH exceeds the MIPI D-PHY Input DC Conditions Table 3-4 and can be calculated with the equation tSU or tH = -0.0005*VIDTH + 0.3284

b. Example calculations

i. tSU and tHO = 0.28 with VIDTH = 100 mV

ii. tSU and tHO = 0.25 with VIDTH = 170 mV

iii. tSU and tHO = 0.20 with VIDTH = 270 mV



NVCM/Flash Download Time^{1, 2}

Symbol	Parameter	Device	Тур.	Units
t _{REFRESH}	POR to Device I/O Active	LCMXO3L/LF-640	1.9	ms
		LCMXO3L/LF-1300	1.9	ms
		LCMXO3L/LF-1300 256-Ball Package	1.4	ms
		LCMXO3L/LF-2100	1.4	ms
		LCMXO3L/LF-2100 324-Ball Package	2.4	ms
		LCMXO3L/LF-4300	2.4	ms
		LCMXO3L/LF-4300 400-Ball Package	3.8	ms
		LCMXO3L/LF-6900	3.8	ms
		LCMXO3L/LF-9400C	5.2	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.



sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Mo	odes				
t _{PRGM}	PROGRAMN low p	ulse accept	55	_	ns
t _{PRGMJ}	PROGRAMN low p	ulse rejection	_	25	ns
t _{INITL}	INITN low time	LCMXO3L/LF-640/ LCMXO3L/LF-1300	—	55	us
		LCMXO3L/LF-1300 256-Ball Package/ LCMXO3L/LF-2100	_	70	us
		LCMXO3L/LF-2100 324-Ball Package/ LCMXO3-4300	_	105	us
		LCMXO3L/LF-4300 400-Ball Package/ LCMXO3-6900	_	130	us
LCMXO3L/LF-9		LCMXO3L/LF-9400C	_	175	us
t _{DPPINIT}	PROGRAMN low to	INITN low	_	150	ns
t _{DPPDONE}	PROGRAMN low to	PROGRAMN low to DONE low		150	ns
t _{IODISS}	PROGRAMN low to	o I/O disable	_	120	ns
Slave SPI					
f _{MAX}	CCLK clock frequer	CCLK clock frequency		66	MHz
t _{CCLKH}	CCLK clock pulse v	CCLK clock pulse width high		—	ns
t _{CCLKL}	CCLK clock pulse v	vidth low	7.5	_	ns
t _{STSU}	CCLK setup time		2	_	ns
t _{STH}	CCLK hold time		0	_	ns
t _{STCO}	CCLK falling edge t	to valid output	—	10	ns
t _{STOZ}	CCLK falling edge t	to valid disable	_	10	ns
t _{STOV}	CCLK falling edge t	to valid enable	_	10	ns
t _{SCS}	Chip select high tim	ne	25	—	ns
t _{SCSS}	Chip select setup ti	me	3	—	ns
t _{SCSH}	Chip select hold tim	ne	3	_	ns
Master SPI					
f _{MAX}	MCLK clock freque	ncy	—	133	MHz
t _{MCLKH}	MCLK clock pulse v	width high	3.75	—	ns
t _{MCLKL}	MCLK clock pulse v	width low	3.75	—	ns
t _{STSU}	MCLK setup time		5	—	ns
t _{STH}	MCLK hold time		1	—	ns
t _{CSSPI}	INITN high to chip s	select low	100	200	ns
t _{MCI K}	INITN high to first N	/ICLK edge	0.75	1	us



	MachXO3L/LF-6900				
	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank		•	•	•	•
Bank 0	50	73	50	71	83
Bank 1	52	68	52	68	84
Bank 2	52	72	52	72	84
Bank 3	16	24	16	24	28
Bank 4	16	16	16	16	24
Bank 5	20	28	20	28	32
Total General Purpose Single Ended IO	206	281	206	279	335
Differential IO per Bank		•	•	•	•
Bank 0	25	36	25	36	42
Bank 1	26	34	26	34	42
Bank 2	26	36	26	36	42
Bank 3	8	12	8	12	14
Bank 4	8	8	8	8	12
Bank 5	10	14	10	14	16
Total General Purpose Differential IO	103	140	103	140	168
Dual Function IO	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes		•	•		
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	21	20	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	21	20	21	21
High-speed Differential Outputs		•	•		
Bank 0	20	21	20	21	21
VCCIO Pins		•	•	•	•
Bank 0	4	4	4	4	5
Bank 1	3	4	4	4	5
Bank 2	4	4	4	4	5
Bank 3	2	2	1	2	2
Bank 4	2	2	2	2	2
Bank 5	2	2	1	2	2
VCC	8	8	8	10	10
GND	24	16	24	16	33
NC	0	0	1	0	0
Reserved for Configuration	1	1	1	1	1
Total Count of Bonded Pins	256	324	256	324	400