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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

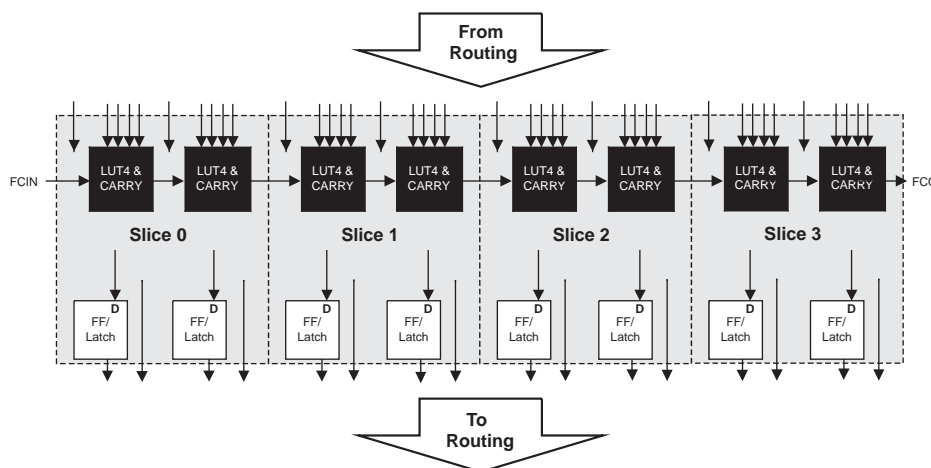
### Details

Product Status	Active
Number of LABs/CLBs	540
Number of Logic Elements/Cells	4320
Total RAM Bits	94208
Number of I/O	279
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-LFBGA
Supplier Device Package	324-CABGA (15x15)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-4300c-6bg324c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-4300c-6bg324c</a>

## PFU Blocks

The core of the MachXO3L/LF device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

**Figure 2-3. PFU Block Diagram**



## Slices

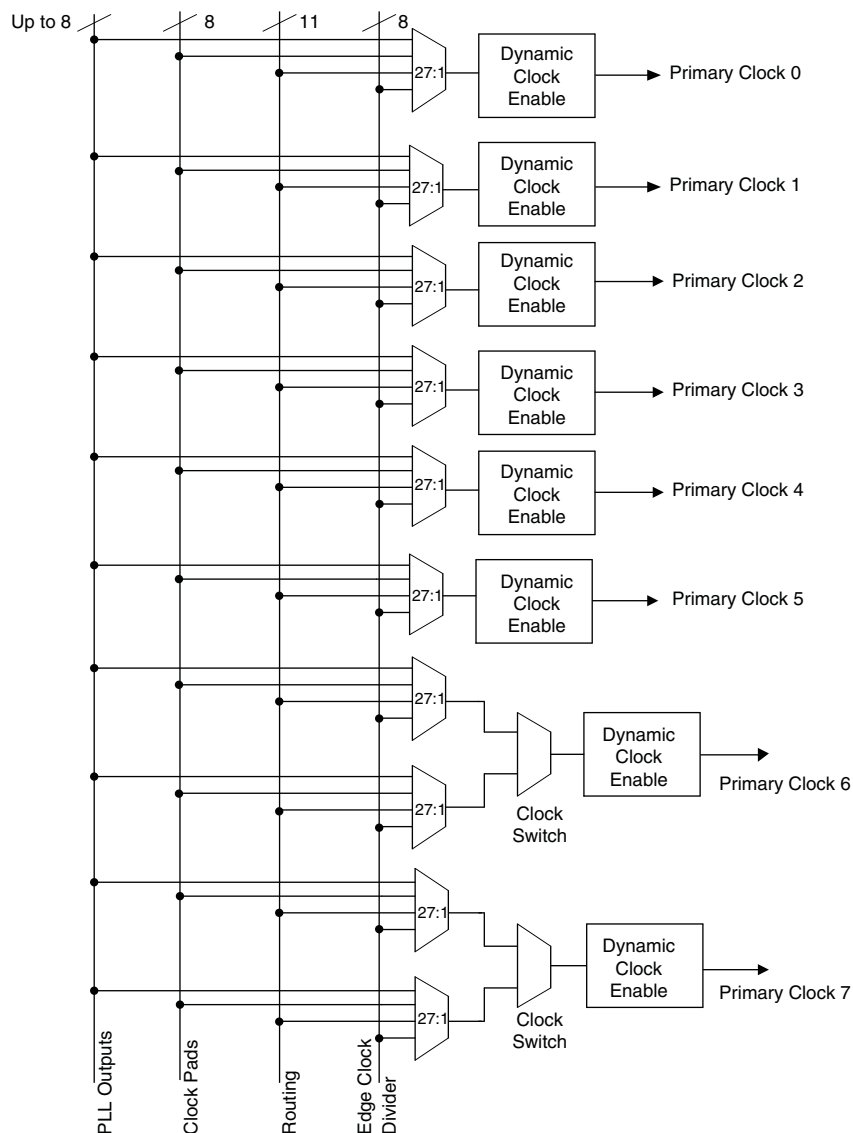
Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

**Table 2-1. Resources and Modes Available per Slice**

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

**Figure 2-5. Primary Clocks for MachXO3L/LF Devices**



Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2-6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO3L/LF External Switching Characteristics table.

**Table 2-4. PLL Signal Descriptions (Continued)**

Port Name	I/O	Description
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLIRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

## sysMEM Embedded Block RAM Memory

The MachXO3L/LF devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.



## PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

**Table 2-8. PIO Signal List**

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

### Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

#### Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

## Input Gearbox

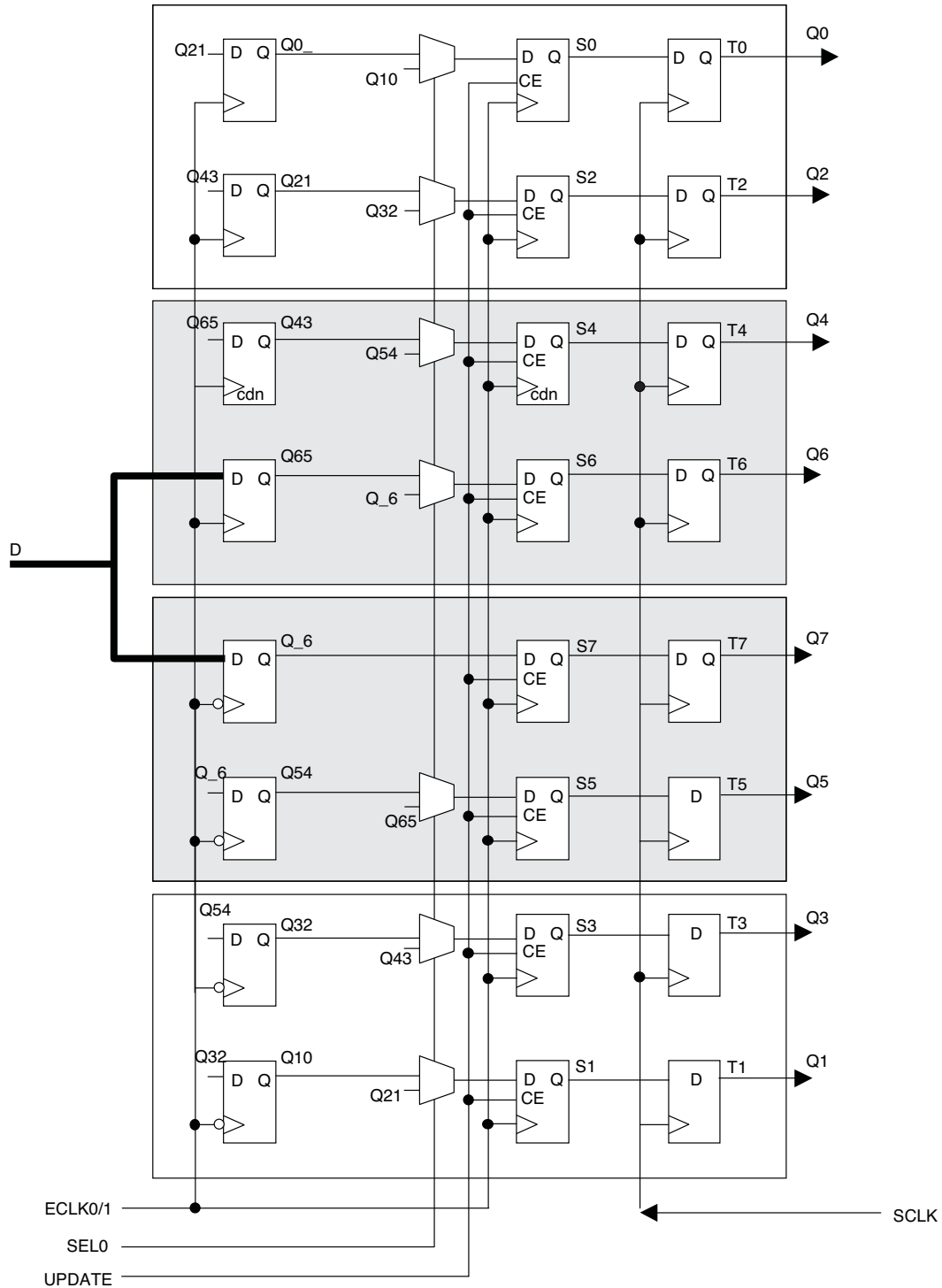
Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

**Table 2-9. Input Gearbox Signal List**

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-13 shows a block diagram of the input gearbox.

Figure 2-13. Input Gearbox



More information on the input gearbox is available in TN1281, [Implementing High-Speed Interfaces with MachXO3 Devices](#).



**Table 2-12. Supported Output Standards**

Output Standard	V <sub>CCIO</sub> (Typ.)
<b>Single-Ended Interfaces</b>	
LVTTL	3.3
LVC MOS33	3.3
LVC MOS25	2.5
LVC MOS18	1.8
LVC MOS15	1.5
LVC MOS12	1.2
LVC MOS33, Open Drain	—
LVC MOS25, Open Drain	—
LVC MOS18, Open Drain	—
LVC MOS15, Open Drain	—
LVC MOS12, Open Drain	—
PCI33	3.3
<b>Differential Interfaces</b>	
LVDS <sup>1</sup>	2.5, 3.3
BLVDS, MLVDS, RSDS <sup>1</sup>	2.5
LVPECL <sup>1</sup>	3.3
MIPI <sup>1</sup>	2.5
LVTTL D	3.3
LVC MOS33D	3.3
LVC MOS25D	2.5
LVC MOS18D	1.8

1. These interfaces can be emulated with external resistors in all devices.

## sysIO Buffer Banks

The numbers of banks vary between the devices of this family. MachXO3L/LF-1300 in the 256 Ball packages and the MachXO3L/LF-2100 and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The MachXO3L/LF-1300 and lower density devices have four banks (one bank per side). Figures 2-15 and 2-16 show the sysIO banks and their associated supplies for all devices.

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## Configuration and Testing

This section describes the configuration and testing features of the MachXO3L/LF family.

### IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO3L/LF devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with V<sub>CCIO</sub> Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see AN8066, [Boundary Scan Testability with Lattice sysIO Capability](#) and TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#).

### Device Configuration

All MachXO3L/LF devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I<sup>2</sup>C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO3L/LF device:

1. Internal NVCM/Flash Download
2. JTAG
3. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Standard I<sup>2</sup>C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally the device can run a CRC check upon entering the user mode. This will ensure that the device was configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/Os if they are not required for configuration. See TN1279, [MachXO3 Programming and Configuration Usage Guide](#) for more information about using the dual-use pins as general purpose I/Os.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO3L/LF devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip NVCM/Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip NVCM/Flash. For more details, refer to TN1279, [MachXO3 Programming and Configuration Usage Guide](#).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to TN1279, [MachXO3 Programming and Configuration Usage Guide](#).

### TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details refer to TN1087, [Minimizing System Interruption During Configuration Using TransFR Technology](#) for details.

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**Security and One-Time Programmable Mode (OTP)**

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO3L/LF devices contain security bits that, when set, prevent the readback of the SRAM configuration and NVCM/Flash spaces. The device can be in one of two modes:

1. Unlocked – Readback of the SRAM configuration and NVCM/Flash spaces is allowed.
2. Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the NVCM/Flash and SRAM OTP portions of the device. For more details, refer to TN1279, [MachXO3 Programming and Configuration Usage Guide](#).

**Password**

The MachXO3LF supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to TN1313, [Using Password Security with MachXO3 Devices](#).

**Dual Boot**

MachXO3L/LF devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip NVCM/Flash. For more details, refer to TN1279, [MachXO3 Programming and Configuration Usage Guide](#).

**Soft Error Detection**

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to TN1292, [MachXO3 Soft Error Detection Usage Guide](#).

**Soft Error Correction**

The MachXO3LF device supports Soft Error Correction (SEC). Optionally, the MachXO3L device can be ordered with a custom specification (c-spec) to support this feature. When BACKGROUND\_RECONFIG is enabled using the Lattice Diamond Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO3 can then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to TN1292, [MachXO3 Soft Error Detection \(SED\)/Correction \(SEC\) Usage Guide](#).

## TraceID

Each MachXO3L/LF device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I<sup>2</sup>C, or JTAG interfaces.

## Density Shifting

The MachXO3L/LF family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the [MachXO3 migration files](#).

**Table 3-5. MIPI D-PHY Output DC Conditions<sup>1</sup>**

	Description	Min.	Typ.	Max.	Units
<b>Transmitter</b>					
<b>External Termination</b>					
RL	1% external resistor with VCCIO = 2.5 V	—	50	—	Ohms
	1% external resistor with VCCIO = 3.3 V	—	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	—	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	—	464	—	Ohms
<b>High Speed</b>					
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	—	2.5	—	V
	VCCIO of the Bank with LVDS Emulated output buffer	—	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage	—	—	360	V
ZOS	Single ended output impedance	—	50	—	Ohms
ΔZOS	Single ended output impedance mismatch	—	—	10	%
<b>Low Power</b>					
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	—	1.2	—	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	–50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

<sup>1</sup>. Over Recommended Operating Conditions

## Typical Building Block Function Performance – C/E Devices<sup>1</sup>

### Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	Units
<b>Basic Functions</b>		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

### Register-to-Register Performance

Function	–6 Timing	Units
<b>Basic Functions</b>		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
<b>Embedded Memory Functions</b>		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
<b>Distributed Memory Functions</b>		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

## Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

### MachXO3L/LF External Switching Characteristics – C/E Devices<sup>1, 2, 3, 4, 5, 6, 10</sup>

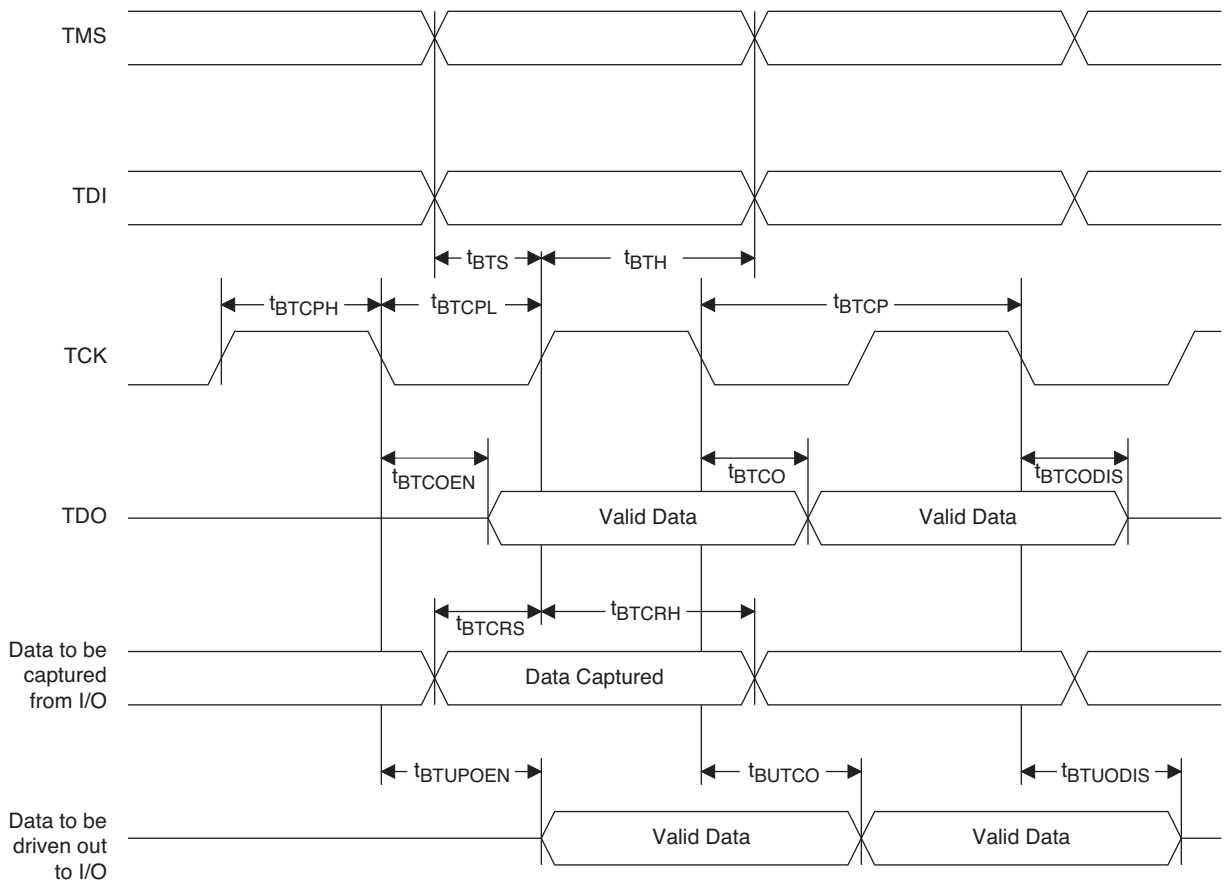
Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Clocks							
Primary Clocks							
f <sub>MAX_PRI</sub> <sup>7</sup>	Frequency for Primary Clock Tree	All MachXO3L/LF devices	—	388	—	323	MHz
t <sub>W_PRI</sub>	Clock Pulse Width for Primary Clock	All MachXO3L/LF devices	0.5	—	0.6	—	ns
t <sub>SKEW_PRI</sub>	Primary Clock Skew Within a Device	MachXO3L/LF-1300	—	867	—	897	ps
		MachXO3L/LF-2100	—	867	—	897	ps
		MachXO3L/LF-4300	—	865	—	892	ps
		MachXO3L/LF-6900	—	902	—	942	ps
		MachXO3L/LF-9400	—	908	—	950	ps
Edge Clock							
f <sub>MAX_EDGE</sub> <sup>7</sup>	Frequency for Edge Clock	MachXO3L/LF	—	400	—	333	MHz
Pin-LUT-Pin Propagation Delay							
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All MachXO3L/LF devices	—	6.72	—	6.96	ns
General I/O Pin Parameters (Using Primary Clock without PLL)							
t <sub>CO</sub>	Clock to Output - PIO Output Register	MachXO3L/LF-1300	—	7.46	—	7.66	ns
		MachXO3L/LF-2100	—	7.46	—	7.66	ns
		MachXO3L/LF-4300	—	7.51	—	7.71	ns
		MachXO3L/LF-6900	—	7.54	—	7.75	ns
		MachXO3L/LF-9400	—	7.53	—	7.83	ns
t <sub>SU</sub>	Clock to Data Setup - PIO Input Register	MachXO3L/LF-1300	–0.20	—	–0.20	—	ns
		MachXO3L/LF-2100	–0.20	—	–0.20	—	ns
		MachXO3L/LF-4300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-6900	–0.23	—	–0.23	—	ns
		MachXO3L/LF-9400	–0.24	—	–0.24	—	ns
t <sub>H</sub>	Clock to Data Hold - PIO Input Register	MachXO3L/LF-1300	1.89	—	2.13	—	ns
		MachXO3L/LF-2100	1.89	—	2.13	—	ns
		MachXO3L/LF-4300	1.94	—	2.18	—	ns
		MachXO3L/LF-6900	1.98	—	2.23	—	ns
		MachXO3L/LF-9400	1.99	—	2.24	—	ns
t <sub>SU_DEL</sub>	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	1.61	—	1.76	—	ns
		MachXO3L/LF-2100	1.61	—	1.76	—	ns
		MachXO3L/LF-4300	1.66	—	1.81	—	ns
		MachXO3L/LF-6900	1.53	—	1.67	—	ns
		MachXO3L/LF-9400	1.65	—	1.80	—	ns
t <sub>H_DEL</sub>	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-2100	–0.23	—	–0.23	—	ns
		MachXO3L/LF-4300	–0.25	—	–0.25	—	ns
		MachXO3L/LF-6900	–0.21	—	–0.21	—	ns
		MachXO3L/LF-9400	–0.24	—	–0.24	—	ns
f <sub>MAX_IO</sub>	Clock Frequency of I/O and PFU Register	All MachXO3L/LF devices	—	388	—	323	MHz

### JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
$f_{MAX}$	TCK clock frequency	—	25	MHz
$t_{BTCPH}$	TCK [BSCAN] clock pulse width high	20	—	ns
$t_{BTCPL}$	TCK [BSCAN] clock pulse width low	20	—	ns
$t_{BTS}$	TCK [BSCAN] setup time	10	—	ns
$t_{BTH}$	TCK [BSCAN] hold time	8	—	ns
$t_{BTCO}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
$t_{BTCOEN}$	TAP controller falling edge of clock to valid enable	—	10	ns
$t_{BTCRS}$	BSCAN test capture register setup time	8	—	ns
$t_{BTCRH}$	BSCAN test capture register hold time	20	—	ns
$t_{BUTCO}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

**Figure 3-8. JTAG Port Timing Waveforms**





## sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
<b>All Configuration Modes</b>					
t <sub>PRGM</sub>	PROGRAMN low pulse accept		55	—	ns
t <sub>PRGMJ</sub>	PROGRAMN low pulse rejection		—	25	ns
t <sub>INITL</sub>	INITN low time	LCMXO3L/LF-640/ LCMXO3L/LF-1300	—	55	us
		LCMXO3L/LF-1300 256-Ball Package/ LCMXO3L/LF-2100	—	70	us
		LCMXO3L/LF-2100 324-Ball Package/ LCMXO3-4300	—	105	us
		LCMXO3L/LF-4300 400-Ball Package/ LCMXO3-6900	—	130	us
		LCMXO3L/LF-9400C	—	175	us
t <sub>DPPINIT</sub>	PROGRAMN low to INITN low		—	150	ns
t <sub>DPPDONE</sub>	PROGRAMN low to DONE low		—	150	ns
t <sub>IODISS</sub>	PROGRAMN low to I/O disable		—	120	ns
<b>Slave SPI</b>					
f <sub>MAX</sub>	CCLK clock frequency		—	66	MHz
t <sub>CCLKH</sub>	CCLK clock pulse width high		7.5	—	ns
t <sub>CCLKL</sub>	CCLK clock pulse width low		7.5	—	ns
t <sub>STSU</sub>	CCLK setup time		2	—	ns
t <sub>STH</sub>	CCLK hold time		0	—	ns
t <sub>STCO</sub>	CCLK falling edge to valid output		—	10	ns
t <sub>STOZ</sub>	CCLK falling edge to valid disable		—	10	ns
t <sub>STOV</sub>	CCLK falling edge to valid enable		—	10	ns
t <sub>SCS</sub>	Chip select high time		25	—	ns
t <sub>SCSS</sub>	Chip select setup time		3	—	ns
t <sub>SCSH</sub>	Chip select hold time		3	—	ns
<b>Master SPI</b>					
f <sub>MAX</sub>	MCLK clock frequency		—	133	MHz
t <sub>MCLKH</sub>	MCLK clock pulse width high		3.75	—	ns
t <sub>MCLKL</sub>	MCLK clock pulse width low		3.75	—	ns
t <sub>STSU</sub>	MCLK setup time		5	—	ns
t <sub>STH</sub>	MCLK hold time		1	—	ns
t <sub>CSSPI</sub>	INITN high to chip select low		100	200	ns
t <sub>MCLK</sub>	INITN high to first MCLK edge		0.75	1	us

## Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions
<b>Configuration</b> (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I <sup>2</sup> C clock input and master I <sup>2</sup> C clock output.
SDA	I/O	Slave I <sup>2</sup> C data input and master I <sup>2</sup> C data output.

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3LF-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND

Date	Version	Section	Change Summary
June 2014	1.0	—	Product name/trademark adjustment.
		Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Changed fcCSP packages to csfBGA. Adjusted 121-ball csfBGA arrow.
			Introduction section general update.
		Architecture	General update.
		DC and Switching Characteristics	Updated sysIO Recommended Operating Conditions section. Removed $V_{REF}$ (V) column. Added standards.
			Updated Maximum sysIO Buffer Performance section. Added MIPI I/O standard.
			Updated MIPI D-PHY Emulation section. Changed Low Speed to Low Power. Updated Table 3-4, MIPI DC Conditions.
			Updated Table 3-5, MIPI D-PHY Output DC Conditions.
			Updated Maximum sysIO Buffer Performance section.
			Updated MachXO3L External Switching Characteristics – C/E Device section.
May 2014	00.3	Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Moved 121-ball fcCSP arrow.
			General update of Introduction section.
		Architecture	General update.
		Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
		Ordering Information	Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
			Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers.
February 2014	00.2	DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.
	00.1	—	Initial release.