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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	65536
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	121-VFBGA, CSPBGA
Supplier Device Package	121-CSFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-640e-6mg121c

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MachXO3 Family Data Sheet Introduction

January 2016

Features

Solutions

- Smallest footprint, lowest power, high data throughput bridging solutions for mobile applications
- Optimized footprint, logic density, IO count, IO performance devices for IO management and logic applications
- High IO/logic, lowest cost/IO, high IO devices for IO expansion applications

■ Flexible Architecture

- Logic Density ranging from 640 to 9.4K LUT4
- High IO to LUT ratio with up to 384 IO pins

Advanced Packaging

- 0.4 mm pitch: 1K to 4K densities in very small footprint WLCSP (2.5 mm x 2.5 mm to 3.8 mm x 3.8 mm) with 28 to 63 IOs
- 0.5 mm pitch: 640 to 6.9K LUT densities in 6 mm x 6 mm to 10 mm x 10 mm BGA packages with up to 281 IOs
- 0.8 mm pitch: 1K to 9.4K densities with up to 384 IOs in BGA packages

Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRx2, DDRx4

High Performance, Flexible I/O Buffer

- Programmable sysIO[™] buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTL
 - LVDS, Bus-LVDS, MLVDS, LVPECL
 - MIPI D-PHY Emulated
 - Schmitt trigger inputs, up to 0.5 V hysteresis
- Ideal for IO bridging applications
- I/Os support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

■ Flexible On-Chip Clocking

- · Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
 - Wide input frequency range (7 MHz to 400 MHz)
- Non-volatile, Multi-time Programmable
 - Instant-on
 - Powers up in microseconds
 - · Optional dual boot with external SPI memory
 - Single-chip, secure solution
 - Programmable through JTAG, SPI or I²C
 - MachXO3L includes multi-time programmable NVCM
 - MachXO3LF infinitely reconfigurable Flash

 Supports background programming of non-volatile memory

■ TransFR Reconfiguration

In-field logic update while IO holds the system state

Enhanced System Level Support

- On-chip hardened functions: SPI, I²C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

Applications

- Consumer Electronics
- Compute and Storage
- Wireless Communications
- Industrial Control Systems
- Automotive System

Low Cost Migration Path

- Migration from the Flash based MachXO3LF to the NVCM based MachXO3L
- · Pin compatible and equivalent timing

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Advance Data Sheet DS1047







 MachXO3L/LF-1300, MachXO3L/LF-2100, MachXO3L/LF-6900 and MachXO3L/LF-9400 are similar to MachXO3L/LF-4300. MachXO3L/LF-1300 has a lower LUT count, one PLL, and seven EBR blocks. MachXO3L/LF-2100 has a lower LUT count, one PLL, and eight EBR blocks. MachXO3L/LF-6900 has a higher LUT count, two PLLs, and 26 EBR blocks. MachXO3L/LF-9400 has a higher LUT count, two PLLs, and 48 EBR blocks.

• MachXO3L devices have NVCM, MachXO3LF devices have Flash.

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO3L/LF family, the number of sysIO banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT usage.

The MachXO3L/LF registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

The MachXO3L/LF architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. These blocks are located at the ends of the on-chip NVCM/Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO3L/LF devices provide commonly used hardened functions such as SPI controller, I²C controller and timer/ counter.

MachXO3LF devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I²C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO3L/LF devices are available for operation from 3.3 V, 2.5 V and 1.2 V power sup-plies, providing easy integration into the overall system.



Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	0	Primary PLL output clock (with phase shift adjustment)
CLKOS	0	Secondary PLL output clock (with phase shift adjust)
CLKOS2	0	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	0	Secondary PLL output clock3 (with phase shift adjust)
LOCK	0	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed- back signals.
DPHSRC	0	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	0	PLL data bus data output
PLLACK	0	PLL data bus acknowledge signal

sysMEM Embedded Block RAM Memory

The MachXO3L/LF devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.



Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that will then feed the output.

Figure 2-12 shows the output register block on the left, top and bottom edges.

Figure 2-12. MachXO3L/LF Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)



Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.



Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-13 shows a block diagram of the input gearbox.



Figure 2-13. Input Gearbox



More information on the input gearbox is available in TN1281, Implementing High-Speed Interfaces with MachXO3 Devices.



Figure 2-15. MachXO3L/LF-1300 in 256 Ball Packages, MachXO3L/LF-2100, MachXO3L/LF-4300, MachXO3L/LF-6900 and MachXO3L/LF-9400 Banks



Figure 2-16. MachXO3L/LF-640 and MachXO3L/LF-1300 Banks





Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-13 lists all the available MCLK frequencies.

Table 2-13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133



Embedded Hardened IP Functions

All MachXO3L/LF devices provide embedded hardened functions such as SPI, I²C and Timer/Counter. MachXO3LF devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-17.

Figure 2-17. Embedded Function Block Interface



Hardened I²C IP Core

Every MachXO3L/LF device contains two I^2C IP cores. These are the primary and secondary I^2C IP cores. Either of the two cores can be configured either as an I^2C master or as an I^2C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the I^2C bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I^2C Master. The I^2C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface



For more details on these embedded functions, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

User Flash Memory (UFM)

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

Standby Mode and Power Saving Options

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} while the E devices operate at 1.2 V V_{CC}.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I²C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned "off" or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.



TraceID

Each MachXO3L/LF device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I²C, or JTAG interfaces.

Density Shifting

The MachXO3L/LF family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO3 migration files.



sysIO Recommended Operating Conditions

	V _{CCIO} (V)				V _{REF} (V)	
Standard	Min.	Тур.	Max.	Min.	Тур.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—
LVDS33 ^{1, 2}	3.135	3.3	3.465	—	—	—
LVPECL ¹	3.135	3.3	3.465	—	—	—
BLVDS ¹	2.375	2.5	2.625	—	—	—
MIPI ³	2.375	2.5	2.625	—	—	—
MIPI_LP ³	1.14	1.2	1.26	—	—	—
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R334	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R254	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33 ⁴	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25 ^₄	2.375	2.5	2.625	0.35	0.5	0.65

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. For the dedicated LVDS buffers.

3. Requires the addition of external resistors.

4. Supported only for inputs and BIDIs for -6 speed grade devices.



sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO3L/LF PLD family.

LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V V	Input Voltage	V _{CCIO} = 3.3 V	0	_	2.605	V
VINP VINM		V _{CCIO} = 2.5 V	0	_	2.05	V
V _{THD}	Differential Input Threshold		±100	_		mV
V	Input Common Mode Voltage	V _{CCIO} = 3.3 V	0.05	_	2.6	V
V _{CM} Input Commo	Input Common Mode Voltage	V _{CCIO} = 2.5 V	0.05	_	2.0	V
I _{IN}	Input current	Power on	_	_	±10	μA
V _{OH}	Output high voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	_	1.375	_	V
V _{OL}	Output low voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.90	1.025	_	V
V _{OD}	Output voltage differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} between high and low		_	_	50	mV
V _{OS}	Output voltage offset	(V _{OP} - V _{OM})/2, R _T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V _{OS} between H and L		—	—	50	mV
IOSD	Output short circuit current	V _{OD} = 0 V driver outputs shorted	_	_	24	mA

Over Recommended Operating Conditions



BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example



Table 3-2. BLVDS DC Conditions¹

Over Recommended	Operating	Conditions
	operating	oonantions

		Noi	ninal	
Symbol	Description	Zo = 45	Zo = 90	Units
Z _{OUT}	Output impedance	20	20	Ohms
R _S	Driver series resistance	esistance 80 80		Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.376	1.480	V
V _{OL}	Output low voltage	1.124	1.020	V
V _{OD}	Output differential voltage	0.253	0.459	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.



	Description	Min.	Тур.	Max.	Units
Low Power	· · ·				
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer		1.2		V
VIH	Logic 1 input voltage	—	—	0.88	V
VIL	Logic 0 input voltage, not in ULP State	0.55	—	—	V
VHYST	Input hysteresis	25	—	—	mV

1. Over Recommended Operating Conditions

Figure 3-5. MIPI D-PHY Output Using External Resistors





DC and Switching Characteristics MachXO3 Family Data Sheet

		-6		-5			
Description	Min.	Max.	Min.	Max.	Units		
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered ^{8, 9}							
Output Data Valid Before CLK Output		0.455	_	0.570	_	ns	
Output Data Valid After CLK Output		0.455	—	0.570	_	ns	
DDRX4 Serial Output Data Speed	MachXO3L/LF devices,	—	800	—	630	Mbps	
DDRX4 ECLK Frequency (minimum limited by PLL)	top side only	_	400	_	315	MHz	
SCLK Frequency	-		100		79	MHz	
Itputs – GDDR71_TX.ECLK.7:1 ^{8, 9}							
Output Data Invalid Before CLK Output			0.160	_	0.180	ns	
Output Data Invalid After CLK Output			0.160		0.180	ns	
DDR71 Serial Output Data Speed	MachXO3L/LF devices,		756		630	Mbps	
DDR71 ECLK Frequency	top side only	_	378	—	315	MHz	
7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL)		_	108	_	90	MHz	
Outputs with Clock and Data Centered at P (.ECLK.Centered ^{10, 11, 12}	in Using PCLK Pin for Clo	ck Input	-				
Output Data Valid Before CLK Output		0.200	—	0.200	_	UI	
Output Data Valid After CLK Output		0.200	_	0.200	_	UI	
MIPI D-PHY Output Data Speed	All MachXO3L/LF	_	900	—	900	Mbps	
MIPI D-PHY ECLK Frequency (minimum limited by PLL)	devices, top side only	_	450	_	450	MHz	
SCLK Frequency	<u> </u>	—	112.5	—	112.5	MHz	
	Description RX4 Outputs with Clock and Data Centered CECLK.Centered ^{8, 9} Output Data Valid Before CLK Output Output Data Valid After CLK Output DDRX4 Serial Output Data Speed DDRX4 ECLK Frequency (minimum limited by PLL) SCLK Frequency ttputs – GDDR71_TX.ECLK.7:1 ^{8, 9} Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed DDR71 ECLK Frequency 7:1 Output Clock Frequency (SCLK) (mini- mum limited by PLL) Outputs with Clock and Data Centered at P C.ECLK.Centered ^{10, 11, 12} Output Data Valid Before CLK Output Output Data Valid After CLK Output MIPI D-PHY Output Data Speed MIPI D-PHY ECLK Frequency (minimum limited by PLL) SCLK Frequency	DescriptionDeviceRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for C.ECLK.Centered ^{8, 9} In Using PCLK Pin for C.ECLK.Centered ^{8, 9} Output Data Valid Before CLK OutputMachXO3L/LF devices, top side onlyDDRX4 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side onlySCLK FrequencyOutput Data Invalid Before CLK OutputOutput Data Invalid Before CLK OutputMachXO3L/LF devices, top side onlyOutput Data Invalid After CLK OutputMachXO3L/LF devices, top side onlyDDR71 Serial Output Data SpeedMachXO3L/LF devices, top side onlyDT71 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side onlyOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputOutput Data Valid Before CLK OutputMachXO3L/LF devices, top side onlyOutput Data Valid Before CLK OutputAll MachXO3L/LFOutput Data Valid After CLK OutputAll MachXO3L/LFMIPI D-PHY Output Data SpeedAll MachXO3L/LFMIPI D-PHY ECLK Frequency (minimum limited by PLL)All MachXO3L/LFSCLK FrequencyAll MachXO3L/LF	Description Device Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock (LECLK.Centered ^{8,9}) 0.455 Output Data Valid Before CLK Output 0.455 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only SCLK Frequency Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid Before CLK Output Output Data Invalid After CLK Output DDR71 Serial Output Data Speed MachXO3L/LF devices, top side only DDR71 ECLK Frequency 7:1 Output Clock Frequency (SCLK) (minimum limited by PLL) Output Data Valid After CLK Output Output Data Valid After CLK Output Output Data Valid After CLK Output 0.200 0.200 0.200 Output Data Valid After CLK	-6Min.Max.RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - CLECLK.Centered ^{8, 9} Output Data Valid Before CLK Output0.455Output Data Valid After CLK OutputMachXO3L/LF devices, top side only0.455DDRX4 ECLK Frequency (minimum limited by PLL)MachXO3L/LF devices, top side only800SCLK Frequency (minimum limited by PLL)100400Output Data Invalid Before CLK Output0.160Output Data Invalid After CLK Output0.160DDR71 Serial Output Data Speed DDR71 Serial Output Data SpeedMachXO3L/LF devices, top side only108Output Swith Clock and Data Centered at Pin Using PCLK Pin for Clock Input - t.ECLK.Centered ^{10, 11, 12} 0.200Output Data Valid Before CLK Output DDR71 Serial Output Data SpeedAll MachXO3L/LF devices, top side only0.200Output Data Valid After CLK Output Mup PLL)All MachXO3L/LF devices, top side only0.200MIPI D-PHY Output Data Speed MIPI D-PHY CLK Frequency (minimum limited by PLL)All MachXO3L/LF devices, top side only450MIPI D-PHY ECLK Frequency (minimum limited by PLL)450450	Description Image: Description Image: Description Max. Min. Max. Min. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{8, 9} 0.455 - 0.570 Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only - 800 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 400 - SCLK Frequency - 0.160 -	Description Device Min. Max. Min. Max. RX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - LECLK.Centered ^{9,9} 0.455 - 0.570 - Output Data Valid Before CLK Output MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 Serial Output Data Speed MachXO3L/LF devices, top side only 0.455 - 0.570 - DDRX4 ECLK Frequency (minimum limited by PLL) MachXO3L/LF devices, top side only - 800 - 630 SCLK Frequency - 0.160 - 916 - 916 Output Data Invalid Before CLK Output MachXO3L/LF devices, top side only - 0.160 - 0.180 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 756 - 630 DDR71 ECLK Frequency MachXO3L/LF devices, top side only - 108 - 90 Output Data Valid After CLK Output MachXO3L/LF	

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Diamond software.

2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.

3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).

4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).

5. For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.

6. The t_{SU DEL} and t_{H DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps (-6), 113 ps (-5), 120 ps (-4).

7. This number for general purpose usage. Duty cycle tolerance is +/-10%.

8. Duty cycle is $\pm -5\%$ for system usage.

9. Performance is calculated with 0.225 UI.

10. Performance is calculated with 0.20 UI.

11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.

12. Performance for Industrial devices and -5 devices are not modeled in the Diamond design tool.

13. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with the device selected.

14. Above 800 Mbps is only supported with WLCSP and csfBGA packages

15. Between 800 Mbps to 900 Mbps:

a. VIDTH exceeds the MIPI D-PHY Input DC Conditions Table 3-4 and can be calculated with the equation tSU or tH = -0.0005*VIDTH + 0.3284

b. Example calculations

i. tSU and tHO = 0.28 with VIDTH = 100 mV

ii. tSU and tHO = 0.25 with VIDTH = 170 mV

iii. tSU and tHO = 0.20 with VIDTH = 270 mV



NVCM/Flash Download Time^{1, 2}

Symbol	Parameter	Device	Тур.	Units
t _{REFRESH}	POR to Device I/O Active	LCMXO3L/LF-640	1.9	ms
		LCMXO3L/LF-1300	1.9	ms
		LCMXO3L/LF-1300 256-Ball Package	1.4	ms
		LCMXO3L/LF-2100	1.4	ms
		LCMXO3L/LF-2100 324-Ball Package	2.4	ms
		LCMXO3L/LF-4300	2.4	ms
		LCMXO3L/LF-4300 400-Ball Package	3.8	ms
		LCMXO3L/LF-6900	3.8	ms
		LCMXO3L/LF-9400C	5.2	ms

1. Assumes sysMEM EBR initialized to an all zero pattern if they are used.

2. The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.



Signal Descriptions (Cont.)

Signal Name	I/O	Descriptions			
Configuration (Dual fu	Configuration (Dual function pins used during sysCONFIG)				
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.			
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.			
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.			
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.			
SN	I	Slave SPI active low chip select input.			
CSSPIN	I/O	Master SPI active low chip select output.			
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.			
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.			
SCL	I/O	Slave I ² C clock input and master I ² C clock output.			
SDA	I/O	Slave I ² C data input and master I ² C data output.			



	MachXO3L/LF-6900							
	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400			
General Purpose IO per Bank								
Bank 0	50	73	50	71	83			
Bank 1	52	68	52	68	84			
Bank 2	52	72	52	72	84			
Bank 3	16	24	16	24	28			
Bank 4	16	16	16	16	24			
Bank 5	20	28	20	28 3				
Total General Purpose Single Ended IO	206	281	206	279	335			
Differential IO per Bank								
Bank 0	25	36	25	36	42			
Bank 1	26	34	26	34	42			
Bank 2	26	36	26	36	42			
Bank 3	8	12	8	12	14			
Bank 4	8	8	8	8	12			
Bank 5	10	14	10	14	16			
Total General Purpose Differential IO	103	140	103	140	168			
Dual Function IO	37	37	37	37	37			
Number 7:1 or 8:1 Gearboxes								
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	21	20	21	21			
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	21	20	21	21			
High-speed Differential Outputs								
Bank 0	20	21	20	21	21			
VCCIO Pins		•	•		•			
Bank 0	4	4	4	4	5			
Bank 1	3	4	4	4	5			
Bank 2	4	4	4	4	5			
Bank 3	2	2	1	2	2			
Bank 4	2	2	2	2	2			
Bank 5	2	2	1	2	2			
VCC	8	8	8	10	10			
GND	24	16	24	16	33			
NC	0	0	1	0	0			
Reserved for Configuration	1	1	1	1	1			
Total Count of Bonded Pins	256	324	256	324	400			



Date	Version	Section	Change Summary		
September 2015	1.5	DC and Switching Characteristics	Updated the MIPI D-PHY Emulation section. Revised Table 3-5, MIPI D- PHY Output DC Conditions. — Revised RL Typ. value. — Revised RH description and values.		
			Updated the Maximum sysIO Buffer Performance section. Revised MIPI Max. Speed value.		
			Updated the MachXO3L/LF External Switching Characteristics – C/E Devices section. Added footnotes 14 and 15.		
August 2015	1.4	Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.		
		Ordering Information	Updated the top side markings section to indicate the use of LMXO3LF for the LCMXO3LF device.		
March 2015	1.3	All	General update. Added MachXO3LF devices.		
October 2014	1.2	Introduction	Updated Table 1-1, MachXO3L Family Selection Guide. Revised XO3L- 2100 and XO3L-4300 IO for 324-ball csfBGA package.		
		Architecture	Updated the Dual Boot section. Corrected information on where the pri- mary bitstream and the golden image must reside.		
		Pinout Information	Updated the Pin Information Summary section.		
			Changed General Purpose IO Bank 5 values for MachXO3L-2100 and MachXO3L-4300 CSFBGA 324 package.		
			Changed Number 7:1 or 8:1 Gearboxes for MachXO3L-640 and MachXO3L-1300.		
			Removed DQS Groups (Bank 1) section.		
			Changed VCCIO Pins Bank 1 values for MachXO3L-1300, MachXO3L- 2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.		
			Changed GND values for MachXO3L-1300, MachXO3L-2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.		
			Changed NC values for MachXO3L-2100 and MachXO3L-4300 CSF- BGA 324 package.		
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.		
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.		
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.		
July 2014	1.1	DC and Switching Characteristics	Updated the Static Supply Current – C/E Devices section. Added devices.		
			Updated the Programming and Erase Supply Current – C/E Device section. Added devices.		
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Revised footnote 4.		
			Added the NVCM Download Time section.		
			Updated the Typical Building Block Function Performance – C/E Devices section. Added information to footnote.		
		Pinout Information	Updated the Pin Information Summary section.		
		Ordering Information	Updated the MachXO3L Part Number Description section. Added packages.		
			Updated the Ordering Information section. General update.		