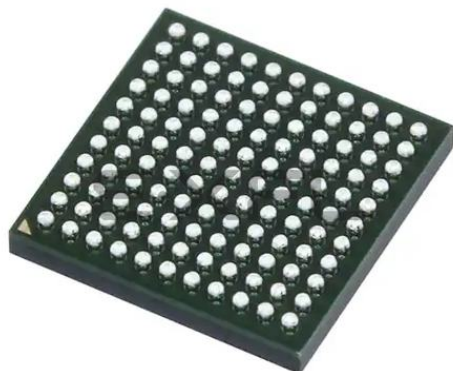




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	65536
Number of I/O	100
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	121-VFBGA, CSPBGA
Supplier Device Package	121-CSFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmx03lf-640e-6mg121i

Table 1-1. MachXO3L/LF Family Selection Guide

Features		MachXO3L-640/ MachXO3LF-640	MachXO3L-1300/ MachXO3LF-1300	MachXO3L-2100/ MachXO3LF-2100	MachXO3L-4300/ MachXO3LF-4300	MachXO3L-6900/ MachXO3LF-6900	MachXO3L-9400/ MachXO3LF-9400
LUTs		640	1300	2100	4300	6900	9400
Distributed RAM (kbits)		5	10	16	34	54	73
EBR SRAM (kbits)		64	64	74	92	240	432
Number of PLLs		1	1	1	2	2	2
Hardened Functions:	I ² C	2	2	2	2	2	2
	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY Support		Yes	Yes	Yes	Yes	Yes	Yes
Multi Time Programmable NVCM		MachXO3L-640	MachXO3L-1300	MachXO3L-2100	MachXO3L-4300	MachXO3L-6900	MachXO3L-9400
Programmable Flash		MachXO3LF-640	MachXO3LF-1300	MachXO3LF-2100	MachXO3LF-4300	MachXO3LF-6900	MachXO3LF-9400
Packages		IO					
36-ball WLCSP ¹ (2.5 mm x 2.5 mm, 0.4 mm)			28				
49-ball WLCSP ¹ (3.2 mm x 3.2 mm, 0.4 mm)				38			
81-ball WLCSP ¹ (3.8 mm x 3.8 mm, 0.4 mm)					63		
121-ball csfBGA ¹ (6 mm x 6 mm, 0.5 mm)		100	100	100	100		
256-ball csfBGA ¹ (9 mm x 9 mm, 0.5 mm)			206	206	206	206	206
324-ball csfBGA ¹ (10 mm x 10 mm, 0.5 mm)				268	268	281	
256-ball caBGA ² (14 mm x 14 mm, 0.8 mm)			206	206	206	206	206
324-ball caBGA ² (15 mm x 15 mm, 0.8 mm)				279	279	279	
400-ball caBGA ² (17 mm x 17 mm, 0.8 mm)					335	335	335
484-ball caBGA ² (19 mm x 19 mm, 0.8 mm)							384

1. Package is only available for E=1.2 V devices.

2. Package is only available for C=2.5 V/3.3 V devices.

Introduction

MachXO3™ device family is an Ultra-Low Density family that supports the most advanced programmable bridging and IO expansion. It has the breakthrough IO density and the lowest cost per IO. The device IO features have the integrated support for latest industry standard IO.

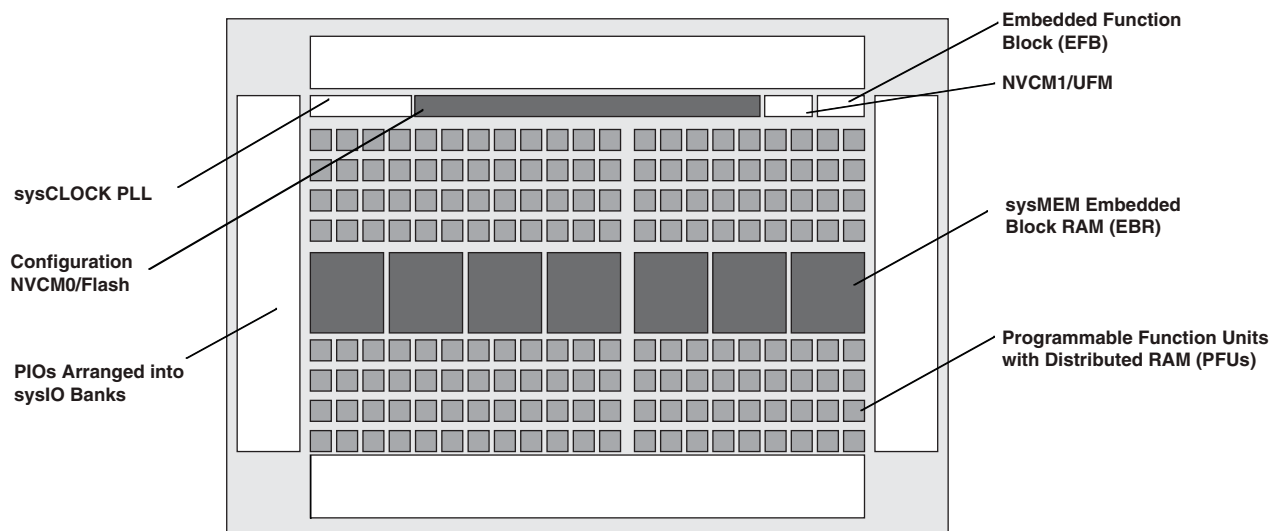
The MachXO3L/LF family of low power, instant-on, non-volatile PLDs has five devices with densities ranging from 640 to 9400 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I²C controller and timer/counter. MachXO3LF devices also support User Flash Memory (UFM). These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO3L/LF devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs

Architecture Overview

The MachXO3L/LF family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2-1 and Figure 2-2 show the block diagrams of the various family members.

Figure 2-1. Top View of the MachXO3L/LF-1300 Device



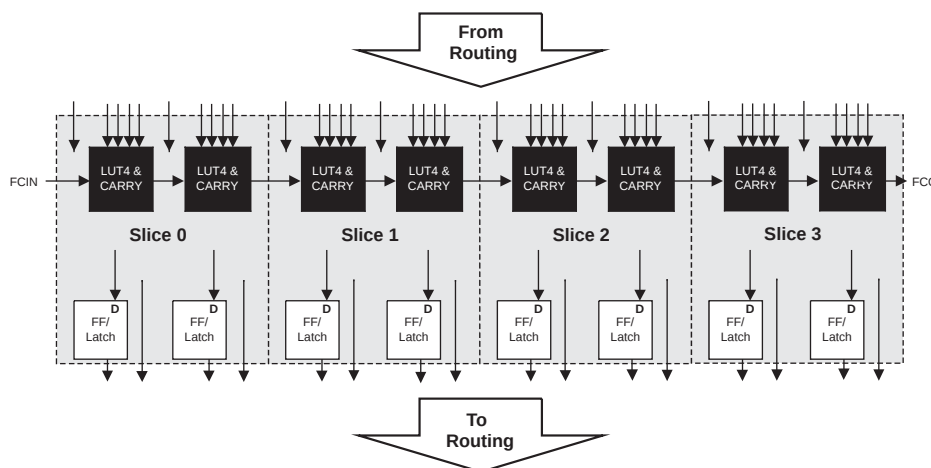
Notes:

- MachXO3L/LF-640 is similar to MachXO3L/LF-1300. MachXO3L/LF-640 has a lower LUT count.
- MachXO3L devices have NVCM, MachXO3LF devices have Flash.

PFU Blocks

The core of the MachXO3L/LF device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2-3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Block Diagram



Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2-1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2-2 lists the signals associated with Slices 0-3.

ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1290, [Memory Usage Guide for MachXO3 Devices](#).

Routing

There are many resources provided in the MachXO3L/LF devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Each MachXO3L/LF device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

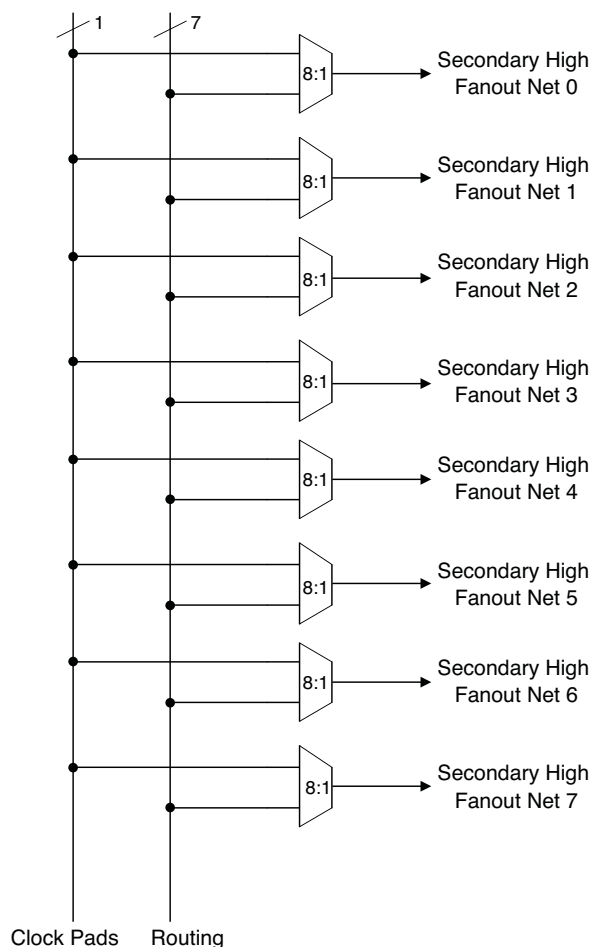
The MachXO3L/LF architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO3L/LF devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3L/LF devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3L/LF External Switching Characteristics table.

Primary clock signals for the MachXO3L/LF-1300 and larger devices are generated from eight 27:1 muxes. The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sys-CLOCK PLL outputs.

Figure 2-6. Secondary High Fanout Nets for MachXO3L/LF Devices



sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO3L/LF devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO3L/LF sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, please see TN1282, [MachXO3 sysCLOCK PLL Design and Usage Guide](#).

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO3L/LF clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-7.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock.

Table 2-6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE ¹	Output Clock Enable	Active High
RST	Reset	Active High
BE ¹	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

1. Optional signals.
2. For dual port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – When new data is being written, the old contents of the address appears at the output.

FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2-7 shows the range of programming values for these flags.

Table 2-7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset

Input Gearbox

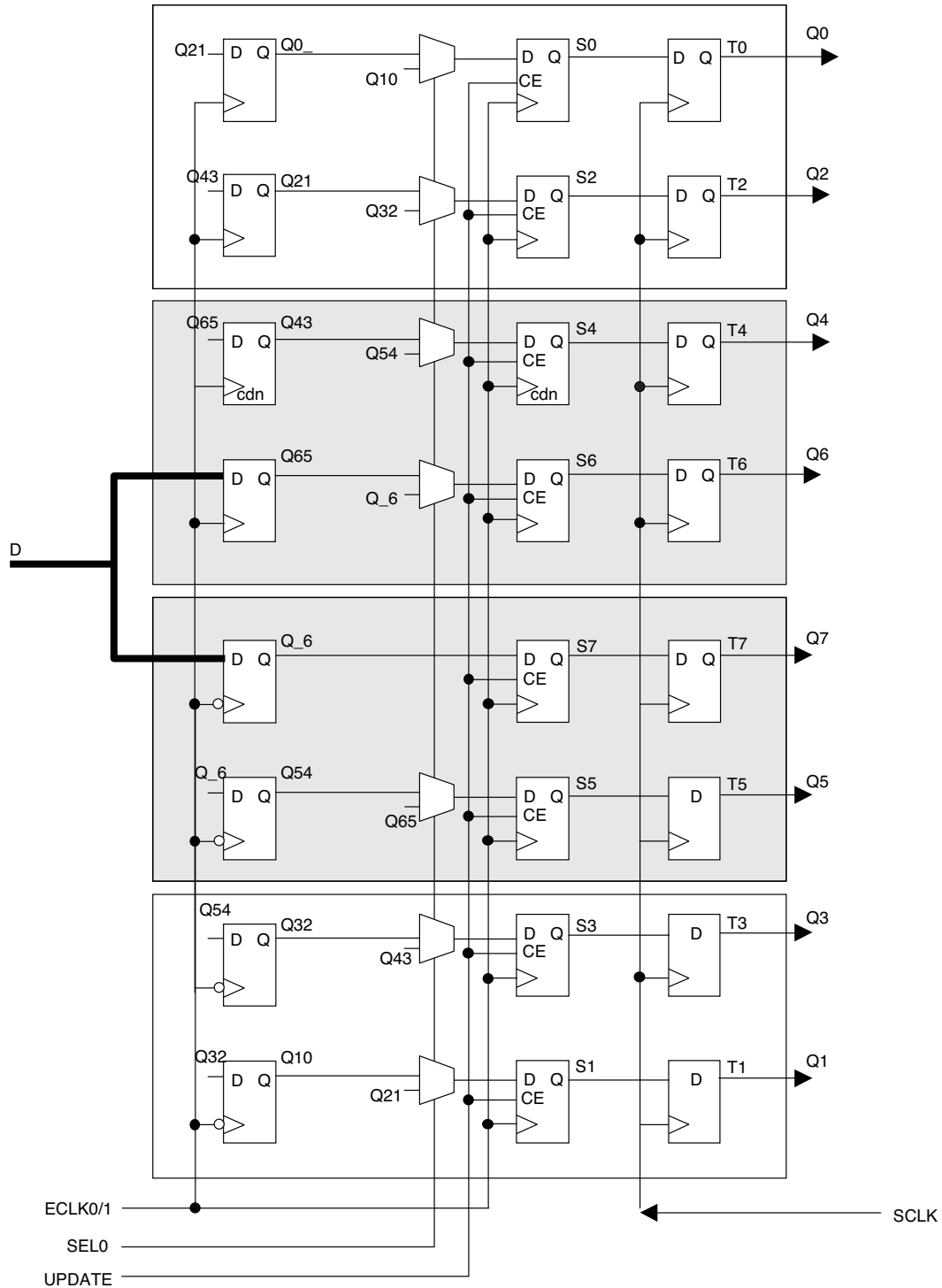
Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2-9 shows the gearbox signals.

Table 2-9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDR4(1:8): Q[7:0] GDDR2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDR2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2-13 shows a block diagram of the input gearbox.

Figure 2-13. Input Gearbox



More information on the input gearbox is available in TN1281, [Implementing High-Speed Interfaces with MachXO3 Devices](#).

Hot Socketing

The MachXO3L/LF devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO3L/LF ideal for many multiple power supply and hot-swap applications.

On-chip Oscillator

Every MachXO3L/LF device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2-13 lists all the available MCLK frequencies.

Table 2-13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

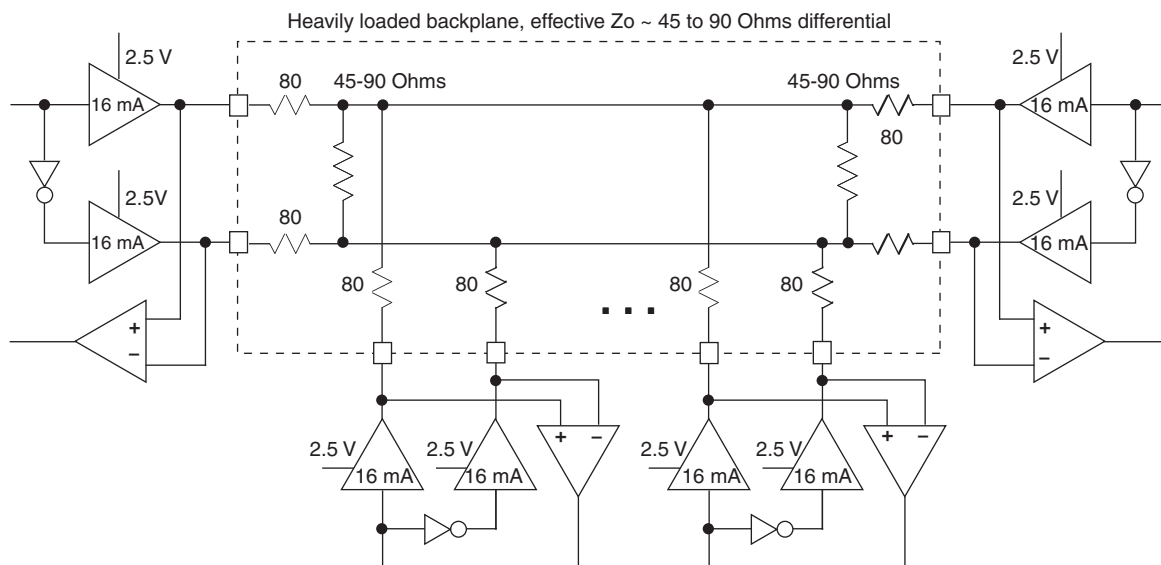


Table 3-2. BLVDS DC Conditions¹

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	20	20	Ohms
R _S	Driver series resistance	80	80	Ohms
R _{TLEFT}	Left end termination	45	90	Ohms
R _{TRIGHT}	Right end termination	45	90	Ohms
V _{OH}	Output high voltage	1.376	1.480	V
V _{OL}	Output low voltage	1.124	1.020	V
V _{OD}	Output differential voltage	0.253	0.459	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

MachXO3L/LF External Switching Characteristics – C/E Devices^{1, 2, 3, 4, 5, 6, 10}
Over Recommended Operating Conditions

Parameter	Description	Device	–6		–5		Units
			Min.	Max.	Min.	Max.	
Clocks							
Primary Clocks							
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	All MachXO3L/LF devices	—	388	—	323	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO3L/LF devices	0.5	—	0.6	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	MachXO3L/LF-1300	—	867	—	897	ps
		MachXO3L/LF-2100	—	867	—	897	ps
		MachXO3L/LF-4300	—	865	—	892	ps
		MachXO3L/LF-6900	—	902	—	942	ps
		MachXO3L/LF-9400	—	908	—	950	ps
Edge Clock							
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	MachXO3L/LF	—	400	—	333	MHz
Pin-LUT-Pin Propagation Delay							
t _{PD}	Best case propagation delay through one LUT-4	All MachXO3L/LF devices	—	6.72	—	6.96	ns
General I/O Pin Parameters (Using Primary Clock without PLL)							
t _{CO}	Clock to Output - PIO Output Register	MachXO3L/LF-1300	—	7.46	—	7.66	ns
		MachXO3L/LF-2100	—	7.46	—	7.66	ns
		MachXO3L/LF-4300	—	7.51	—	7.71	ns
		MachXO3L/LF-6900	—	7.54	—	7.75	ns
		MachXO3L/LF-9400	—	7.53	—	7.83	ns
t _{SU}	Clock to Data Setup - PIO Input Register	MachXO3L/LF-1300	–0.20	—	–0.20	—	ns
		MachXO3L/LF-2100	–0.20	—	–0.20	—	ns
		MachXO3L/LF-4300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-6900	–0.23	—	–0.23	—	ns
		MachXO3L/LF-9400	–0.24	—	–0.24	—	ns
t _H	Clock to Data Hold - PIO Input Register	MachXO3L/LF-1300	1.89	—	2.13	—	ns
		MachXO3L/LF-2100	1.89	—	2.13	—	ns
		MachXO3L/LF-4300	1.94	—	2.18	—	ns
		MachXO3L/LF-6900	1.98	—	2.23	—	ns
		MachXO3L/LF-9400	1.99	—	2.24	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	MachXO3L/LF-1300	1.61	—	1.76	—	ns
		MachXO3L/LF-2100	1.61	—	1.76	—	ns
		MachXO3L/LF-4300	1.66	—	1.81	—	ns
		MachXO3L/LF-6900	1.53	—	1.67	—	ns
		MachXO3L/LF-9400	1.65	—	1.80	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	MachXO3L/LF-1300	–0.23	—	–0.23	—	ns
		MachXO3L/LF-2100	–0.23	—	–0.23	—	ns
		MachXO3L/LF-4300	–0.25	—	–0.25	—	ns
		MachXO3L/LF-6900	–0.21	—	–0.21	—	ns
		MachXO3L/LF-9400	–0.24	—	–0.24	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO3L/LF devices	—	388	—	323	MHz

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned ^{8,9}							
t _{DVA}	Input Data Valid After CLK	All MachXO3L/LF devices, all sides	—	0.317	—	0.344	UI
t _{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	UI
f _{DATA}	DDRX1 Input Data Speed		—	300	—	250	Mbps
f _{DDR1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered ^{8,9}							
t _{SU}	Input Data Setup Before CLK	All MachXO3L/LF devices, all sides	0.566	—	0.560	—	ns
t _{HO}	Input Data Hold After CLK		0.778	—	0.879	—	ns
f _{DATA}	DDRX1 Input Data Speed		—	300	—		Mbps
f _{DDR1}	DDRX1 SCLK Frequency		—	150	—	125	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned ^{8,9}							
t _{DVA}	Input Data Valid After CLK	MachXO3L/LF devices, bottom side only	—	0.316	—	0.342	UI
t _{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f _{DDR2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered ^{8,9}							
t _{SU}	Input Data Setup Before CLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t _{HO}	Input Data Hold After CLK		0.287	—	0.287	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	Mbps
f _{DDR2}	DDRX2 ECLK Frequency		—	332	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Aligned ⁸							
t _{DVA}	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.307	—	0.320	UI
t _{DVE}	Input Data Hold After ECLK		0.782	—	0.699	—	UI
f _{DATA}	DDR4 Serial Input Data Speed		—	800	—	630	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	400	—	315	MHz
f _{SCLK}	SCLK Frequency		—	100	—	79	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Centered ⁸							
t _{SU}	Input Data Setup Before ECLK	MachXO3L/LF devices, bottom side only	0.233	—	0.219	—	ns
t _{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	ns
f _{DATA}	DDR4 Serial Input Data Speed		—	800	—	630	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	400	—	315	MHz
f _{SCLK}	SCLK Frequency		—	100	—	79	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1) ⁹							
t _{DVA}	Input Data Valid After ECLK	MachXO3L/LF devices, bottom side only	—	0.290	—	0.320	UI
t _{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	UI
f _{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	378	—	315	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	MHz

Parameter	Description	Device	-6		-5		Units
			Min.	Max.	Min.	Max.	
MIPI D-PHY Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDR4_RX.ECLK.Centered ^{10, 11, 12}							
t _{SU} ¹⁵	Input Data Setup Before ECLK	All MachXO3L/LF devices, bottom side only	0.200	—	0.200	—	UI
t _{HO} ¹⁵	Input Data Hold After ECLK		0.200	—	0.200	—	UI
f _{DATA} ¹⁴	MIPI D-PHY Input Data Speed		—	900	—	900	Mbps
f _{DDR4} ¹⁴	MIPI D-PHY ECLK Frequency		—	450	—	450	MHz
f _{SCLK} ¹⁴	SCLK Frequency		—	112.5	—	112.5	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Aligned ⁸							
t _{DIA}	Output Data Invalid After CLK Output	All MachXO3L/LF devices, all sides	—	0.520	—	0.550	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	Mbps
f _{DDR1}	DDR1 SCLK frequency		—	150	—	125	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Centered ⁸							
t _{DVB}	Output Data Valid Before CLK Output	All MachXO3L/LF devices, all sides	1.210	—	1.510	—	ns
t _{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	Mbps
f _{DDR1}	DDR1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	MHz
Generic DDR2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Aligned ⁸							
t _{DIA}	Output Data Invalid After CLK Output	MachXO3L/LF devices, top side only	—	0.200	—	0.215	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	Mbps
f _{DDR2}	DDR2 ECLK frequency		—	332	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Centered ^{8, 9}							
t _{DVB}	Output Data Valid Before CLK Output	MachXO3L/LF devices, top side only	0.535	—	0.670	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	Mbps
f _{DDR2}	DDR2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	MHz
Generic DDR4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_TX.ECLK.Aligned ^{8, 9}							
t _{DIA}	Output Data Invalid After CLK Output	MachXO3L/LF devices, top side only	—	0.200	—	0.215	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	ns
f _{DATA}	DDR4 Serial Output Data Speed		—	800	—	630	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	400	—	315	MHz
f _{SCLK}	SCLK Frequency		—	100	—	79	MHz

I²C Port Timing Specifications^{1, 2}

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCL clock frequency	—	400	kHz

- MachXO3L/LF supports the following modes:
 - Standard-mode (Sm), with a bit rate up to 100 kbit/s (user and configuration mode)
 - Fast-mode (Fm), with a bit rate up to 400 kbit/s (user and configuration mode)
- Refer to the I²C specification for timing requirements.

SPI Port Timing Specifications¹

Symbol	Parameter	Min.	Max.	Units
f _{MAX}	Maximum SCK clock frequency	—	45	MHz

- Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

Switching Test Conditions

Figure 3-9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-9. Output Test Load, LVTTTL and LVCMOS Standards

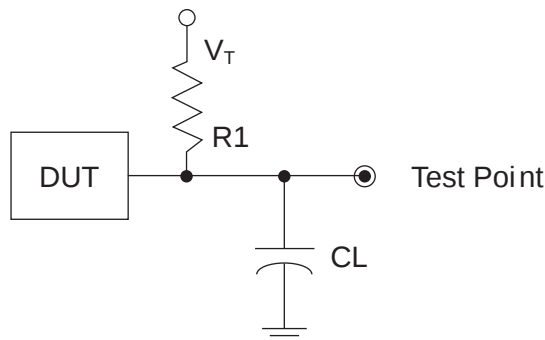


Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = V _{CCIO} /2	—
			LVCMOS 1.8 = V _{CCIO} /2	—
			LVCMOS 1.5 = V _{CCIO} /2	—
			LVCMOS 1.2 = V _{CCIO} /2	—
LVTTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5	V _{OL}
LVTTTL and LVCMOS 3.3 (Z -> L)			1.5	V _{OH}
Other LVCMOS (Z -> H)			V _{CCIO} /2	V _{OL}
Other LVCMOS (Z -> L)			V _{CCIO} /2	V _{OH}
LVTTTL + LVCMOS (H -> Z)			V _{OH} - 0.15	V _{OL}
LVTTTL + LVCMOS (L -> Z)			V _{OL} - 0.15	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

	MachXO3L/LF-6900				
	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank					
Bank 0	50	73	50	71	83
Bank 1	52	68	52	68	84
Bank 2	52	72	52	72	84
Bank 3	16	24	16	24	28
Bank 4	16	16	16	16	24
Bank 5	20	28	20	28	32
Total General Purpose Single Ended IO	206	281	206	279	335
Differential IO per Bank					
Bank 0	25	36	25	36	42
Bank 1	26	34	26	34	42
Bank 2	26	36	26	36	42
Bank 3	8	12	8	12	14
Bank 4	8	8	8	8	12
Bank 5	10	14	10	14	16
Total General Purpose Differential IO	103	140	103	140	168
Dual Function IO	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes					
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	20	21	20	21	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	21	20	21	21
High-speed Differential Outputs					
Bank 0	20	21	20	21	21
VCCIO Pins					
Bank 0	4	4	4	4	5
Bank 1	3	4	4	4	5
Bank 2	4	4	4	4	5
Bank 3	2	2	1	2	2
Bank 4	2	2	2	2	2
Bank 5	2	2	1	2	2
VCC	8	8	8	10	10
GND	24	16	24	16	33
NC	0	0	1	0	0
Reserved for Configuration	1	1	1	1	1
Total Count of Bonded Pins	256	324	256	324	400

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3L-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3L-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3L-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND

MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-640E-5MG121C	640	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-6MG121C	640	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-640E-5MG121I	640	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-640E-6MG121I	640	1.2 V	6	Halogen-Free csfBGA	121	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-1300E-5UWG36CTR	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR50	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36CTR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	COM
LCMXO3LF-1300E-5UWG36ITR	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR50	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5UWG36ITR1K	1300	1.2 V	5	Halogen-Free WLCSP	36	IND
LCMXO3LF-1300E-5MG121C	1300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-6MG121C	1300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-1300E-5MG121I	1300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-6MG121I	1300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-1300E-5MG256C	1300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-6MG256C	1300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-1300E-5MG256I	1300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300E-6MG256I	1300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-1300C-5BG256C	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-6BG256C	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-1300C-5BG256I	1300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-1300C-6BG256I	1300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-2100E-5UWG49CTR	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR50	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49CTR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	COM
LCMXO3LF-2100E-5UWG49ITR	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR50	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5UWG49ITR1K	2100	1.2 V	5	Halogen-Free WLCSP	49	IND
LCMXO3LF-2100E-5MG121C	2100	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-6MG121C	2100	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3LF-2100E-5MG121I	2100	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-6MG121I	2100	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3LF-2100E-5MG256C	2100	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-6MG256C	2100	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-2100E-5MG256I	2100	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-6MG256I	2100	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-2100E-5MG324C	2100	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-6MG324C	2100	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3LF-2100E-5MG324I	2100	1.2 V	5	Halogen-Free csfBGA	324	IND

MachXO3 Family Data Sheet

Revision History

February 2017

Advance Data Sheet DS1047

Date	Version	Section	Change Summary
February 2017	1.8	Architecture	Updated Supported Standards section. Corrected “MDVS” to “MLDVS” in Table 2-11, Supported Input Standards.
		DC and Switching Characteristics	Updated ESD Performance section. Added reference to the MachXO2 Product Family Qualification Summary document.
			Updated Static Supply Current – C/E Devices section. Added footnote 7.
			Updated MachXO3L/LF External Switching Characteristics – C/E Devices section. — Populated values for MachXO3L/LF-9400. — Under 7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1, corrected “t _{DVB} ” to “t _{DIB} ” and “t _{DVA} ” to “t _{DIA} ” and revised their descriptions. — Added Figure 3-6, Receiver GDDR71_RX Waveforms and Figure 3-7, Transmitter GDDR71_TX Waveforms.
		Pinout Information	Updated the Pin Information Summary section. Added MachXO3L/LF-9600C packages.
May 2016	1.7	DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Modified I/O Tri-state Voltage Applied and Dedicated Input Voltage Applied footnotes.
			Updated sysIO Recommended Operating Conditions section. — Added standards. — Added V _{REF} (V) — Added footnote 4.
			Updated sysIO Single-Ended DC Electrical Characteristics section. Added I/O standards.
		Ordering Information	Updated MachXO3L Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.
			Updated MachXO3LF Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added LCMXO3L-9400C part numbers.

Date	Version	Section	Change Summary
June 2014	1.0	—	Product name/trademark adjustment.
		Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Changed fcCSP packages to csfBGA. Adjusted 121-ball csfBGA arrow.
			Introduction section general update.
		Architecture	General update.
		DC and Switching Characteristics	Updated sysIO Recommended Operating Conditions section. Removed V_{REF} (V) column. Added standards.
			Updated Maximum sysIO Buffer Performance section. Added MIPI I/O standard.
			Updated MIPI D-PHY Emulation section. Changed Low Speed to Low Power. Updated Table 3-4, MIPI DC Conditions.
			Updated Table 3-5, MIPI D-PHY Output DC Conditions.
			Updated Maximum sysIO Buffer Performance section.
			Updated MachXO3L External Switching Characteristics – C/E Device section.
May 2014	00.3	Introduction	Updated Features section.
			Updated Table 1-1, MachXO3L Family Selection Guide. Moved 121-ball fcCSP arrow.
			General update of Introduction section.
		Architecture	General update.
		Pinout Information	Updated Pin Information Summary section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
		Ordering Information	Updated MachXO3L Part Number Description section. Updated or added data on WLCSP49, WLCSP81, CABGA324, and CABGA400 for specific devices.
			Updated Ultra Low Power Commercial and Industrial Grade Devices, Halogen Free (RoHS) Packaging section. Added part numbers.
February 2014	00.2	DC and Switching Characteristics	Updated MachXO3L External Switching Characteristics – C/E Devices table. Removed LPDDR and DDR2 parameters.
	00.1	—	Initial release.