# E · Chattile Semiconductor Corporation - <u>LCMXO3LF-9400C-5BG400C Datasheet</u>



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	1175
Number of Logic Elements/Cells	9400
Total RAM Bits	442368
Number of I/O	335
Number of Gates	-
Voltage - Supply	2.375V ~ 3.465V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lcmxo3lf-9400c-5bg400c

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# MachXO3 Family Data Sheet Introduction

#### January 2016

# **Features**

### Solutions

- Smallest footprint, lowest power, high data throughput bridging solutions for mobile applications
- Optimized footprint, logic density, IO count, IO performance devices for IO management and logic applications
- High IO/logic, lowest cost/IO, high IO devices for IO expansion applications

## ■ Flexible Architecture

- Logic Density ranging from 640 to 9.4K LUT4
- High IO to LUT ratio with up to 384 IO pins

## Advanced Packaging

- 0.4 mm pitch: 1K to 4K densities in very small footprint WLCSP (2.5 mm x 2.5 mm to 3.8 mm x 3.8 mm) with 28 to 63 IOs
- 0.5 mm pitch: 640 to 6.9K LUT densities in 6 mm x 6 mm to 10 mm x 10 mm BGA packages with up to 281 IOs
- 0.8 mm pitch: 1K to 9.4K densities with up to 384 IOs in BGA packages

## Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/Os
- Generic DDR, DDRx2, DDRx4

## High Performance, Flexible I/O Buffer

- Programmable sysIO<sup>™</sup> buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
  - LVDS, Bus-LVDS, MLVDS, LVPECL
  - MIPI D-PHY Emulated
  - Schmitt trigger inputs, up to 0.5 V hysteresis
- Ideal for IO bridging applications
- I/Os support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

## ■ Flexible On-Chip Clocking

- · Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
  - Wide input frequency range (7 MHz to 400 MHz)
- Non-volatile, Multi-time Programmable
  - Instant-on
    - Powers up in microseconds
    - · Optional dual boot with external SPI memory
    - Single-chip, secure solution
    - Programmable through JTAG, SPI or I<sup>2</sup>C
    - MachXO3L includes multi-time programmable NVCM
    - MachXO3LF infinitely reconfigurable Flash

       Supports background programming of non-volatile memory

## TransFR Reconfiguration

In-field logic update while IO holds the system state

## Enhanced System Level Support

- On-chip hardened functions: SPI, I<sup>2</sup>C, timer/ counter
- On-chip oscillator with 5.5% accuracy
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

#### Applications

- Consumer Electronics
- Compute and Storage
- Wireless Communications
- Industrial Control Systems
- Automotive System

#### Low Cost Migration Path

- Migration from the Flash based MachXO3LF to the NVCM based MachXO3L
- · Pin compatible and equivalent timing

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#### Advance Data Sheet DS1047



# **ROM Mode**

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

# Routing

There are many resources provided in the MachXO3L/LF devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

# **Clock/Control Distribution Network**

Each MachXO3L/LF device has eight clock inputs (PCLK [T, C] [Banknum]\_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO3L/LF architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO3L/LF devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO3L/LF devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO3L/LF External Switching Characteristics table.

Primary clock signals for the MachXO3L/LF-1300 and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sys-CLOCK PLL outputs.



### Table 2-4. PLL Signal Descriptions (Continued)

Port Name	I/O	Description
CLKOP	0	Primary PLL output clock (with phase shift adjustment)
CLKOS	0	Secondary PLL output clock (with phase shift adjust)
CLKOS2	0	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	0	Secondary PLL output clock3 (with phase shift adjust)
LOCK	0	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed- back signals.
DPHSRC	0	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset - includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	0	PLL data bus data output
PLLACK	0	PLL data bus acknowledge signal

# sysMEM Embedded Block RAM Memory

The MachXO3L/LF devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

#### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-5.



state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

#### Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-9.

#### Figure 2-9. Memory Core Reset



For further information on the sysMEM EBR block, please refer to TN1290, Memory Usage Guide for MachXO3 Devices.

#### EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-10. The GSR input to the EBR is always asynchronous.

#### Figure 2-10. EBR Asynchronous Reset (Including GSR) Timing Diagram

Reset	
Clock	
Clock	

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of 1/f<sub>MAX</sub> (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.



# PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Pin Name	I/О Туре	Description
CE	Input	Clock Enable
D	Input	Pin input from sysIO buffer.
INDD	Output	Register bypassed input.
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysIO Buffer
TQ	Output	Tri-state output signals to sysIO Buffer
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

# Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

## Left, Top, Bottom Edges

Input signals are fed from the sysIO buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/Os on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.



# Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2-10 shows the gearbox signals.

## Table 2-10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]		
GDDRX4(8:1): D[7:0]		
GDDRX2(4:1)(IOL-A): D[3:0]		
GDDRX2(4:1)(IOL-C): D[7:4]		
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysIO buffer. Figure 2-14 shows the output gearbox block diagram.



# **Embedded Hardened IP Functions**

All MachXO3L/LF devices provide embedded hardened functions such as SPI, I<sup>2</sup>C and Timer/Counter. MachXO3LF devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2-17.

## Figure 2-17. Embedded Function Block Interface



# Hardened I<sup>2</sup>C IP Core

Every MachXO3L/LF device contains two  $I^2C$  IP cores. These are the primary and secondary  $I^2C$  IP cores. Either of the two cores can be configured either as an  $I^2C$  master or as an  $I^2C$  slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it will be able to control other devices on the  $I^2C$  bus through the interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an  $I^2C$  Master. The  $I^2C$  cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface



For more details on these embedded functions, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

# **User Flash Memory (UFM)**

MachXO3LF devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 256 kbits
- 100K write cycles
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, please refer to TN1293, Using Hardened Control Functions in MachXO3 Devices.

# **Standby Mode and Power Saving Options**

MachXO3L/LF devices are available in two options, the C and E devices. The C devices have a built-in voltage regulator to allow for 2.5 V V<sub>CC</sub> and 3.3 V V<sub>CC</sub> while the E devices operate at 1.2 V V<sub>CC</sub>.

MachXO3L/LF devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO3L/LF devices support a low power Stand-by mode.

In the stand-by mode the MachXO3L/LF devices are powered on and configured. Internal logic, I/Os and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I<sup>2</sup>C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry etc can be configured such that they are automatically turned "off" or go into a low power consumption state to save power when the device enters this state. Note that the MachXO3L/LF devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.



## Table 2-17. MachXO3L/LF Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors VCC levels. In the event of unsafe $V_{CC}$ drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL will wait until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/Os such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/Os off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the standby mode refer to TN1289, Power Estimation and Management for MachXO3 Devices.

# Power On Reset

MachXO3L/LF devices have power-on reset circuitry to monitor  $V_{CCINT}$  and  $V_{CCIO}$  voltage levels during power-up and operation. At power-up, the POR circuitry monitors  $V_{CCINT}$  and  $V_{CCIO}$  (controls configuration) voltage levels. It then triggers download from the on-chip configuration NVCM/Flash memory after reaching the  $V_{PORUP}$  level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For "E" devices without voltage regulators,  $V_{CCINT}$  is the same as the  $V_{CC}$  supply voltage. For "C" devices with voltage regulators,  $V_{CCINT}$  is regulated from the  $V_{CC}$  supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as NVCM/Flash Download Time ( $t_{REFRESH}$ ) in the DC and Switching Characteristics section of this data sheet. Before and during configuration. Note that for "C" devices, a separate POR circuit monitors external  $V_{CC}$  voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor  $V_{CCINT}$  levels. If  $V_{CCINT}$  drops below  $V_{PORDNBG}$  level (with the bandgap circuitry switched on) or below  $V_{PORDNSRAM}$  level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the  $V_{CCINT}$  and  $V_{CCIO}$  voltage levels.  $V_{PORDNBG}$  and  $V_{PORDNSRAM}$  are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once an "E" device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a mini-mal, low power POR circuit is still operational (this corresponds to the  $V_{PORDNSRAM}$  reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the  $V_{CC}$  supply dropping below  $V_{CC}$  (min) they should not shut down the bandgap or POR circuit.



# TraceID

Each MachXO3L/LF device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I<sup>2</sup>C, or JTAG interfaces.

# **Density Shifting**

The MachXO3L/LF family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices. For more details refer to the MachXO3 migration files.



# LVDS Emulation

MachXO3L/LF devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.





Note: All resistors are ±1%.

## Table 3-1. LVDS25E DC Conditions

#### **Over Recommended Operating Conditions**

Parameter	Description	Тур.	Units
Z <sub>OUT</sub>	Output impedance	20	Ohms
R <sub>S</sub>	Driver series resistor	158	Ohms
R <sub>P</sub>	Driver parallel resistor	140	Ohms
R <sub>T</sub>	Receiver termination	100	Ohms
V <sub>OH</sub>	Output high voltage	1.43	V
V <sub>OL</sub>	Output low voltage	1.07	V
V <sub>OD</sub>	Output differential voltage	0.35	V
V <sub>CM</sub>	Output common mode voltage	1.25	V
Z <sub>BACK</sub>	Back impedance	100.5	Ohms
I <sub>DC</sub>	DC output current	6.03	mA



# BLVDS

The MachXO3L/LF family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

## Figure 3-2. BLVDS Multi-point Output Example



#### Table 3-2. BLVDS DC Conditions<sup>1</sup>

Over Recommended	Operating	Conditions
	operating	oonantions

	Nominal			
Symbol	Description	Zo = 45	Zo = 90	Units
Z <sub>OUT</sub>	Output impedance	20	20	Ohms
R <sub>S</sub>	Driver series resistance	80	80	Ohms
R <sub>TLEFT</sub>	Left end termination	45	90	Ohms
R <sub>TRIGHT</sub>	Right end termination	45	90	Ohms
V <sub>OH</sub>	Output high voltage	1.376	1.480	V
V <sub>OL</sub>	Output low voltage	1.124	1.020	V
V <sub>OD</sub>	Output differential voltage	0.253	0.459	V
V <sub>CM</sub>	Output common mode voltage	1.250	1.250	V
I <sub>DC</sub>	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.



## Table 3-5. MIPI D-PHY Output DC Conditions<sup>1</sup>

	Description	Min.	Тур.	Max.	Units
Transmitter	· · ·			•	
External Termination	on				
RL	1% external resistor with VCCIO = 2.5 V		50		Ohms
	1% external resistor with VCCIO = 3.3 V	—	50	—	
RH	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when VCCIO = 2.5 V	—	330	_	Ohms
	1% external resistor with performance between 800 Mbps to 900 Mbps when VCCIO = 3.3 V	_	464	—	Ohms
High Speed	· ·				
VCCIO	VCCIO of the Bank with LVDS Emulated output buffer	_	2.5	_	V
	VCCIO of the Bank with LVDS Emulated output buffer	_	3.3	—	V
VCMTX	HS transmit static common mode voltage	150	200	250	mV
VOD	HS transmit differential voltage	140	200	270	mV
VOHHS	HS output high voltage	_	—	360	V
ZOS	Single ended output impedance		50	_	Ohms
ΔZOS	Single ended output impedance mismatch		—	10	%
Low Power					
VCCIO	VCCIO of the Bank with LVCMOS12D 6 mA drive bidirectional IO buffer	_	1.2	_	V
VOH	Output high level	1.1	1.2	1.3	V
VOL	Output low level	-50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ohms

1. Over Recommended Operating Conditions



# Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
MIPI	450	MHz
LVDS25	400	MHz
LVDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVCMOS33	150	MHz
LVCMOS33D	150	MHz
LVCMOS25	150	MHz
LVCMOS25D	150	MHz
LVCMOS18	150	MHz
LVCMOS18D	150	MHz
LVCMOS15	150	MHz
LVCMOS15D	150	MHz
LVCMOS12	91	MHz
LVCMOS12D	91	MHz



# **JTAG Port Timing Specifications**

Symbol	Parameter	Min.	Max.	Units
f <sub>MAX</sub>	TCK clock frequency	—	25	MHz
t <sub>BTCPH</sub>	TCK [BSCAN] clock pulse width high	20	—	ns
t <sub>BTCPL</sub>	TCK [BSCAN] clock pulse width low	20	—	ns
t <sub>BTS</sub>	TCK [BSCAN] setup time	10	—	ns
t <sub>BTH</sub>	TCK [BSCAN] hold time	8	—	ns
t <sub>BTCO</sub>	TAP controller falling edge of clock to valid output	—	10	ns
t <sub>BTCODIS</sub>	TAP controller falling edge of clock to valid disable	—	10	ns
t <sub>BTCOEN</sub>	TAP controller falling edge of clock to valid enable	—	10	ns
t <sub>BTCRS</sub>	BSCAN test capture register setup time	8	—	ns
t <sub>BTCRH</sub>	BSCAN test capture register hold time	20	—	ns
t <sub>BUTCO</sub>	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t <sub>BTUODIS</sub>	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t <sub>BTUPOEN</sub>	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

## Figure 3-8. JTAG Port Timing Waveforms





# sysCONFIG Port Timing Specifications

Symbol	Parameter		Min.	Max.	Units
All Configuration Mo	odes				
t <sub>PRGM</sub>	PROGRAMN low p	ulse accept	55	_	ns
t <sub>PRGMJ</sub>	PROGRAMN low p	ulse rejection	_	25	ns
t <sub>INITL</sub>	INITN low time	LCMXO3L/LF-640/ LCMXO3L/LF-1300	—	55	us
		LCMXO3L/LF-1300 256-Ball Package/ LCMXO3L/LF-2100	_	70	us
		LCMXO3L/LF-2100 324-Ball Package/ LCMXO3-4300	_	105	us
		LCMXO3L/LF-4300 400-Ball Package/ LCMXO3-6900	_	130	us
		LCMXO3L/LF-9400C	_	175	us
t <sub>DPPINIT</sub>	PROGRAMN low to	NITN low	_	150	ns
t <sub>DPPDONE</sub>	PROGRAMN low to	DONE low	_	150	ns
t <sub>IODISS</sub>	PROGRAMN low to	o I/O disable	_	120	ns
Slave SPI					
f <sub>MAX</sub>	CCLK clock frequer	псу		66	MHz
t <sub>CCLKH</sub>	CCLK clock pulse v	vidth high	7.5	—	ns
t <sub>CCLKL</sub>	CCLK clock pulse v	CCLK clock pulse width low			ns
t <sub>STSU</sub>	CCLK setup time		2	_	ns
t <sub>STH</sub>	CCLK hold time		0	_	ns
t <sub>STCO</sub>	CCLK falling edge t	CCLK falling edge to valid output			ns
t <sub>STOZ</sub>	CCLK falling edge t	o valid disable	—	10	ns
t <sub>STOV</sub>	CCLK falling edge t	o valid enable	—	10	ns
t <sub>SCS</sub>	Chip select high tim	ne	25	—	ns
t <sub>SCSS</sub>	Chip select setup ti	me	3	—	ns
t <sub>SCSH</sub>	Chip select hold tim	ne	3	—	ns
Master SPI					
f <sub>MAX</sub>	MCLK clock freque	ncy	_	133	MHz
t <sub>MCLKH</sub>	MCLK clock pulse v	vidth high	3.75	_	ns
t <sub>MCLKL</sub>	MCLK clock pulse v	width low	3.75	—	ns
t <sub>STSU</sub>	MCLK setup time		5	—	ns
t <sub>STH</sub>	MCLK hold time		1	—	ns
t <sub>CSSPI</sub>	INITN high to chip s	select low	100	200	ns
t <sub>MCLK</sub>	INITN high to first M	ICLK edge	0.75	1	US



	MachXO3L/LF-4300						
	WLCSP81	CSFBGA121	CSFBGA256	CSFBGA324	CABGA256	CABGA324	CABGA400
General Purpose IO per Bank							
Bank 0	29	24	50	71	50	71	83
Bank 1	0	26	52	62	52	68	84
Bank 2	20	26	52	72	52	72	84
Bank 3	7	7	16	22	16	24	28
Bank 4	0	7	16	14	16	16	24
Bank 5	7	10	20	27	20	28	32
Total General Purpose Single Ended IO	63	100	206	268	206	279	335
Differential IO per Bank							
Bank 0	15	12	25	36	25	36	42
Bank 1	0	13	26	30	26	34	42
Bank 2	10	13	26	36	26	36	42
Bank 3	3	3	8	10	8	12	14
Bank 4	0	3	8	6	8	8	12
Bank 5	3	5	10	13	10	14	16
Total General Purpose Differential IO	31	49	103	131	103	140	168
Dual Function IO	25	37	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes							
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	10	7	18	18	18	18	21
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	10	13	18	18	18	18	21
High-speed Differential Outputs							
Bank 0	10	7	18	18	18	18	21
VCCIO Pins							
Bank 0	3	1	4	4	4	4	5
Bank 1	0	1	3	4	4	4	5
Bank 2	2	1	4	4	4	4	5
Bank 3	1	1	2	2	1	2	2
Bank 4	0	1	2	2	2	2	2
Bank 5	1	1	2	2	1	2	2
VCC	4	4	8	8	8	10	10
GND	6	10	24	16	24	16	33
NC	0	0	0	13	1	0	0
Reserved for Configuration	1	1	1	1	1	1	1
Total Count of Bonded Pins	81	121	256	324	256	324	400



Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-2100E-6MG324I	2100	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-2100C-5BG256C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-6BG256C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-2100C-5BG256I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-6BG256I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-2100C-5BG324C	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-6BG324C	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-2100C-5BG324I	2100	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-2100C-6BG324I	2100	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
				1		
Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3L-4300E-5UWG81CTR	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR50	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81CTR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	COM
LCMXO3L-4300E-5UWG81ITR	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR50	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5UWG81ITR1K	4300	1.2 V	5	Halogen-Free WLCSP	81	IND
LCMXO3L-4300E-5MG121C	4300	1.2 V	5	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-6MG121C	4300	1.2 V	6	Halogen-Free csfBGA	121	COM
LCMXO3L-4300E-5MG121I	4300	1.2 V	5	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-6MG121I	4300	1.2 V	6	Halogen-Free csfBGA	121	IND
LCMXO3L-4300E-5MG256C	4300	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-6MG256C	4300	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3L-4300E-5MG256I	4300	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-6MG256I	4300	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3L-4300E-5MG324C	4300	1.2 V	5	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-6MG324C	4300	1.2 V	6	Halogen-Free csfBGA	324	COM
LCMXO3L-4300E-5MG324I	4300	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3L-4300E-6MG324I	4300	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3L-4300C-5BG256C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-6BG256C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3L-4300C-5BG256I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-6BG256I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3L-4300C-5BG324C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-6BG324C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3L-4300C-5BG324I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-6BG324I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3L-4300C-5BG400C	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-6BG400C	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3L-4300C-5BG400I	4300	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3L-4300C-6BG400I	4300	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND



Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-6900E-5MG256C	6900	1.2 V	5	Halogen-Free csfBGA	256	СОМ
LCMXO3LF-6900E-6MG256C	6900	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-6900E-5MG256I	6900	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-6MG256I	6900	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-6900E-5MG324C	6900	1.2 V	5	Halogen-Free csfBGA	324	СОМ
LCMXO3LF-6900E-6MG324C	6900	1.2 V	6	Halogen-Free csfBGA	324	СОМ
LCMXO3LF-6900E-5MG324I	6900	1.2 V	5	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900E-6MG324I	6900	1.2 V	6	Halogen-Free csfBGA	324	IND
LCMXO3LF-6900C-5BG256C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-6BG256C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-6900C-5BG256I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-6BG256I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-6900C-5BG324C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-6BG324C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	COM
LCMXO3LF-6900C-5BG324I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-6BG324I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	324	IND
LCMXO3LF-6900C-5BG400C	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-6BG400C	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-6900C-5BG400I	6900	2.5 V / 3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-6900C-6BG400I	6900	2.5 V / 3.3 V	6	Halogen-Free caBGA	400	IND
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Part Number	LUTs	Supply Voltage	Speed	Package	Leads	Temp.
LCMXO3LF-9400E-5MG256C	9400	1.2 V	5	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-6MG256C	9400	1.2 V	6	Halogen-Free csfBGA	256	COM
LCMXO3LF-9400E-5MG256I	9400	1.2 V	5	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400E-6MG256I	9400	1.2 V	6	Halogen-Free csfBGA	256	IND
LCMXO3LF-9400C-5BG256C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-6BG256C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	COM
LCMXO3LF-9400C-5BG256I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-6BG256I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	256	IND
LCMXO3LF-9400C-5BG400C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-6BG400C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	COM
LCMXO3LF-9400C-5BG400I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-6BG400I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	400	IND
LCMXO3LF-9400C-5BG484C	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-6BG484C	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	COM
LCMXO3LF-9400C-5BG484I	9400	2.5 V/3.3 V	5	Halogen-Free caBGA	484	IND
LCMXO3LF-9400C-6BG484I	9400	2.5 V/3.3 V	6	Halogen-Free caBGA	484	IND



Date	Version	Section	Change Summary
September 2015	1.5	DC and Switching Characteristics	Updated the MIPI D-PHY Emulation section. Revised Table 3-5, MIPI D- PHY Output DC Conditions. — Revised RL Typ. value. — Revised RH description and values.
			Updated the Maximum sysIO Buffer Performance section. Revised MIPI Max. Speed value.
			Updated the MachXO3L/LF External Switching Characteristics – C/E Devices section. Added footnotes 14 and 15.
August 2015	1.4	Architecture	Updated the Device Configuration section. Added JTAGENB to TAP dual purpose pins.
		Ordering Information	Updated the top side markings section to indicate the use of LMXO3LF for the LCMXO3LF device.
March 2015	1.3	All	General update. Added MachXO3LF devices.
October 2014	1.2	Introduction	Updated Table 1-1, MachXO3L Family Selection Guide. Revised XO3L- 2100 and XO3L-4300 IO for 324-ball csfBGA package.
		Architecture	Updated the Dual Boot section. Corrected information on where the pri- mary bitstream and the golden image must reside.
		Pinout Information	Updated the Pin Information Summary section.
			Changed General Purpose IO Bank 5 values for MachXO3L-2100 and MachXO3L-4300 CSFBGA 324 package.
			Changed Number 7:1 or 8:1 Gearboxes for MachXO3L-640 and MachXO3L-1300.
			Removed DQS Groups (Bank 1) section.
			Changed VCCIO Pins Bank 1 values for MachXO3L-1300, MachXO3L- 2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.
			Changed GND values for MachXO3L-1300, MachXO3L-2100, MachXO3L-4300 and MachXO3L-6900 CSFBGA 256 package.
			Changed NC values for MachXO3L-2100 and MachXO3L-4300 CSF- BGA 324 package.
		DC and Switching Characteristics	Updated the BLVDS section. Changed output impedance nominal values in Table 3-2, BLVDS DC Condition.
			Updated the LVPECL section. Changed output impedance nominal value in Table 3-3, LVPECL DC Condition.
			Updated the sysCONFIG Port Timing Specifications section. Updated INITN low time values.
July 2014	1.1	DC and Switching Characteristics	Updated the Static Supply Current – C/E Devices section. Added devices.
			Updated the Programming and Erase Supply Current – C/E Device section. Added devices.
			Updated the sysIO Single-Ended DC Electrical Characteristics section. Revised footnote 4.
			Added the NVCM Download Time section.
			Updated the Typical Building Block Function Performance – C/E Devices section. Added information to footnote.
		Pinout Information	Updated the Pin Information Summary section.
		Ordering Information	Updated the MachXO3L Part Number Description section. Added packages.
			Updated the Ordering Information section. General update.