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Applications of "Embedded - Microcontrollers"

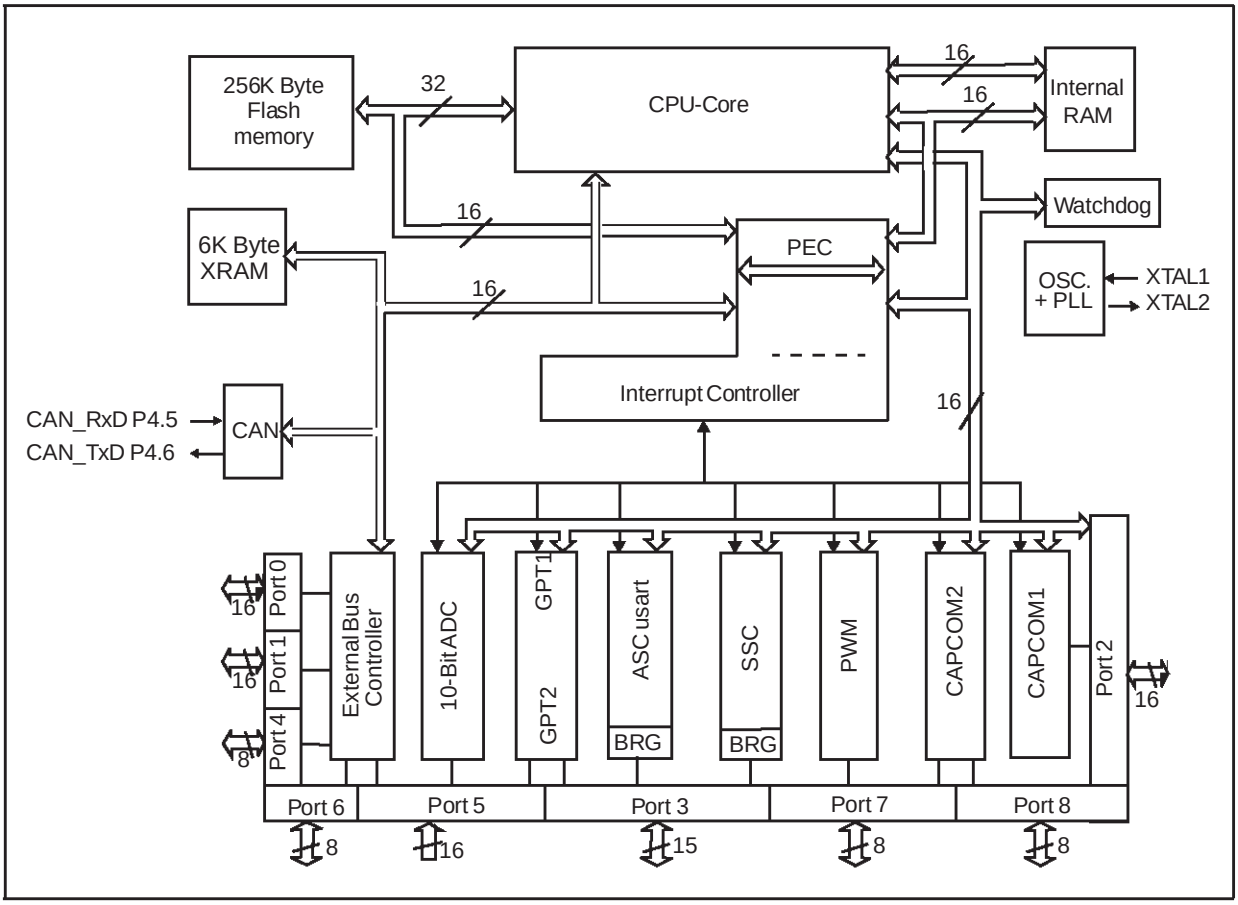
Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f168sq6

3 - FUNCTIONAL DESCRIPTION

The architecture of the ST10F168 combines advantages of both RISC and CISC processors and an advanced peripheral subsystem.

The block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10F168.

Figure 3 : Block Diagram



5 - FLASH MEMORY

The ST10F168 provides 256K Byte of an electrically erasable and reprogrammable Flash Memory on-chip.

The Flash Memory can be used both for code and data storage. It is organized into four 32-bit wide blocks allowing even double Word instructions to be fetched in one machine cycle. The four blocks of size16K, 48K, 96K and 96K Byte can be erased and reprogrammed individually (see Table 2 and Table 3).

The Flash Memory can be programmed in a programming board or in the target system which provides high system flexibility. The algorithms to program or erase the flash memory are embedded in the Flash Memory itself (ST Embedded Algorithm Kernel, or STEAK^{TM}).

To start a program / erase operation, the user's software has just to load GPRs with the address and data to be programmed, or sector to be erased. STEAK uses embedded routines, which check the validity of the programmed parameters, decode and then execute the programming or erase command. During operation, the STEAK routines carry out checks and retries to verify proper cell programming or erasing. When an error occurs, STEAK returns an error-code which identifies the cause of the error.

A Flash Memory protection option prevents the read-back of the Flash Memory contents from external memory, or from on-chip RAM. Code operation from within the Flash continues as normal.

The first bank (16K Byte) and part of the second bank (16K Byte out of 48K Byte) of the on-chip Flash Memory of the ST10F168 can be mapped to either segment 0 (addresses 00000h to 07FFFh) or to segment 1 (addresses 10000h to 17FFFh) during the initialization phase. External memory can be used for additional system flexibility.

V_{DD} = 5V ± 10%, V_{PP} = 12V ± 5%, V_{SS} = 0V, f_{CPU} = 25MHz, for Q6 version : T_A = -40°C, +85°C and for Q3 version T_A = -40°C, + 125°C.

Table 2 : Flash Memory Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{CPU}	CPU Frequency during erasing / programming operation		5	-	32	MHz
Cyc	Erasing / Programming Cycles	f_{CPU} = 25MHz	-	-	10K	
t_{SPRG}	Single Word Programming Time	f_{CPU} = 25MHz	-	40	1500	µs
t_{DPRG}	Double Word Programming Time	f_{CPU} = 25MHz	-	40	1500	µs
t_{EBNK}	Sector Erasing Time	f_{CPU} = 25MHz	-	3	15	s
t_{RET}	Data Retention Time	Defectivity below 1ppm / year	20	-	-	year

Table 3 : Flash Memory Bank Organisation

Bank	Addresses (segment 0)	Addresses (segment 1)	Size (Byte)
0	000000h to 003FFFh	010000h to 013FFFh	16K
1	004000h to 007FFFh + 018000h to 01FFFFh	014000h to 01FFFFh	48K
2	020000h to 037FFFh	020000h to 03FFFFh	96K
3	038000h to 04FFFFh	038000h to 04FFFFh	96K

Table 6 : Error Code Definition (R0 content after STEAK execution)

Error Code	Meaning
00h	Operation was successful
01h	Flash Protection is active
02h	Vpp voltage not present
03h	Programming operation failed
04h	Address value (R1) incorrect: not in Flash address area or odd
05h	CPU period out of range (must be between 30 ns to 500 ns)
06h	Not enough free space on system stack for proper operation
07h	Incorrect bank number (R2,R3) specified
08h	Erase operation failed (phase 1)
09h	Bad source address for Multiple Word programming command
0Ah	Bad number of words to be copied in Multiple Word programming command: one destination will be out of flash.
0Bh	PLL Unlocked or Oscillator watchdog overflow occured during programming or erasing the flash.
0Ch	Erase operation failed (phase 2)
FFh	Unknown or bad command

Table 7 : Return values for each programming / erase command

Programming Command	R0	R1	R2	R3	R4-R15
Single or double Word programming	Error code	Unchanged	Data in Flash for location Segment + Segment Offset (R0.[3:0] with R1)	Data in Flash for location Segment + Segment Offset + 2 (R0[3:0] with R1+2)	Unchanged
Block programming	Error code	The last segment offset address of the last written Word in Flash (failing Flash address if R0 is not equal to zero)	Undefined		Unchanged
Erasing	Error code	Undefined			Unchanged
After status read	Error code	Flash embedded rev MSByte = major release LSByte = minor revision	Circuit identifiers : R2 = #0787h R3 = #0101h for this device		Unchanged

Note: The Flash Embedded STEAK Algorithms require at least **50 words** on the Internal System Stack for proper operation. The program itself verifies that there is enough free space on the System Stack before performing a programming or erasing operation, by computing the Word number between Stack Pointer (SP) and Stack Overflow register (STKOV).
The MDH, MDL and MDC register content are modified.
Registers R0 to R4 are used as Input Data for STEAK, and are modified as explained above (Return Values).
Registers R5 to R15 are used internally by STEAK, but preserved on entry and restore on exit of STEAK.
IT IS VERY IMPORTANT TO TAKE INTO ACCOUNT THE FACT THAT STEAK USES UP TO 50 WORDS ON THE SYSTEM STACK. TO PREVENT ANY ABNORMAL SITUATION, IT IS VERY IMPORTANT TO INITIALIZE CORRECTLY THE STACK SIZE TO AT LEAST 64 WORDS, AND TO CORRECTLY INITIALIZE REGISTER STKOV.

6.1 - Instruction Set Summary

The Table 8 lists the instructions of the ST10F168. The various addressing modes, instruction operation, parameters for conditional execution of instructions, opcodes and a detailed description of each instruction can be found in the “ST10 Family Programming Manual”.

Table 8 : Instruction set summary

Mnemonic	Description	Bytes
ADD(B)	Add Word (Byte) operands	2 / 4
ADDC(B)	Add Word (Byte) operands with Carry	2 / 4
SUB(B)	Subtract Word (Byte) operands	2 / 4
SUBC(B)	Subtract Word (Byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16 x 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16 / 16-bit)	2
DIVL(U)	(Un)Signed long divide register MD by direct GPR (32 / 16-bit)	2
CPL(B)	Complement direct Word (Byte) GPR	2
NEG(B)	Negate direct Word (Byte) GPR	2
AND(B)	Bitwise AND, (Word / Byte operands)	2 / 4
OR(B)	Bitwise OR, (Word / Byte operands)	2 / 4
XOR(B)	Bitwise XOR, (Word / Byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND / OR / XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high / low Byte of bit-addressable direct Word memory with immediate data	4
CMP(B)	Compare Word (Byte) operands	2 / 4
CMPD1/2	Compare Word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare Word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct Word GPR and store result in direct Word GPR	2
SHL/SHR	Shift left / right direct Word GPR	2
ROL/ROR	Rotate left / right direct Word GPR	2
ASHR	Arithmetic (sign bit) shift right direct Word GPR	2
MOV(B)	Move Word (Byte) data	2 / 4
MOVBS	Move Byte operand to Word operand with sign extension	2 / 4
MOVBZ	Move Byte operand to Word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute / indirect / relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4

Table 8 : Instruction set summary

Mnemonic	Description	Bytes
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute / indirect / relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct Word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push / pop direct Word register onto / from system stack	2
SCXT	Push direct Word register onto system stack and update register with Word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct Word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on $\overline{\text{RSTOUT}}$-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

7 - EXTERNAL BUS CONTROLLER

All external memory accesses are performed by the on-chip external bus controller. The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes :

– 16 / 18 / 20 / 24-bit addresses and 16-bit data, demultiplexed.
– 16 / 18 / 20 / 24-bit addresses and 16-bit data, multiplexed.
– 16 / 18 / 20 / 24-bit addresses and 8-bit data, multiplexed.
– 16 / 18 / 20 / 24-bit addresses and 8-bit data, demultiplexed.

In demultiplexed bus modes addresses are output on Port1 and data are input / output on Port0 or P0L, respectively. In the multiplexed bus modes both addresses and data use Port0 for input / output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read / write delay) are programmable giving the choice of a wide range of memories and external peripherals. Up to 4 independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a 'Ready' function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register SYSCON. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to'1' the slave mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1M Byte, 256K Byte or to 64K Byte. Port4 outputs all 8 address lines if an address space of 16M Byte is used, otherwise four, two or no address lines.

Chip select timing can be programmed. By default (after reset), the CSx lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the CSx lines can change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOLx in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOLx in the associated BUSCONx register.

Hardware traps are exceptions or error conditions that arise during run-time. They cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location).

The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any other program execution.

Hardware trap services cannot not be interrupted by standard interrupt or by PEC interrupts.

Table 10 shows all of the possible exceptions or error conditions that can arise during run-time :

Table 10 : Exceptions or error conditions that can arise during run-time

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions					
Hardware Reset		RESET	00'0000h	00h	III
Software Reset		RESET	00'0000h	00h	III
Watchdog Timer Overflow		RESET	00'0000h	00h	III
Class A Hardware Traps					
Non-Maskable Interrupt	NMI	NMITRAP	00'0008h	02h	II
Stack Overflow	STKOF	STOTRAP	00'0010h	04h	II
Stack Underflow	STKUF	STUTRAP	00'0018h	06h	II
Class B Hardware Traps					
Undefined Opcode	UNDOPC	BTRAP	00'0028h	0Ah	I
Protected Instruction Fault	PRTFLT	BTRAP	00'0028h	0Ah	I
Illegal Word Operand Access	ILLOPA	BTRAP	00'0028h	0Ah	I
Illegal Instruction Access	ILLINA	BTRAP	00'0028h	0Ah	I
Illegal External Bus Access	ILLBUS	BTRAP	00'0028h	0Ah	I
Reserved			[2Ch –3Ch]	[0Bh – 0Fh]	
Software Traps TRAP Instruction			Any [00'0000h– 00'01FCh] in steps of 4h	Any [00h – 7Fh]	Current CPU Priority

Table 12 : CAPCOM timer input frequencies, resolution and periods

f_{CPU} = 25MHz	Timer Input Selection TxI							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
f_{CPU} pre-scaler	8	16	32	64	128	256	512	1024
Input Frequency	3.125MHz	1.56MHz	781KHz	391KHz	195KHz	97.7KHz	48.8KHz	24.4KHz
Resolution	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs	40.96µs
Period	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s	2.68s

Table 13 : CAPCOM Channels Pin Assignement

CAPCOM Unit	**Channel**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
CAPCOM1	I/O	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8[1]	CC9[1]	CC10[1]	CC11[1]	CC12	CC13	CC14	CC15
	Port	2.0	2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	2.9	2.10	2.11	2.12	2.13	2.14	2.15
	Pin Number	47	48	49	50	51	52	53	54	57	58	59	60	61	62	63	64
CAPCOM2	I/O	CC16	CC17	CC18	CC19	CC20	CC21	CC22	CC23	CC24	CC25	CC26	CC27	CC28	CC29	CC30	CC31
	Port	8.0	8.1	8.2	8.3	8.4	8.5	8.6	8.7	1H.4	1H.5	1H.6	1H.7	7.4	7.5	7.6	7.7
	Pin Number	9	10	11	12	13	14	15	16	132	133	134	135	23	24	25	26

Note: 1. Input only.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT).

The overflows / underflows of timer T6 can also be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register.

The CAPREL register can capture the contents of T5 from an external signal transition on the corresponding port pin (CAPIN), and T5 may be optionally cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated on transitions of GPT1 timer T3 inputs T3IN and / or T3EUD. This is useful when T3 operates in Incremental Interface Mode.

Table 15 GPT2 timer input frequencies, resolution and periods lists the timer input frequencies, resolution and periods for each pre-scaler option at 25MHz CPU clock. This also applies to the Gated Timer Mode of T6 and to the auxiliary timer T5 in Timer and Gated Timer Mode.

Table 15 : GPT2 timer input frequencies, resolution and periods

f_{CPU} = 25MHz	Timer Input Selection T5I / T6I							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Pre-scaler Factor	4	8	16	32	64	128	256	512
Input Frequency	6.25MHz	3.125MHz	1.563MHz	781.3KHz	390KHz	195.3KHz	97.66KHz	48.83KHz
Resolution	160ns	320ns	640ns	1.28µs	2.56µs	5.12µs	10.24µs	20.48µs
Period	10.49ms	21.0ms	41.9ms	83.9ms	167ms	336ms	671ms	1.34s

Figure 6 : Block Diagram of GPT1

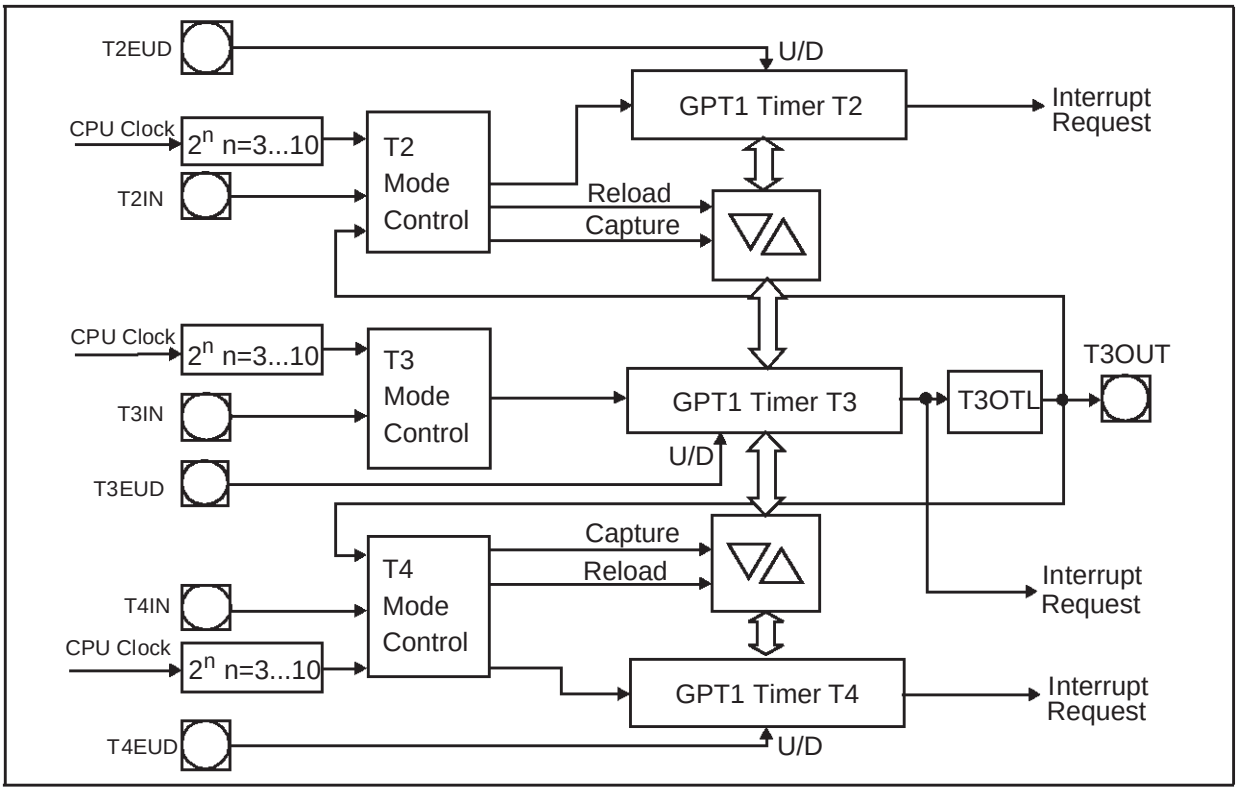
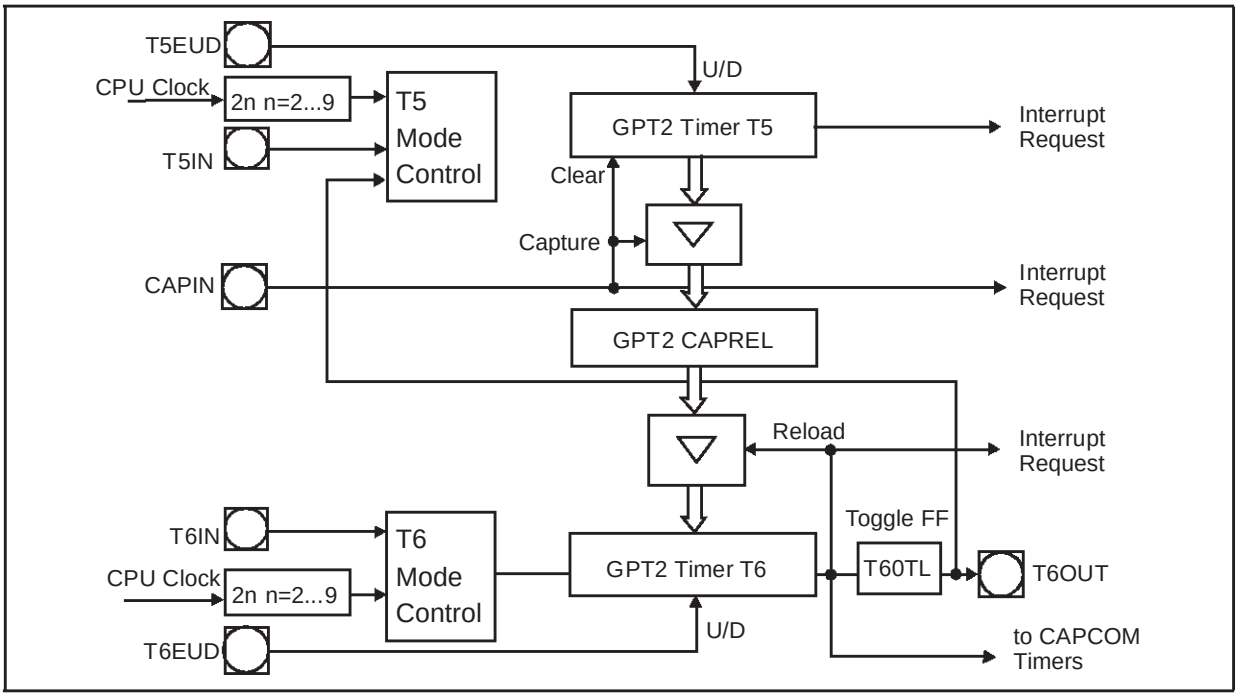


Figure 7 : Block Diagram of GPT2



13 - A/D CONVERTER

A10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit is integrated on-chip. The sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry.

Overrun error detection / protection is controlled by the ADDAT register. Either an interrupt request is generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended until the previous result has been read. For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the ST10F168 supports different conversion modes :

– **Single channel single conversion** : the analog level of the selected channel is sampled once and converted. The result of the conversion is stored in the ADDAT register.

– **Single channel continuous conversion** : the analog level of the selected channel is repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register.

– **Auto scan single conversion** : the analog level of the selected channels are sampled once and converted. After each conversion the result is stored in the ADDAT register. The data can be transfered to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.

– **Auto scan continuous conversion** : the analog level of the selected channels are repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register. The data can be transfered to the RAM by interrupt software management or using the powerfull Peripheral Event Controller data transfert.

– **Wait for ADDAT read mode** : when using continuous modes, in order to avoid to overwrite the result of the current conversion by the next one, the ADWR bit of ADCON control register must be activated. Then, until the ADDAT register is read, the new result is stored in a temporary buffer and the conversion is on hold.

– **Channel injection mode** : when using continuous modes, a selected channel can be converted in between without changing the current operating mode. The 10 bit data of the conversion are stored in ADRES field of ADDAT2. The current continuous mode remains active after the single conversion is completed.

The Table 17 ADC sample clock and conversion clock shows conversion clock and sample clock of the ADC unit. A complete conversion will take $14t_{CC} + 2t_{SC} + 4TCL$. This time includes the conversion it self, the sampling time and the time required to transfer the digital value to the result register. For example at 25MHz of CPU clock, the minimum complete conversion time is 7.76µs.

The A/D converter provides automatic offset and linearity self calibration. The calibration operation is performed in two ways :

– A full calibration sequence is performed after a reset and lasts 1.25ms minimum (at 25MHz CPU clock). During this time, the ADBSY flag is set to indicate the operation. Normal conversion can be performed during this time. The duration of the calibration sequence is then extended by the time consumed by the conversions.
Note : After a power-on reset, the total unadjusted error (TUE) of the ADC might be worse than ±2LSB (max. ±4LSB). During the full calibration sequence, the TUE is constantly improved until at the end of the cycle, TUE is within the specified limits of ±2LSB.

– One calibration cycle is performed after each conversion : each calibration cycle takes 4 ADC clock cycles. These operation cycles ensure constant updating of the ADC accuracy, compensating changing operating conditions.

Table 17 : ADC sample clock and conversion clock

ADCTC	Conversion Clock t_{CC}		ADSTC	Sample Clock t_{SC}	
	TCL[1] = 1/2 x f_{XTAL}	At f_{CPU} = 25MHz		t_{SC} =	At f_{CPU} = 25MHz
00	TCL x 24	0.48µs	00	t_{CC}	0.48µs [2]
01	Reserved, do not use	Reserved	01	t_{CC} x 2	0.96µs [2]
10	TCL x 96	1.92µs	10	t_{CC} x 4	1.92µs [2]
11	TCL x 48	0.96µs	11	t_{CC} x 8	3.84µs [2]

Notes: 1. See Section 20.5.5 - Direct Drive on page 55.
2. t_{CC} = TCL x 24.

17 - SYSTEM RESET

Table 21 : Reset event definition

Reset Source	Short-cut	Conditions
Power-on reset	PONR	Power-on
Long Hardware reset (synchronous & asynchronous)	LHWR	t_{RSTIN} > 1032 TCL
Short Hardware reset (synchronous reset)	SHWR	4 TCL < t_{RSTIN} ≤ 1032 TCL
Watchdog Timer reset	WDTR	WDT overflow
Software reset	SWR	SRST execution

System reset initializes the MCU in a predefined state. There are five ways to activate a reset state. The system start-up configuration is different for each case as shown in Table 21.

17.1 - Asynchronous Reset (Long Hardware Reset)

An asynchronous reset is triggered when $\overline{RSTIN}$ pin is pulled low while V_{PP} pin is at low level. Then the MCU is immediately forced in reset default state. It pulls low $\overline{RSTOUT}$ pin, it cancels pending internal hold states if any, it waits for any internal access cycles to finish, it aborts external bus cycle, it switches buses (data, address and control signals) and I/O pin drivers to high-impedance, it pulls high Port0 pins and the reset sequence starts.

Power-on Reset

The asynchronous reset must be used during the power-on of the MCU. Depending on crystal frequency, the on-chip oscillator needs about 10ms to 50ms to stabilize. The logic of the MCU does not need a stabilized clock signal to detect an asynchronous reset, so it is suitable for power-on conditions. To ensure a proper reset sequence, the $\overline{RSTIN}$ pin and the V_{PP} pin must be held at low level until the MCU clock signal is stabilized and the system configuration value on Port0 is settled.

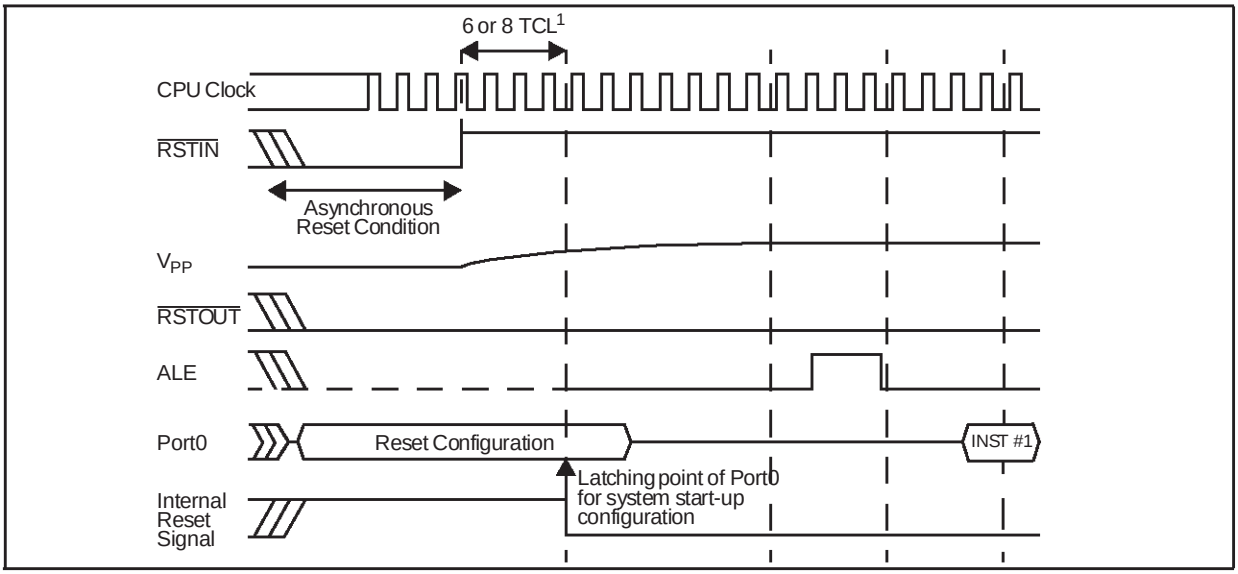
Hardware Reset

The asynchronous reset must be used to recover from catastrophic situations of the application. It may be triggerred by the hardware of the application. Internal hardware logic and application circuitry are described in Reset circuitry chapter and Figures 12, 13 and 14.

Exit of Asynchrounous Reset State

When the $\overline{RSTIN}$ pin is pulled high, the MCU restarts. The system configuration is latched from Port0 and ALE, $\overline{RD}$ and $\overline{R/W}$ pins are driven to their inactive level. The MCU starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. Timing of asynchronous reset sequence are summarized in Figure 9.

Figure 9 : Asynchronous Reset Timing



Note: 1. $\overline{RSTIN}$ rising edge to internal latch of Port0 is 3CPU clock cycles (6 TCL) if the PLL is bypassed and the prescaler is on ($f_{CPU} = f_{XTAL} / 2$), else it is 4 CPU clock cycles (8 TCL).

The simplest way to reset the ST10F168 is to insert a capacitor C1 between $\overline{RSTIN}$ pin and V_{SS}, and a capacitor between V_{PP} pin and V_{SS} (C0) with a pullup resistor R0 between V_{PP} pin and V_{CC}. The input $\overline{RSTIN}$ provides an internal pullup device equalling a resistor of 50kΩ to 150kΩ (the minimum reset time must be determined by the lowest value). Select C1 that produce a sufficient discharge time to permit the internal or external oscillator and / or internal PLL to stabilize.

To insure correct power-up reset with controlled supply current consumption, specially if clock signal requires a long period of time to stabilized, an asynchronous hardware reset is required during power-up. It is recommended to connect the external R0C0 circuit shown in Figure 12 to the V_{PP} pin. On power-up, the logical low level on V_{PP} pin forces an asynchronous harware reset when $\overline{RSTIN}$ is asserted.

The external pullup R0 will then charge the capacitor C0. Note that an internal pulldown device on V_{PP} pin is turned on when $\overline{RSTIN}$ pin is low, and causes the external capacitor (C0) to begin discharging at a typical rate of 100µA to 200µA. With this mechanism, after power-up reset, short low pulses applied on $\overline{RSTIN}$ produce synchronous hardware reset. If $\overline{RSTIN}$ is asserted longer than the time needed for C0 to be discharged by the internal pulldown device, then the device is forced in an asynchronous reset. This mechanism insures recovery from very catastrophic failure.

Figure 12 : Minimum External Reset Circuitry

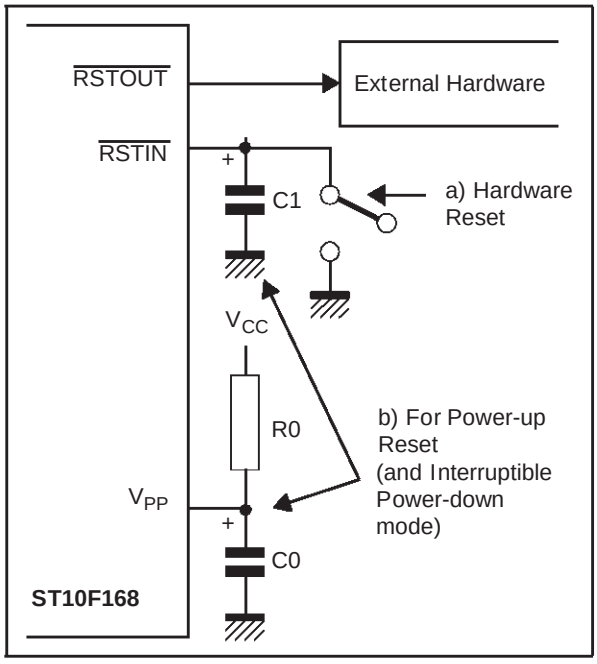


Figure 13 : Internal (simplified) Reset Circuitry

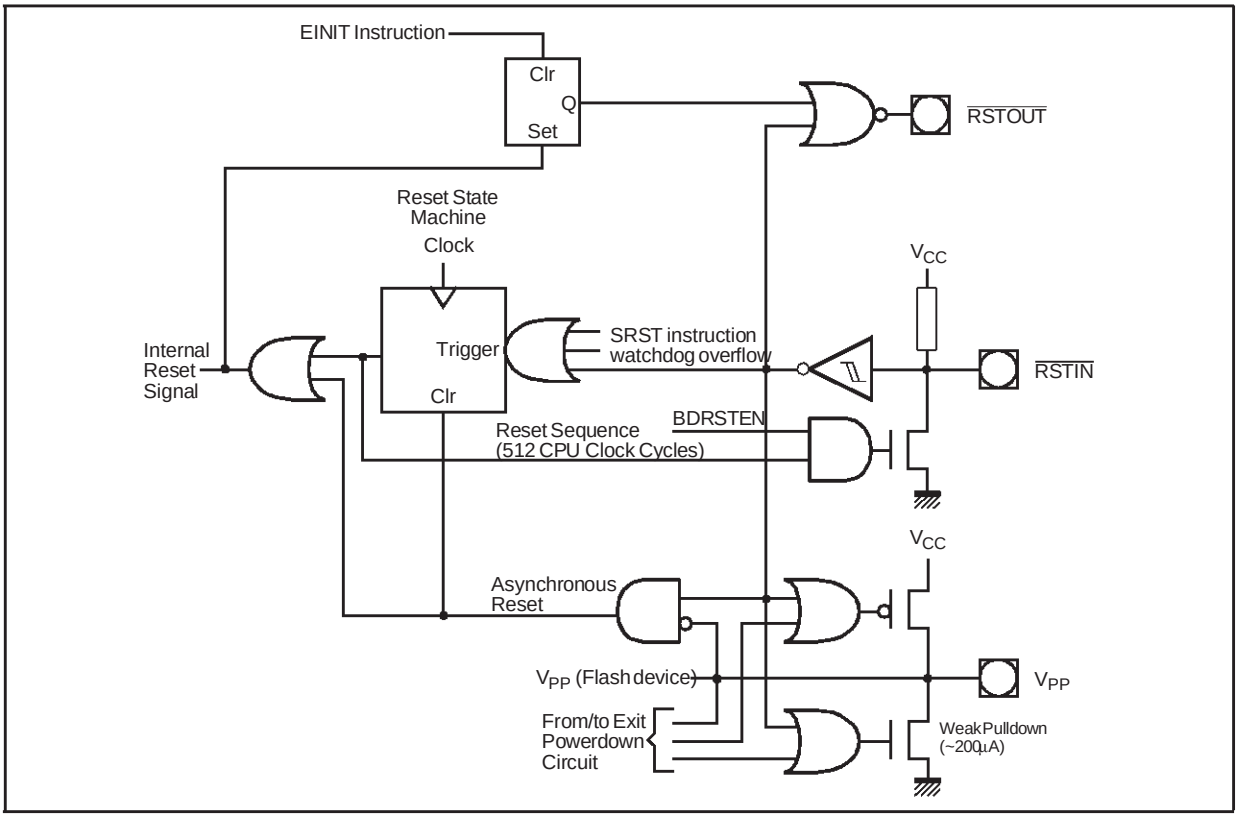


Table 22 : Special Function Registers listed by name

Name	Physical address	8-bit address	Description	Reset value
CC9IC b	FF8Ah	C5h	CAPCOM Register 9 Interrupt Control Register	0000h
CC10	FE94h	4Ah	CAPCOM Register 10	0000h
CC10IC b	FF8Ch	C6h	CAPCOM Register 10 Interrupt Control Register	0000h
CC11	FE96h	4Bh	CAPCOM Register 11	0000h
CC11IC b	FF8Eh	C7h	CAPCOM Register 11 Interrupt Control Register	0000h
CC12	FE98h	4Ch	CAPCOM Register 12	0000h
CC12IC b	FF90h	C8h	CAPCOM Register 12 Interrupt Control Register	0000h
CC13	FE9Ah	4Dh	CAPCOM Register 13	0000h
CC13IC b	FF92h	C9h	CAPCOM Register 13 Interrupt Control Register	0000h
CC14	FE9Ch	4Eh	CAPCOM Register 14	0000h
CC14IC b	FF94h	CAh	CAPCOM Register 14 Interrupt Control Register	0000h
CC15	FE9Eh	4Fh	CAPCOM Register 15	0000h
CC15IC b	FF96h	CBh	CAPCOM Register 15 Interrupt Control Register	0000h
CC16	FE60h	30h	CAPCOM Register 16	0000h
CC16IC b	F160h E	B0h	CAPCOM Register 16 Interrupt Control Register	0000h
CC17	FE62h	31h	CAPCOM Register 17	0000h
CC17IC b	F162h E	B1h	CAPCOM Register 17 Interrupt Control Register	0000h
CC18	FE64h	32h	CAPCOM Register 18	0000h
CC18IC b	F164h E	B2h	CAPCOM Register 18 Interrupt Control Register	0000h
CC19	FE66h	33h	CAPCOM Register 19	0000h
CC19IC b	F166h E	B3h	CAPCOM Register 19 Interrupt Control Register	0000h
CC20	FE68h	34h	CAPCOM Register 20	0000h
CC20IC b	F168h E	B4h	CAPCOM Register 20 Interrupt Control Register	0000h
CC21	FE6Ah	35h	CAPCOM Register 21	0000h
CC21IC b	F16Ah E	B5h	CAPCOM Register 21 Interrupt Control Register	0000h
CC22	FE6Ch	36h	CAPCOM Register 22	0000h
CC22IC b	F16Ch E	B6h	CAPCOM Register 22 Interrupt Control Register	0000h
CC23	FE6Eh	37h	CAPCOM Register 23	0000h
CC23IC b	F16Eh E	B7h	CAPCOM Register 23 Interrupt Control Register	0000h
CC24	FE70h	38h	CAPCOM Register 24	0000h
CC24IC b	F170h E	B8h	CAPCOM Register 24 Interrupt Control Register	0000h
CC25	FE72h	39h	CAPCOM Register 25	0000h
CC25IC b	F172h E	B9h	CAPCOM Register 25 Interrupt Control Register	0000h
CC26	FE74h	3Ah	CAPCOM Register 26	0000h
CC26IC b	F174h E	BAh	CAPCOM Register 26 Interrupt Control Register	0000h
CC27	FE76h	3Bh	CAPCOM Register 27	0000h
CC27IC b	F176h E	BBh	CAPCOM Register 27 Interrupt Control Register	0000h
CC28	FE78h	3Ch	CAPCOM Register 28	0000h
CC28IC b	F178h E	BCh	CAPCOM Register 28 Interrupt Control Register	0000h
CC29	FE7Ah	3Dh	CAPCOM Register 29	0000h

20 - ELECTRICAL CHARACTERISTICS

20.1 - Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Voltage on V_{DD} pins with respect to ground[1]	-0.5, +6.5	V
V_{IO}	Voltage on any pin with respect to ground[1]	-0.5, (V_{DD} +0.5)	V
I_{OV}	Input Current on any pin during overload condition[1]	-10, +10	mA
I_{TOV}	Absolute Sum of all input currents during overload condition[1]	|100 mA|	mA
P_{tot}	Power Dissipation[1]	1.5	W
T_A	Ambient Temperature under bias for - Q6[1] Ambient Temperature under bias for - Q3[1]	-40, +85 -40, +125	°C °C
T_{stg}	Storage Temperature[1]	-65, +150	°C

Note: 1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

20.2 - Parameter Interpretation

The parameters listed in the following tables represent the characteristics of the ST10F168 and its demands on the system.

Where the ST10F168 logic provides signals with their respective timing characteristics, the symbol "**CC**" for Controller Characteristics is included in the "Symbol" column.

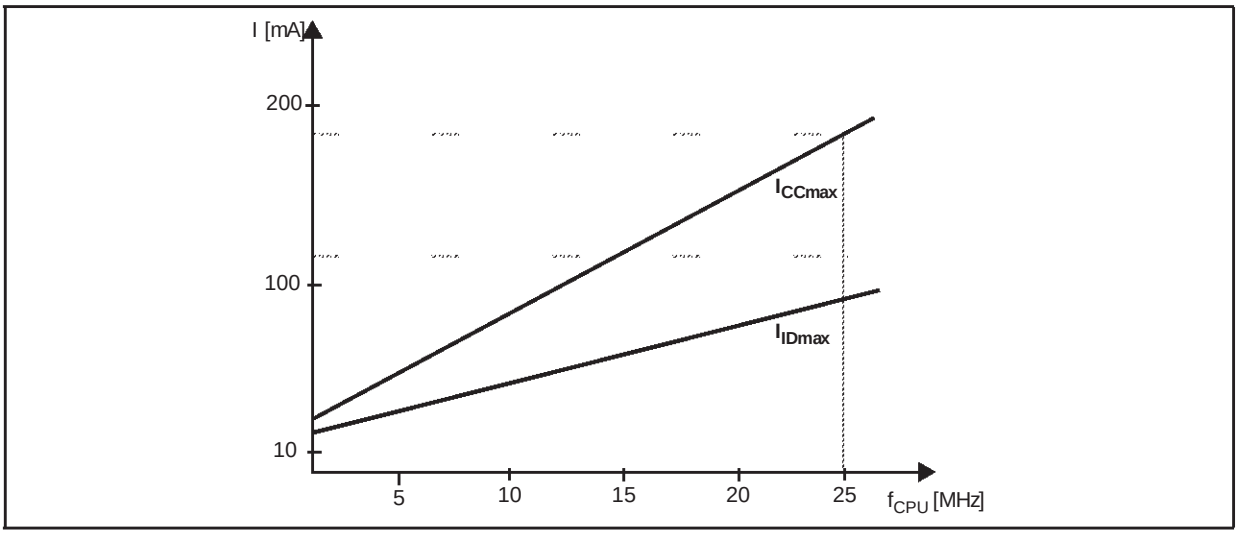
Where the external system must provide signals with their respective timing characteristics to the ST10F168, the symbol "**SR**" for System Requirement is included in the "Symbol" column.

20.3 - DC Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, Reset active, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, +125°C, unless otherwise specified.

Symbol		Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	SR	Input low voltage	–	– 0.5	0.2 V_{DD} – 0.1	V
V_{ILS}	SR	Input low voltage (special threshold)	–	– 0.5	2.0	V
V_{IH}	SR	Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	–	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	SR	Input high voltage $\overline{RSTIN}$	–	0.6 V_{DD}	V_{DD} + 0.5	V
V_{IH2}	SR	Input high voltage XTAL1	–	0.7 V_{DD}	V_{DD} + 0.5	V
V_{IHS}	SR	Input high voltage (special threshold)	–	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V
HYS		Input Hysteresis (special threshold)	–	300	-	mV
V_{OL}	CC	Output low voltage [1] (Port0, Port1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	I_{OL} = 2.4mA	–	0.45	V
V_{OL1}	CC	Output low voltage[1] (all other outputs)	I_{OL1} = 1.6mA	–	0.45	V
V_{OH}	CC	Output high voltage[1] (Port0, Port1, Port4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	I_{OH} = – 500µA I_{OH} = –2.4mA	0.9 V_{DD} 2.4	– –	V
V_{OH1}	CC	Output high voltage [1 2] (all other outputs)	I_{OH} = – 250µA I_{OH} = – 1.6mA	0.9 V_{DD} 2.4	– –	V V
I_{OZ1}	CC	Input leakage current (Port 5)	0V < V_{IN} < V_{DD}	–	±0.5	µA

Figure 15 : Supply / idle current as a function of operation frequency



20.4 - A/D Converter Characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, 4.0V ≤ V_{AREF} ≤ V_{DD} + 0.1V, V_{SS} - 0.1V ≤ V_{AGND} ≤ V_{SS} + 0.2V, Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40°C, +125°C, unless otherwise specified

Symbol		Parameter	Test Conditions	Min.	Max.	Unit
V_{AIN}	SR	Analog input voltage range	1 - 8	V_{AGND}	V_{AREF}	V
t_S	CC	Sample time	2 - 4	48 TCL	1 536 TCL	
t_C	CC	Conversion time	3 - 4	388 TCL	2 884 TCL	
TUE	CC	Total unadjusted error	5	–	± 2	LSB
R_{AREF}	SR	Internal resistance of reference voltage source	t_{CC} in [ns] 6 - 7	–	(t_{CC} / 165) - 0.25	kΩ
R_{ASRC}	SR	Internal resistance of analog source	t_S in [ns] 2 - 7	–	(t_S / 330) - 0.25	kΩ
C_{AIN}	CC	ADC input capacitance	7	–	33	pF

Notes: 1. V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000h or X3FFh, respectively.

2. During the t_S sample time the input capacitance C_{ain} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within the t_S sample time. After the end of the t_S sample time, changes of the analog input voltage have no effect on the conversion result. Values for the t_{SC} sample clock depend on the programming. Referring to the t_C conversion time formula of chapter 13, to the table 17 of page 33 and to the table below:

t_S min = 2 t_{SC} min = 2 t_{CC} min = 2 x 24 x TCL = 48 TCL

t_S max = 2 t_{SC} max = 2 x 8 t_{CC} max = 2 x 8 x 96 TCL = 1536 TCL

TCL is defined in section 20.5.5 at page 55.

3. The conversion time formula is:

t_C = 14 t_{CC} + t_S + 4 TCL (= 14 t_{CC} + 2 t_{SC} + 4 TCL)

The t_C parameter includes the t_S sample time, the time for determining the digital result and the time to load the result register with the result of the conversion. Values for the t_{CC} conversion clock depend on the programming. Referring to the table 17 of page 33 and to the table below:

t_C min = 14 t_{CC} min + t_S min + 4 TCL = 14 x 24 x TCL + 48 TCL + 4 TCL = 388 TCL

t_C max = 14 t_{CC} max + t_S max + 4 TCL = 14 x 96 TCL + 1536 TCL + 4 TCL = 2884 TCL

4. This parameter is fixed by ADC control logic.

5. TUE is tested at V_{AREF} = 5.0V, V_{AGND} = 0V, V_{CC} = 4.9V. It is guaranteed by design characterization for all other voltages within the defined voltage range. The specified TUE is guaranteed only if an overload condition (see Iov specification) occurs on maximum of 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10mA. During the reset calibration sequence the maximum TUE may be ±4 LSB.

20.5.4 - Prescaler Operation

When pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC Characteristics that refer to TCL therefore can be calculated using the period of f_{XTAL} for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

20.5.5 - Direct Drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

Therefore, the timings given in this chapter refer to the minimum TCL. This minimum value can be calculated by the following formula:

$$TCL_{min} = 1/f_{XTAL} \times DC_{min}$$

$$DC = \text{duty cycle}$$

For two consecutive TCLs, the deviation caused by the duty cycle of f_{XTAL} is compensated, so the duration of 2TCL is always $1/f_{XTAL}$. The minimum value TCL_{min} has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

Note: The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL (TCL_{max} = $1/f_{XTAL}$ x DC_{max}) instead of TCL_{min}.

If bit OWDDIS in the SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

20.5.6 - Oscillator Watchdog (OWD)

When the clock option selected is direct drive or direct drive with prescaler, in order to provide a fail safe mechanism in case of a loss of the external clock, an oscillator watchdog is implemented as an additional functionality of the PLL circuitry. This oscillator watchdog operates as follows :
After a reset, the Oscillator Watchdog is enabled by default. To disable the OWD, the bit OWDDIS (bit 4 of SYSCON register) must be set.

When the OWD is enabled, the PLL runs on its free-running frequency, and increments the Oscillator Watchdog counter. On each transition of XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles). The CPU clock signal will be switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

20.5.7 - Phase Locked Loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock (see Table 23).

The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (i.e. f_{CPU} = f_{XTAL} x F). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCL.

The timings listed in the AC Characteristics that refer to TCL therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

20.5.9 - Memory Cycle Variables

The tables below use three variables which are derived from the BUSCONx registers and which represent the special characteristics of the programmed memory cycle. The following table describes how these variables are computed.

Symbol	Description	Values
t_A	ALE Extension	TCL x <ALECTL>
t_C	Memory Cycle Time wait states	2TCL x (15 - <MCTC>)
t_F	Memory Tristate Time	2TCL x (1 - <MTTC>)

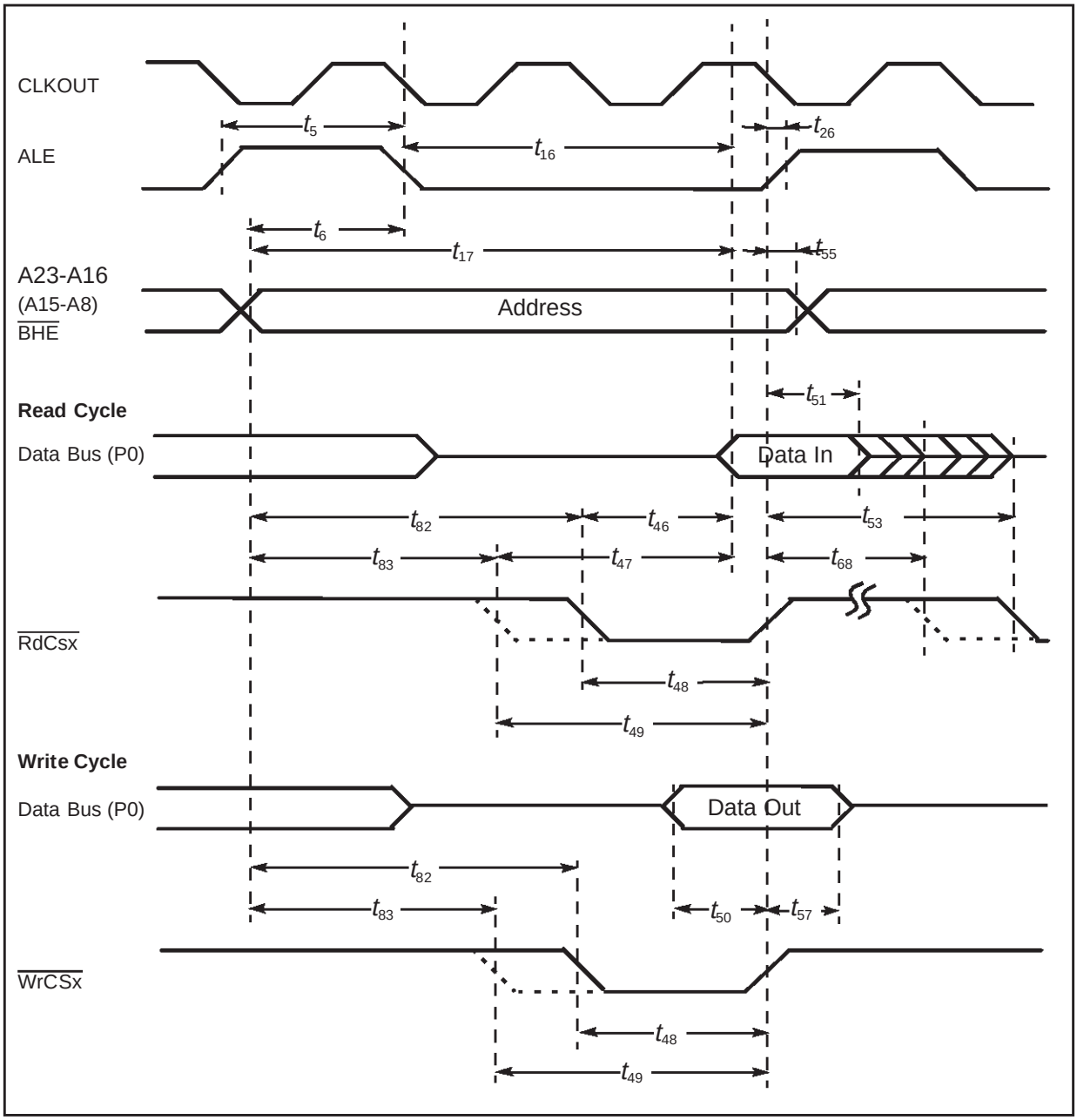
20.5.10 - Multiplexed Bus

V_{DD} = 5V ±10%, V_{SS} = 0V, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, + 125°C, C_L = 100pF, ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120ns at 25MHz CPU clock without wait states), unless otherwise specified.

Table 24 : Multiplexed bus characteristics

Symbol		Parameter	Maximum CPU Clock 25MHz		Variable CPU Clock 1/2 TCL = 1 to 25MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_5	CC	ALE high time	10 + t_A	–	TCL - 10 + t_A	–	ns
t_6	CC	Address setup to ALE	4 + t_A	–	TCL - 16+ t_A	–	ns
t_7	CC	Address hold after ALE	10 + t_A	–	TCL - 10 + t_A	–	ns
t_8	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	10 + t_A	–	TCL - 10 + t_A	–	ns
t_9	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	-10 + t_A	–	-10 + t_A	–	ns
t_{10}	CC	Address float after $\overline{RD}$, $\overline{WR}$ [1] (with RW-delay)	–	6	–	6	ns
t_{11}	CC	Address float after $\overline{RD}$, $\overline{WR}$ [1] (no RW-delay)	–	26	–	TCL + 6	ns
t_{12}	CC	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	30 + t_C	–	2TCL - 10 + t_C	–	ns
t_{13}	CC	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	50 + t_C	–	3TCL - 10 + t_C	–	ns
t_{14}	SR	$\overline{RD}$ to valid data in (with RW-delay)	–	20 + t_C	–	2TCL - 20+ t_C	ns
t_{15}	SR	$\overline{RD}$ to valid data in (no RW-delay)	–	40 + t_C	–	3TCL - 20+ t_C	ns
t_{16}	SR	ALE low to valid data in	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
t_{17}	SR	Address / Unlatched $\overline{CS}$ to valid data in	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
t_{18}	SR	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{19}	SR	Data float after $\overline{RD}$ [1]	–	26 + t_F	–	2TCL - 14 + t_F	ns
t_{22}	CC	Data valid to $\overline{WR}$	20 + t_C	–	2TCL - 20 + t_C	–	ns

Figure 28 : External Memory Cycle: demultiplexed bus, no read/write delay, extended ALE, read/write chip select



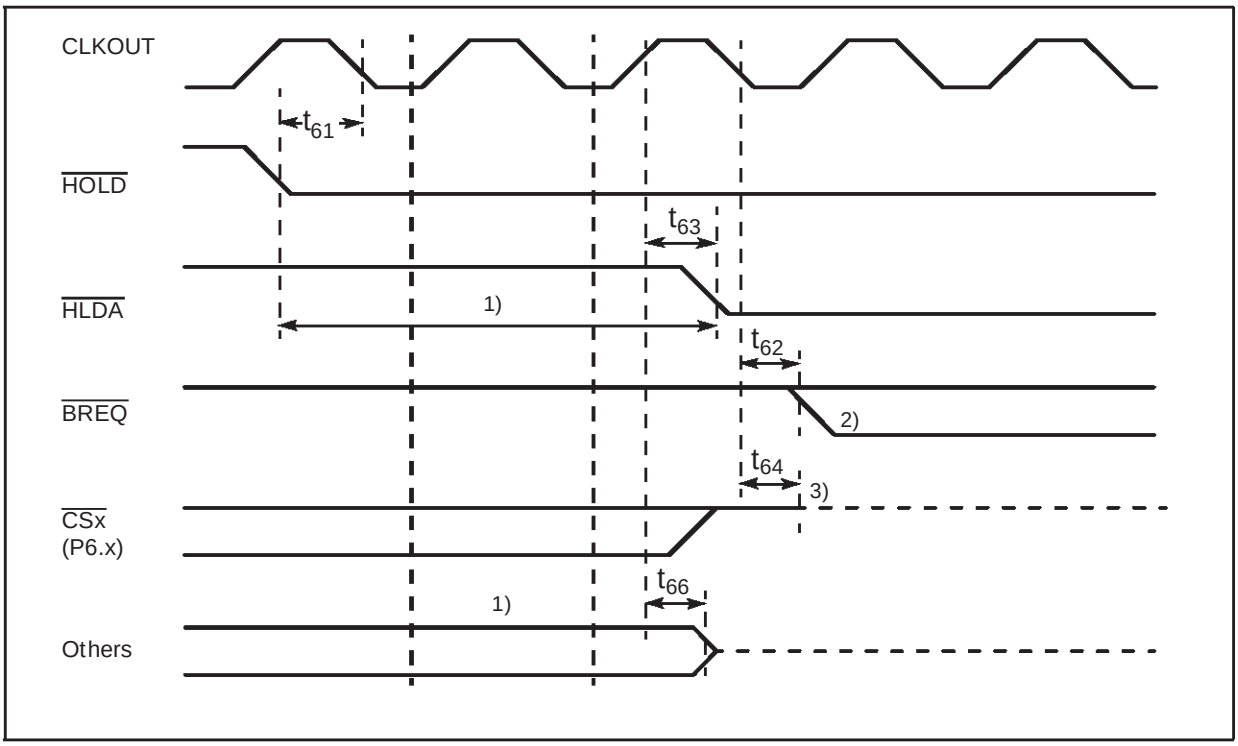
20.5.13 - External Bus Arbitration

V_{DD} = 5V ± 10%, V_{SS} = 0V, for Q6 version : T_A = -40, +85°C and for Q3 version T_A = -40, +125°C, C_L = 100pF, unless otherwise specified.

Symbol		Parameter	Max. CPU Clock 25MHz		Variable CPU Clock 1/2 TCL = 1 to 25MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_{61}	SR	$\overline{HOLD}$ input setup time to CLKOUT	20	–	20	–	ns
t_{62}	CC	CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	–	20	–	20	ns
t_{63}	CC	CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	–	20	–	20	ns
t_{64}	CC	$\overline{CSx}$ release [1]	–	20	–	20	ns
t_{65}	CC	$\overline{CSx}$ drive	-4	24	-4	24	ns
t_{66}	CC	Other signals release [1]	–	20	–	20	ns
t_{67}	CC	Other signals drive	-4	24	-4	24	ns

Note: 1. Partially tested, guaranted by design characterization.

Figure 30 : External bus arbitration, releasing the bus



Notes: 1. The ST10F168 will complete the currently running bus cycle before granting bus access.

2. This is the first possibility for $\overline{BREQ}$ to become active.

3. The $\overline{CS}$ outputs will be resistive high (pullup) after t_{64}.