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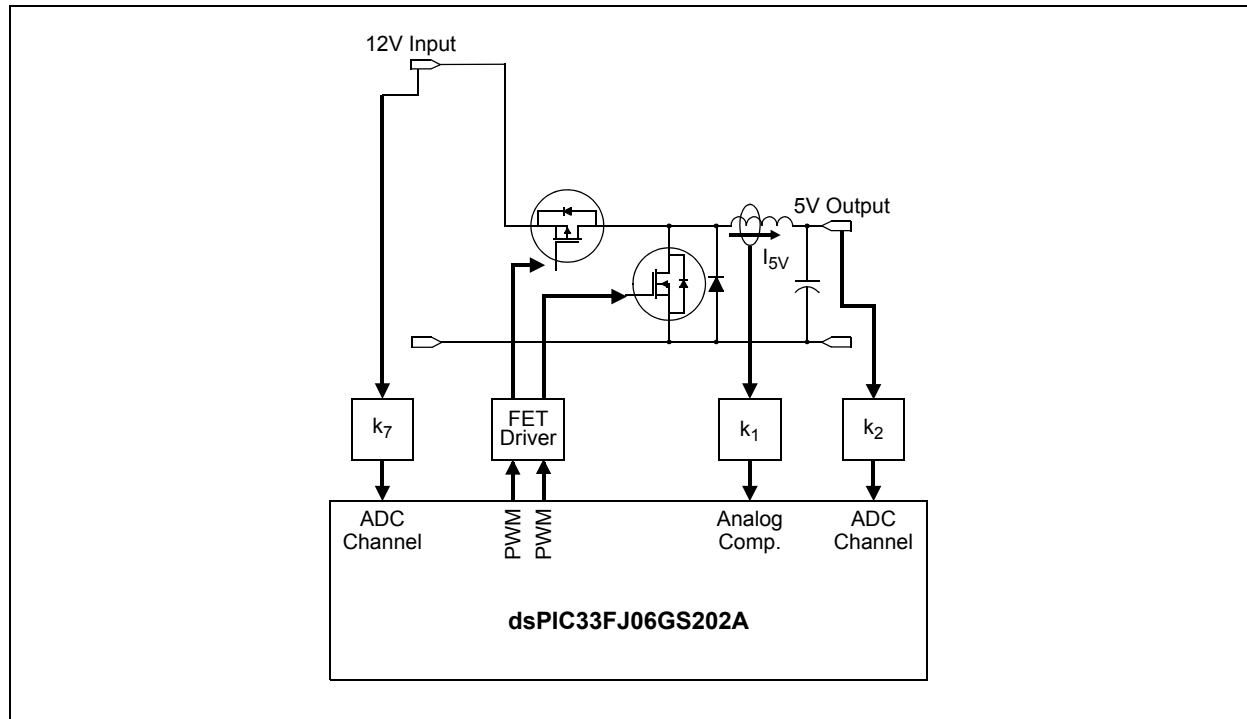
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

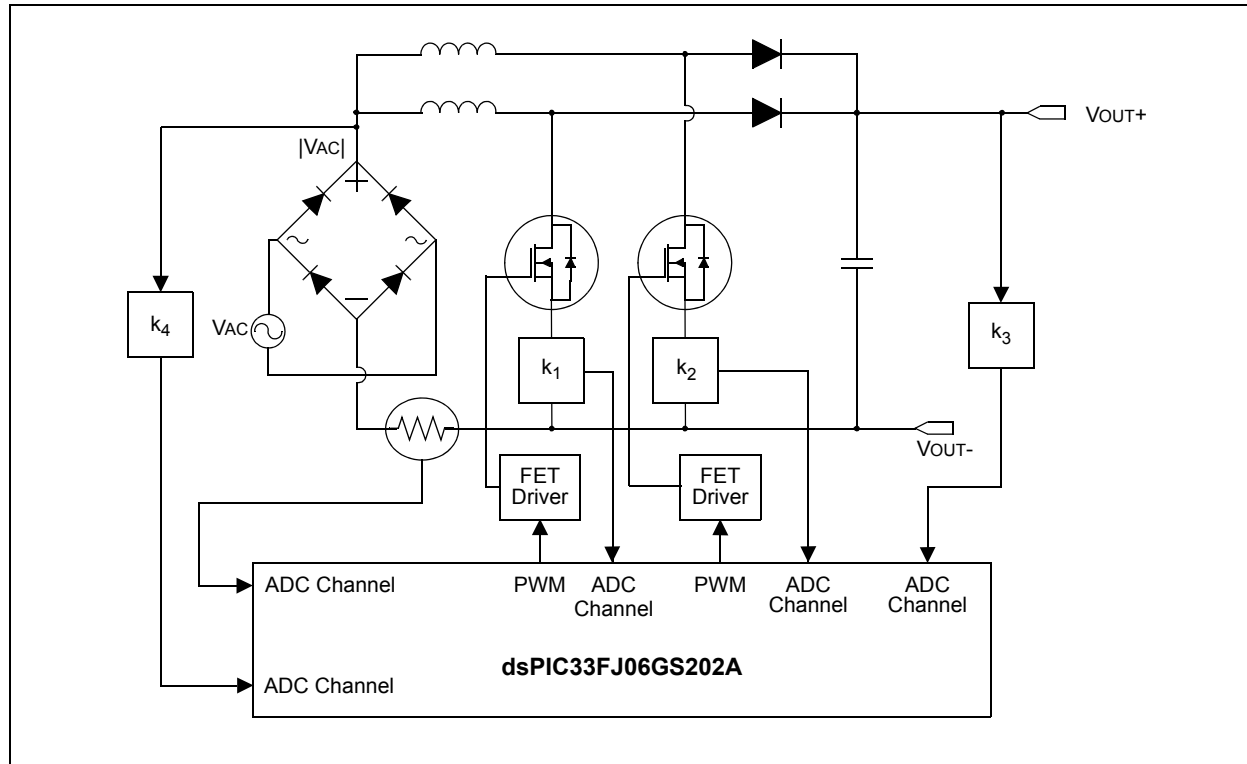
#### Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	6KB (2K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs001-e-so">https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs001-e-so</a>

**FIGURE 2-6: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER**



**FIGURE 2-7: INTERLEAVED PFC**



### 4.2.5 X AND Y DATA SPACES

The core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y data space is used in concert with the X data space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space.

All data memory writes, included in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

All Effective Addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes, or 32K words, though the implemented memory locations vary by device.

## **6.5 External Reset (EXTR)**

The external Reset is generated by driving the  $\overline{\text{MCLR}}$  pin low. The  $\overline{\text{MCLR}}$  pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to **Section 25.0 “Electrical Characteristics”** for minimum pulse width specifications. The external Reset ( $\overline{\text{MCLR}}$ ) pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the  $\overline{\text{MCLR}}$  Reset.

### **6.5.1 EXTERNAL SUPERVISORY CIRCUIT**

Many systems have external supervisory circuits that generate Reset signals to reset multiple devices in the system. This external Reset signal can be directly connected to the  $\overline{\text{MCLR}}$  pin to reset the device when the rest of the system is reset.

### **6.5.2 INTERNAL SUPERVISORY CIRCUIT**

When using the internal power supervisory circuit to reset the device, the external Reset pin ( $\overline{\text{MCLR}}$ ) should be tied directly or resistively to VDD. In this case, the  $\overline{\text{MCLR}}$  pin will not be used to generate a Reset. The external Reset pin ( $\overline{\text{MCLR}}$ ) does not have an internal pull-up and must not be left unconnected.

## **6.6 Software RESET Instruction (SWR)**

Whenever the RESET instruction is executed, the device will assert  $\overline{\text{SYSRST}}$ , placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the RESET instruction will still remain.  $\overline{\text{SYSRST}}$  is released at the next instruction cycle and the Reset vector fetch will commence.

The Software Reset (SWR) flag (instruction) in the Reset Control register (RCON<6>) is set to indicate the software Reset.

## **6.7 Watchdog Time-out Reset (WDTO)**

Whenever a Watchdog Timer time-out occurs, the device will asynchronously assert  $\overline{\text{SYSRST}}$ . The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out (WDTO) flag in the Reset Control (RCON<4>) register is set to indicate the Watchdog Timer Reset. Refer to **Section 22.4 “Watchdog Timer (WDT)”** for more information on Watchdog Reset.

## **6.8 Trap Conflict Reset**

If a lower priority hard trap occurs, while a higher priority trap is being processed, a hard Trap Conflict Reset occurs. The hard traps include exceptions of Priority Level 13 through Level 15, inclusive. The address error (Level 13) and oscillator error (Level 14) traps fall into this category.

The Trap Reset (TRAPR) flag in the Reset Control register (RCON<15>) is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 “Interrupt Controller”** for more information on Trap Conflict Resets.

## **6.9 Illegal Condition Device Reset**

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The illegal opcode or Uninitialized W Access Reset (IOPUWR) flag in the Reset Control register (RCON<14>) is set to indicate the illegal condition device Reset.

### **6.9.1 ILLEGAL OPCODE RESET**

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 0x3F, which is an illegal opcode value.

### **6.9.2 UNINITIALIZED W REGISTER RESET**

Any attempt to use the uninitialized W register as an Address Pointer will Reset the device. The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to.

## dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

### REGISTER 7-9: IFS5: INTERRUPT FLAG STATUS REGISTER 5

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
PWM2IF <sup>(1)</sup>	PWM1IF	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	JTAGIF
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15      **PWM2IF:** PWM2 Interrupt Flag Status bit<sup>(1)</sup>

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 14      **PWM1IF:** PWM1 Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 13-1    **Unimplemented:** Read as '0'

bit 0        **JTAGIF:** JTAG Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

**Note 1:** This bit is not implemented in dsPIC33FJ06GS001/101A devices.

# dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

## REGISTER 7-17: IEC6: INTERRUPT ENABLE CONTROL REGISTER 6

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
ADCP1IE	ADCP0IE	—	—	—	—	—	—
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
AC2IE <sup>(1)</sup>	—	—	—	—	—	PWM4IE <sup>(2)</sup>	—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15      **ADCP1IE:** ADC Pair 1 Conversion Done Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 14      **ADCP0IE:** ADC Pair 0 Conversion Done Interrupt Enable bit

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 13-8      **Unimplemented:** Read as '0'

bit 7      **AC2IE:** Analog Comparator 2 Interrupt Enable bit<sup>(1)</sup>

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 6-2      **Unimplemented:** Read as '0'

bit 1      **PWM4IE:** PWM4 Interrupt Enable bit<sup>(2)</sup>

1 = Interrupt request is enabled

0 = Interrupt request is not enabled

bit 0      **Unimplemented:** Read as '0'

**Note 1:** This bit is not implemented in dsPIC33FJ06GS101A/102A devices.

**2:** This bit is not implemented in dsPIC33FJ06GS102A/202A devices.

## dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

### REGISTER 7-20: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	T2IP<2:0>			—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'bit 14-12 **T2IP<2:0>:** Timer2 Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

- 
- 
- 

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 11-0 **Unimplemented:** Read as '0'

## dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

### REGISTER 7-22: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	ADIP<2:0>			—	U1TXIP<2:0> <sup>(1)</sup>		
bit 7				bit 0			

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7      **Unimplemented:** Read as '0'

bit 6-4      **ADIP<2:0>:** ADC1 Conversion Complete Interrupt Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3      **Unimplemented:** Read as '0'

bit 2-0      **U1TXIP<2:0>:** UART1 Transmitter Interrupt Priority bits<sup>(1)</sup>

111 = Interrupt is Priority 7 (highest priority interrupt)

•  
•  
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

**Note 1:** These bits are not implemented in the dsPIC33FJ06GS001 device.



## dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

### REGISTER 7-30: IPC24: INTERRUPT PRIORITY CONTROL REGISTER 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	PWM4IP <sup>(1)</sup>			—	—	—	—
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'bit 6-4 **PWM4IP<2:0>:** PWM4 Interrupt Priority bits<sup>(1)</sup>

111 = Interrupt is Priority 7 (highest priority)

- 
- 
- 

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'**Note 1:** These bits are not implemented in dsPIC33FJ06GS102A/202A devices.

## REGISTER 7-35: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR<3:0>			
bit 15				bit 8			

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM<6:0>						
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits

1111 = CPU Interrupt Priority Level is 15

•

•

•

0001 = CPU Interrupt Priority Level is 1

0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt bits

0111111 = Interrupt vector pending is Number 135

•

•

•

0000001 = Interrupt vector pending is Number 9

0000000 = Interrupt vector pending is Number 8

## 8.0 OSCILLATOR CONFIGURATION

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 42. "Oscillator (Part IV)"** (DS70307) in the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip website ([www.microchip.com](http://www.microchip.com)).

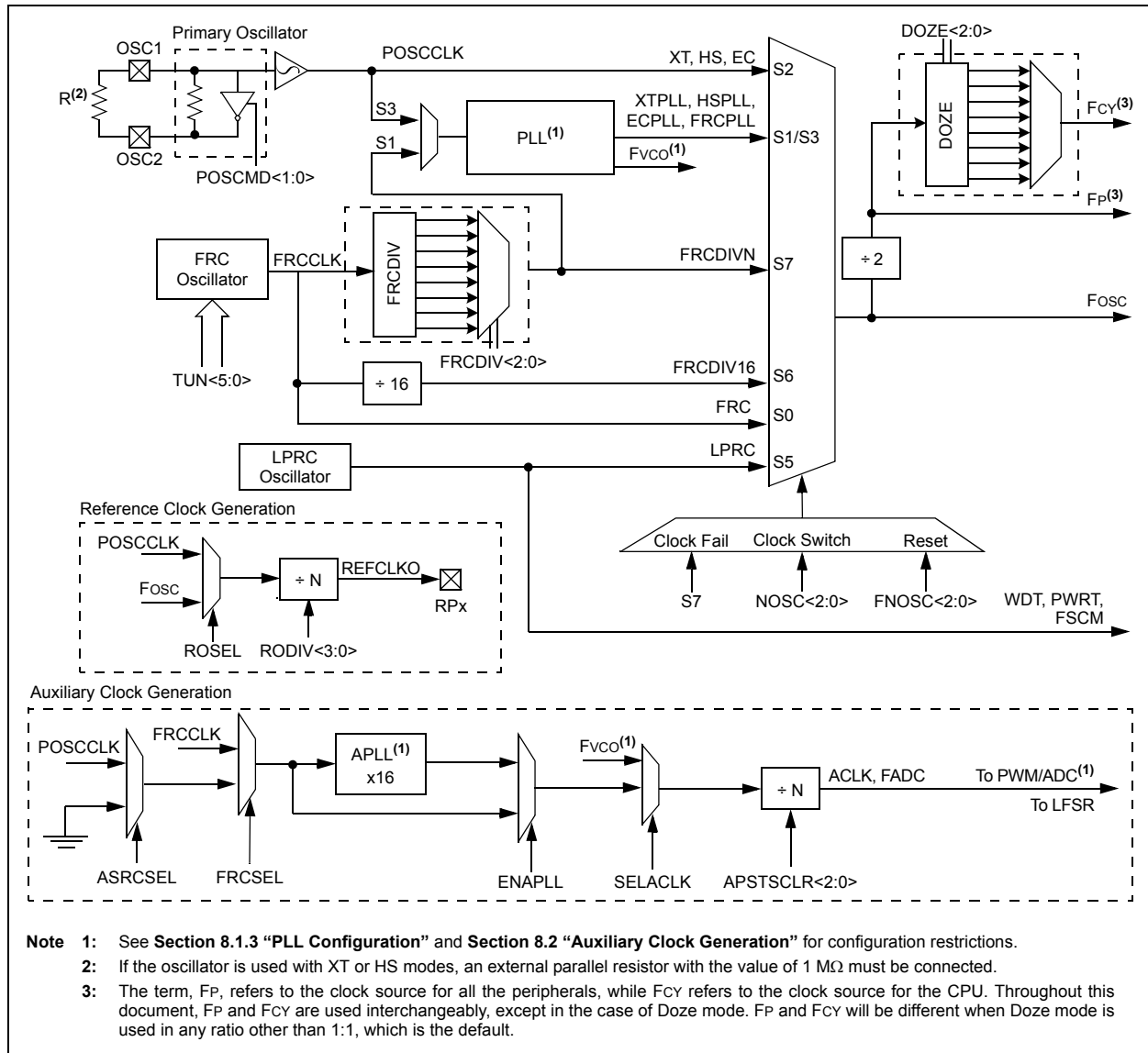
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The oscillator system provides:

- External and internal oscillator options as clock sources
- An on-chip Phase Lock Loop (PLL) to scale the internal operating frequency to the required system clock frequency
- An internal FRC oscillator that can also be used with the PLL, thereby allowing full-speed operation without any external clock generation hardware
- Clock switching between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- An Oscillator Control register (OSCCON)
- Nonvolatile Configuration bits for main oscillator selection
- An auxiliary PLL for ADC and PWM

A simplified diagram of the oscillator system is shown in Figure 8-1.

**FIGURE 8-1: OSCILLATOR SYSTEM DIAGRAM**



## 9.0 POWER-SAVING FEATURES

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. “Watchdog Timer (WDT) and Power-Saving Modes”** (DS70196) in the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

These devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. Devices can manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

### 9.1 Clock Frequency and Clock Switching

These devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC<2:0> bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 8.0 “Oscillator Configuration”**.

#### EXAMPLE 9-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV #IDLE_MODE      ; Put the device into IDLE mode
```

## 9.2 Instruction-Based Power-Saving Modes

The devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 9-1.

**Note:** SLEEP\_MODE and IDLE\_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake-up.

### 9.2.1 SLEEP MODE

The following occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate. This includes items, such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device will wake-up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

## 10.6.2.3 Virtual Pins

Four virtual RPn pins (RP32, RP33, RP34 and RP35) are supported, which are identical in functionality to all other RPn pins, with the exception of pinouts. These four pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP32 and the PWM Fault input can be configured for RP32 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

## 10.6.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. dsPIC33F devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit pin select lock

### 10.6.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

**Note:** MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:

```
__builtin_write_OSCCONL(value)  
__builtin_write_OSCCONH(value)
```

See the MPLAB C30 Help files for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence, followed by an update to all control registers, then locked with a second lock sequence.

### 10.6.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset will be triggered.

### 10.6.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC<5>) Configuration bit blocks the IOLOCK bit from being cleared, after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute and the Peripheral Pin Select Control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

**REGISTER 10-7: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18**

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U1CTSR<5:0> <sup>(1)</sup>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U1RXR<5:0> <sup>(1)</sup>					
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **U1CTSR<5:0>:** Assign UART1 Clear-to-Send (U1CTS) to the Corresponding RPn Pin bits<sup>(1)</sup>

111111 = Input tied to Vss

100011 = Input tied to RP35

100010 = Input tied to RP34

100001 = Input tied to RP33

100000 = Input tied to RP32

•

•

•

00000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **U1RXR<5:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits<sup>(1)</sup>

111111 = Input tied to Vss

100011 = Input tied to RP35

100010 = Input tied to RP34

100001 = Input tied to RP33

100000 = Input tied to RP32

•

•

•

00000 = Input tied to RP0

**Note 1:** These bits are not implemented in the dsPIC33FJ06GS001 device.

## 13.1 Input Capture Registers

**REGISTER 13-1: IC1CON: INPUT CAPTURE 1 CONTROL REGISTER**

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR <sup>(1)</sup>	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

<b>Legend:</b>	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-14      **Unimplemented:** Read as '0'
- bit 13      **ICSIDL:** Input Capture Module Stop in Idle Control bit  
1 = Input capture module halts in CPU Idle mode  
0 = Input capture module continues to operate in CPU Idle mode
- bit 12-8      **Unimplemented:** Read as '0'
- bit 7      **ICTMR:** Input Capture Timer Select bit<sup>(1)</sup>  
1 = TMR2 contents are captured on capture event  
0 = Reserved
- bit 6-5      **ICI<1:0>:** Select Number of Captures per Interrupt bits  
11 = Interrupt on every fourth capture event  
10 = Interrupt on every third capture event  
01 = Interrupt on every second capture event  
00 = Interrupt on every capture event
- bit 4      **ICOV:** Input Capture Overflow Status Flag bit (read-only)  
1 = Input capture overflow occurred  
0 = No input capture overflow occurred
- bit 3      **ICBNE:** Input Capture Buffer Empty Status bit (read-only)  
1 = Input capture buffer is not empty, at least one more capture value can be read  
0 = Input capture buffer is empty
- bit 2-0      **ICM<2:0>:** Input Capture Mode Select bits  
111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode. Rising edge detect only; all other control bits are not applicable.  
110 = Unused (module disabled)  
101 = Capture mode, every 16th rising edge  
100 = Capture mode, every 4th rising edge  
011 = Capture mode, every rising edge  
010 = Capture mode, every falling edge  
001 = Capture mode, every edge (rising and falling). ICI<1:0> bits do not control interrupt generation for this mode.  
000 = Input capture module is turned off

**Note 1:** This bit is not available in dsPIC33FJ06GS001/101A/102A devices.

## 22.4 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

### 22.4.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit (FWDT<4>). With a 32 kHz input, the prescaler yields a nominal WDT time-out period (TWDT) of 1 ms in 5-bit mode or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC<2:0> bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

**Note:** The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

### 22.4.2 SLEEP AND IDLE MODES

If the WDT is enabled, it will continue to run during Sleep or Idle modes. When the WDT time-out occurs, the device will wake the device and code execution will continue from where the PWRSAV instruction was executed. The corresponding SLEEP bit (RCON<3>) or IDLE bit (RCON<2>) will need to be cleared in software after the device wakes up.

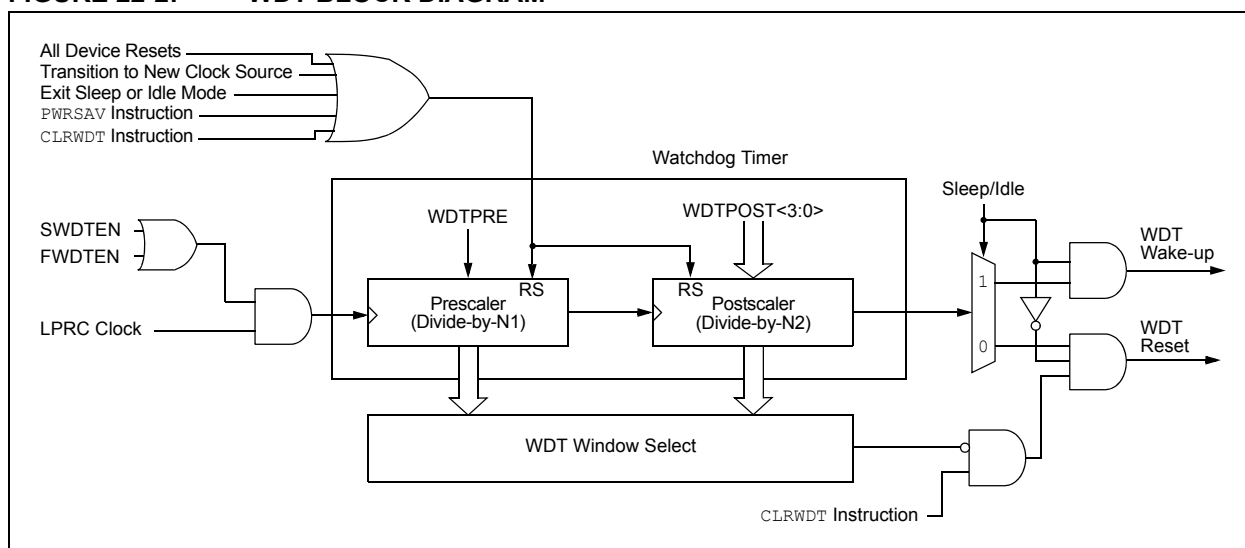
### 22.4.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register (FWDT<7>). When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

**FIGURE 22-2: WDT BLOCK DIAGRAM**





## **24.0 DEVELOPMENT SUPPORT**

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C® for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICKit™ 3 Debug Express
- Device Programmers
  - PICKit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

## **24.1 MPLAB Integrated Development Environment Software**

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

# dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

**TABLE 25-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)		
			Operating temperature    -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Param.	Typical <sup>(1)</sup>	Max.	Units	Conditions	
Operating Current (IDD) <sup>(2)</sup>					
DC20d	15	23	mA	-40°C	3.3V  10 MIPS
DC20a	15	23	mA	+25°C	
DC20b	15	23	mA	+85°C	
DC20c	15	23	mA	+125°C	
DC21d	23	34	mA	-40°C	3.3V  16 MIPS <sup>(3)</sup>
DC21a	23	34	mA	+25°C	
DC21b	23	34	mA	+85°C	
DC21c	23	34	mA	+125°C	
DC22d	25	38	mA	-40°C	3.3V  20 MIPS <sup>(3)</sup>
DC22a	25	38	mA	+25°C	
DC22b	25	38	mA	+85°C	
DC22c	25	38	mA	+125°C	
DC23d	34	51	mA	-40°C	3.3V  30 MIPS <sup>(3)</sup>
DC23a	34	51	mA	+25°C	
DC23b	34	51	mA	+85°C	
DC23c	34	51	mA	+125°C	
DC24d	43	64	mA	-40°C	3.3V  40 MIPS <sup>(3)</sup>
DC24a	43	64	mA	+25°C	
DC24b	43	64	mA	+85°C	
DC24c	43	64	mA	+125°C	
DC25d	83	125	mA	-40°C	3.3V  40 MIPS See <b>Note 2</b> , except PWM and ADC are operating at maximum speed (PTCON2 = 0x0000)
DC25a	83	125	mA	+25°C	
DC25b	83	125	mA	+85°C	
DC25c	83	125	mA	+125°C	

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

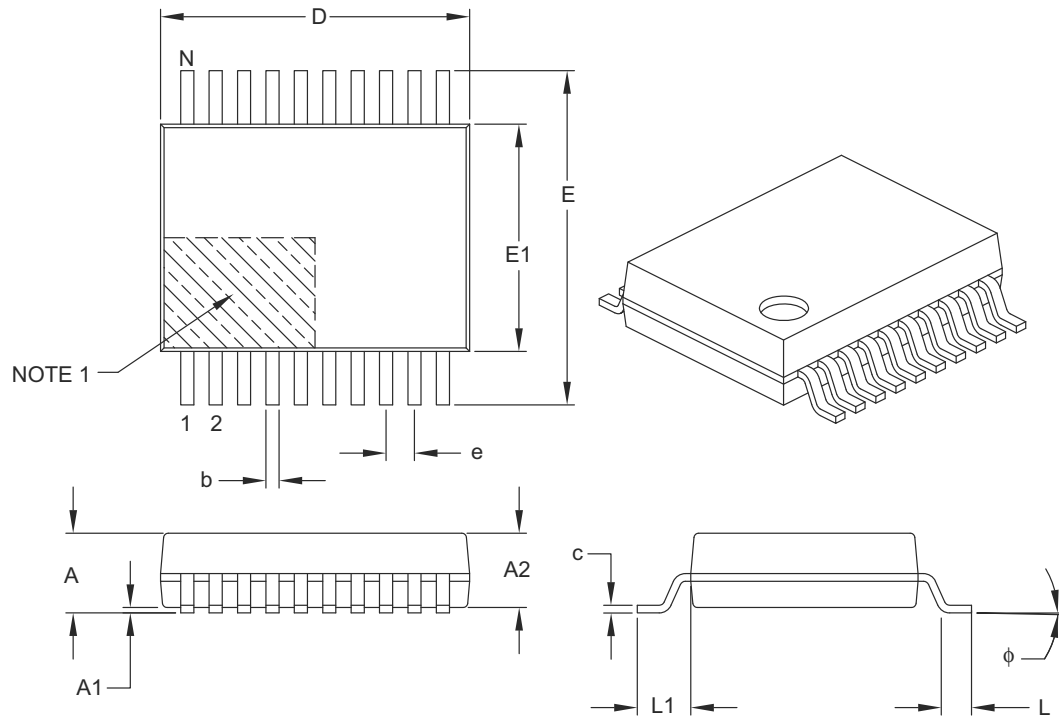
**2:** IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode, OSC1 is driven with external square wave from rail-to-rail
- CLK0 is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- MCLR = VDD; WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (PMDx bits are all zeroed)
- CPU is executing `while(1)` statement

**3:** These parameters are characterized but not tested in manufacturing.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

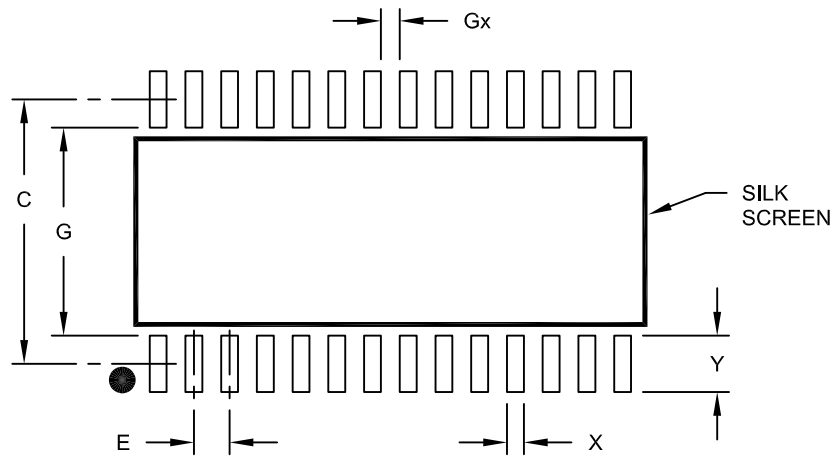
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

#### Notes:

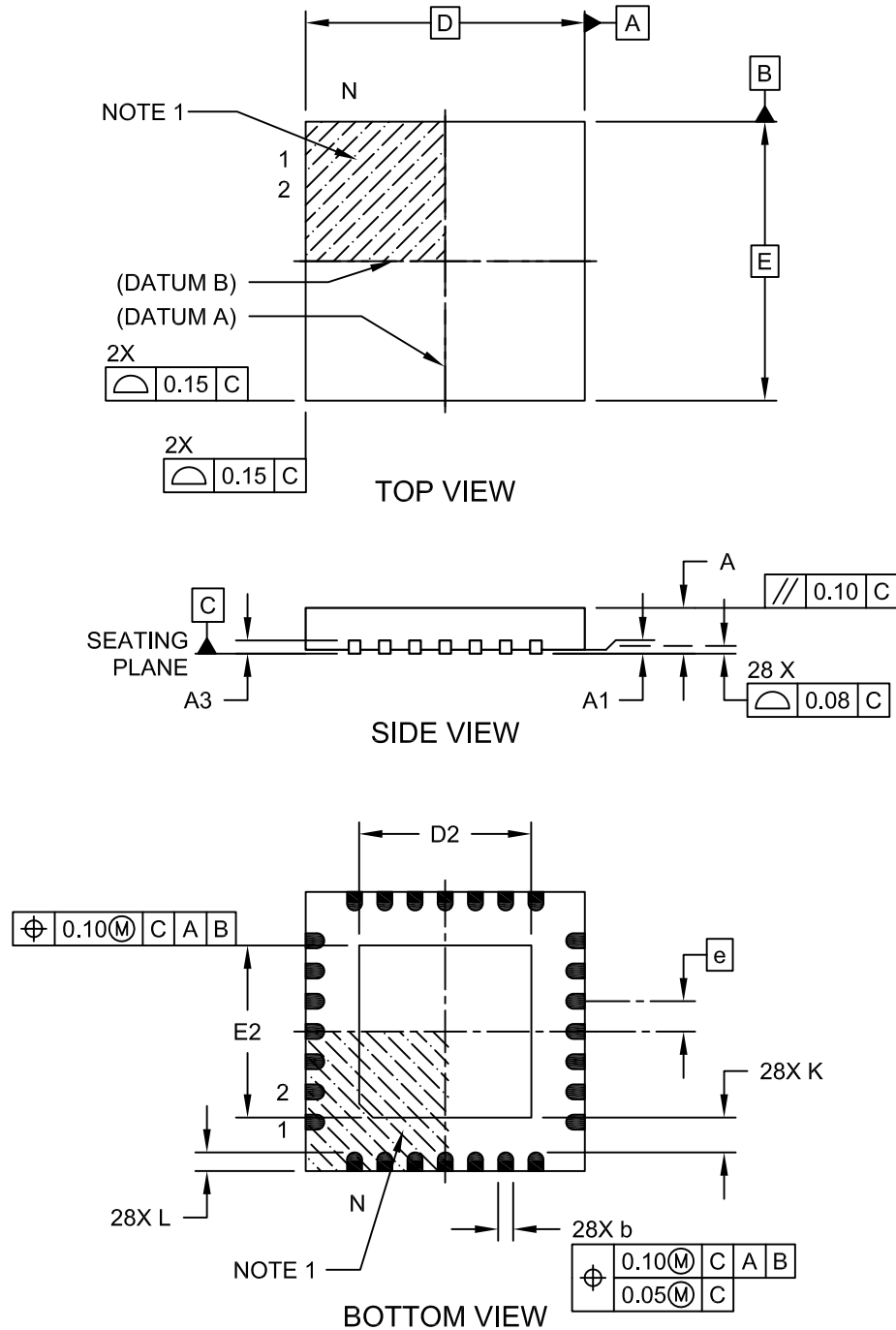
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

**28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S]  
With 0.40 mm Terminal Length**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-124C Sheet 1 of 2