Microchip Technology - DSPIC33FJ06GS101AT-I/SS Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	6KB (2K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs101at-i-ss

TABLE 4-16: I2C1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator Register									0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	AMSK<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-17: UART1 REGISTER MAP FOR dsPIC33FJ06GS101A, dsPIC33FJ06GS102A, dsPIC33FJ06GS202A AND dsPIC33FJ09GS302

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: SPI1 REGISTER MAP FOR dsPIC33FJ06GS101A, dsPIC33FJ06GS102A, dsPIC33FJ06GS202A AND dsPIC33FJ09GS302

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPIROV	—	—	—	—	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33FJ06GS001

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680	—	—	INT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR1	0682	—	—	—	—	—	—	—	—	—	—	INT2R<5:0>						003F
RPINR2	0684	—	—	T1CKR<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR3	0686	—	—	—	—	—	—	—	—	—	—	T2CKR<5:0>						003F
RPINR29	06BA	—	—	FLT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR30	06BC	—	—	FLT3R<5:0>						—	—	FLT2R<5:0>						3F3F
RPINR31	06BE	—	—	FLT5R<5:0>						—	—	FLT4R<5:0>						3F3F
RPINR32	06C0	—	—	FLT7R<5:0>						—	—	FLT6R<5:0>						3F3F
RPINR33	06C2	—	—	SYNCI1R<5:0>						—	—	FLT8R<5:0>						3F3F
RPINR34	06C4	—	—	—	—	—	—	—	—	—	—	SYNCI2R<5:0>						003F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33FJ06GS101A AND dsPIC33FJ06GS102A

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680	—	—	INT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR1	0682	—	—	—	—	—	—	—	—	—	—	INT2R<5:0>						003F
RPINR2	0684	—	—	T1CKR<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR3	0686	—	—	—	—	—	—	—	—	—	—	T2CKR<5:0>						003F
RPINR11	0696	—	—	—	—	—	—	—	—	—	—	OCFAR<5:0>						003F
RPINR18	06A4	—	—	U1CTSR<5:0>							—	U1RXR<5:0>						3F3F
RPINR20	06A8	—	—	SCK1R<5:0>							—	SDI1R<5:0>						3F3F
RPINR21	06AA	—	—	—	—	—	—	—	—	—	—	SS1R<5:0>						003F
RPINR29	06BA	—	—	FLT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR30	06BC	—	—	FLT3R<5:0>						—	—	FLT2R<5:0>						3F3F
RPINR31	06BE	—	—	FLT5R<5:0>						—	—	FLT4R<5:0>						3F3F
RPINR32	06C0	—	—	FLT7R<5:0>						—	—	FLT6R<5:0>						3F3F
RPINR33	06C2	—	—	SYNCI1R<5:0>						—	—	FLT8R<5:0>						3F3F
RPINR34	06C4	—	—	—	—	—	—	—	—	—	—	SYNCI2R<5:0>						003F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

6.0 RESETS

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Reset"** (DS70192) in the "*dsPIC33F/PIC24H Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: Software RESET Instruction
- WDTO: Watchdog Timer Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state, and some are unaffected.

Note: Refer to the specific peripheral section or **Section 3.0 "CPU"** of this data sheet for register Reset states.

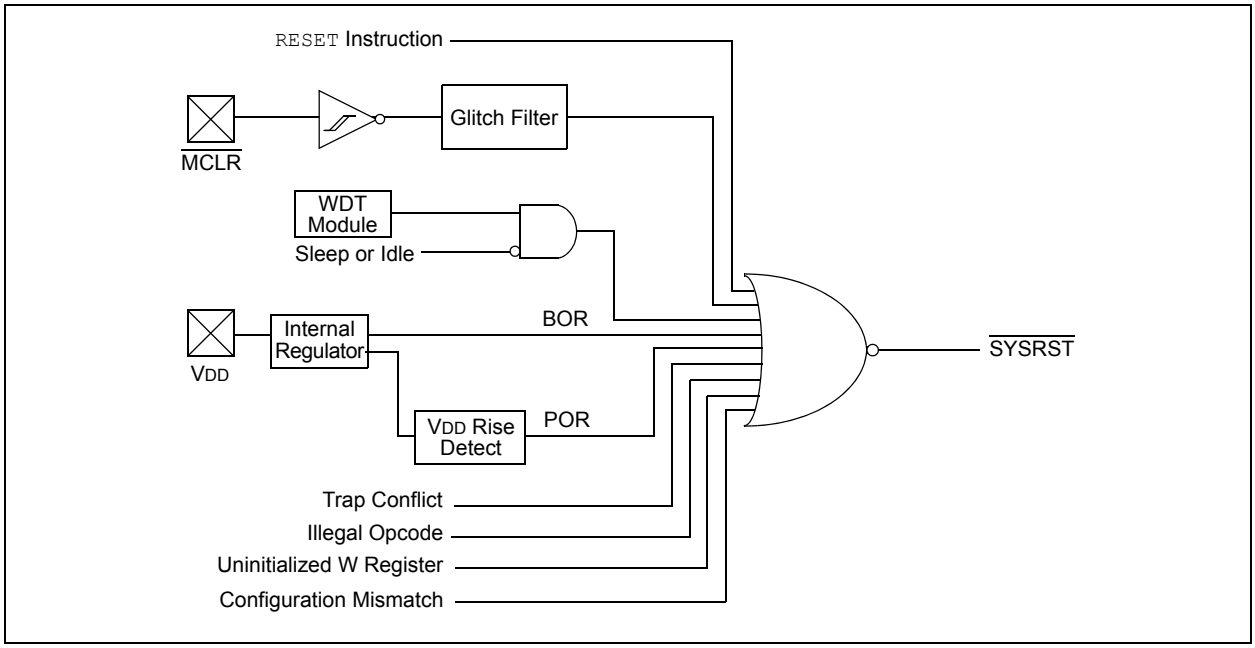
All types of device Reset sets a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits (except for the POR (RCON<0> bit) that are set. The user application can set or clear any bit, at any time, during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	INT2IF	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IF	CNIF	AC1IF(1	MI2C1IF	SI2C1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **INT2IF:** External Interrupt 2 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-5 **Unimplemented:** Read as '0'

bit 4 **INT1IF:** External Interrupt 1 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CNIF:** Input Change Notification Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **AC1IF:** Analog Comparator 1 Interrupt Flag Status bit(1)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 1 **MI2C1IF:** I2C1 Master Events Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **SI2C1IF:** I2C1 Slave Events Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: This bit is not implemented in dsPIC33FJ06GS101A/102A devices.

REGISTER 7-14: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	PSEMIE	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **PSEMIE:** PWM Special Event Match Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8-0 **Unimplemented:** Read as '0'

REGISTER 7-15: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	U1EIE(1)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **U1EIE:** UART1 Error Interrupt Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not implemented in the dsPIC33FJ06GS001 device.

REGISTER 8-5: ACLKCON: AUXILIARY CLOCK DIVISOR CONTROL REGISTER(1)

R/W-0	R-0	R/W-1	U-0	U-0	R/W-1	R/W-1	R/W-1
ENAPLL	APLLCK	SELACLK	—	—	APSTSCLR<2:0>(2)		
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
ASRCSEL	FRCSEL	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ENAPLL:** Auxiliary PLL Enable bit
1 = APLL is enabled
0 = APLL is disabled

bit 14 **APLLCK:** APLL Locked Status bit (read-only)
1 = Indicates that auxiliary PLL is in lock
0 = Indicates that auxiliary PLL is not in lock

bit 13 **SELACLK:** Select Auxiliary Clock Source for Auxiliary Clock Divider bit
1 = Auxiliary oscillators provides the source clock for auxiliary clock divider
0 = Primary PLL (FVCO) provides the source clock for auxiliary clock divider

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **APSTSCLR<2:0>:** Auxiliary Clock Output Divider bits(2)
111 = Divided by 1
110 = Divided by 2
101 = Divided by 4
100 = Divided by 8
011 = Divided by 16
010 = Divided by 32
001 = Divided by 64
000 = Divided by 256

bit 7 **ASRCSEL:** Select Reference Clock Source for Auxiliary Clock bit
1 = Primary oscillator is the clock source
0 = No clock input is selected

bit 6 **FRCSEL:** Select Reference Clock Source for Auxiliary PLL bit
1 = Selects FRC clock for auxiliary PLL
0 = Input clock source is determined by ASRCSEL bit setting

bit 5-0 **Unimplemented:** Read as '0'

Note 1: This register is reset only on a Power-on Reset (POR).

2: The auxiliary clock postscaler must be configured to divide-by-1 (APSTSCLR<2:0> = 111) for proper operation of the PWM module.

REGISTER 10-3: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T1CKR<5:0>					
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **T1CKR<5:0>:** Assign Timer1 External Clock (T1CK) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 10-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCFAR<5:0>(1)					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **OCFAR<5:0>:** Assign Output Compare A (OCFA) to the Corresponding RPn Pin bits(1)

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

Note 1: These bits are not implemented in the dsPIC33FJ06GS001 device.

REGISTER 10-15: RPINR34: PERIPHERAL PIN SELECT INPUT REGISTER 34

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SYNCI2R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **SYNCI2R<5:0>:** Assign PWM Master Time Base External Synchronization Signal to the Corresponding RPn Pin bits

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

REGISTER 15-6: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,3)
1 = Center-Aligned mode is enabled
0 = Center-Aligned mode is disabled

bit 1 **XPRES:** External PWM Reset Control bit(4)
1 = Current-limit source resets time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWM time base

bit 0 **IUE:** Immediate Update Enable bit
1 = Updates to the active MDC/PDCx/SDCx registers are immediate
0 = Updates to the active MDC/PDCx/SDCx registers are synchronized to the PWM time base

Note 1: Software must clear the interrupt status here and the corresponding IFSx bit in the interrupt controller.

2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

3: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

4: To operate in External Period Reset mode, configure the CLMOD (FCLCONx<8>) bit = 0 and ITB (PWMCONx<9>) bit = 1.

REGISTER 15-7: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8>(2)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0>(2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits(2)

Note 1: In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL. The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period-0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSBs.

REGISTER 15-8: SDCx: PWMx SECONDARY DUTY CYCLE REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<15:8>(2)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<7:0>(2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **SDCx<15:0>:** Secondary Duty Cycle for PWMxL Output Pin bits(2)

Note 1: The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle. The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period-0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSBs.

REGISTER 15-11: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 15-12: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTR <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 18-2: U1STA: UART1 STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1(2)	UTXINV(2)	UTXISEL0(2)	—	UTXBRK(2)	UTXEN(1,2)	UTXBF(2)	TRMT(2)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL<1:0>(2)		ADDEN(2)	RIDLE(2)	PERR(2)	FERR(2)	OERR(2)	URXDA(2)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL<1:0>:** Transmission Interrupt Mode Selection bits(2)
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies that there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** Transmit Polarity Inversion bit(2)

If IREN = 0:
- 1 = U1TX Idle state is '0'
- 0 = U1TX Idle state is '1'

If IREN = 1:
- 1 = IrDA® encoded U1TX Idle state is '1'
- 0 = IrDA encoded U1TX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** Transmit Break bit(2)
- 1 = Send Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** Transmit Enable bit(1,2)
- 1 = Transmit is enabled, U1TX pin is controlled by UART1
- 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; U1TX pin is controlled by port

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)(2)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full; at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)(2)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

Note 1: Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F/PIC24H Family Reference Manual"* for information on enabling the UART module for transmit operation.

2: This bit is not available in the dsPIC33FJ06GS001 device.

REGISTER 19-3: ADBASE: ADC BASE REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADBASE<15:8>(2)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
ADBASE<7:1>(2)							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **ADBASE<15:1>:** ADC Base Register bits(2)

This register contains the base address of the user's ADC Interrupt Service Routine (ISR) jump table. This register, when read, contains the sum of the ADBASE register contents and the encoded value of the PxRDY status bits.

The encoder logic provides the bit number of the highest priority PxRDY bits, where P0RDY is the highest priority and P6RDY is the lowest priority.

bit 0 **Unimplemented:** Read as '0'

Note 1: As an alternative to using the ADBASE register, the ADCP0-6 ADC Pair Conversion Complete Interrupts can be used to invoke A to D conversion completion routines for individual ADC input pairs.

2: The encoding results are shifted left two bits, so bits 1-0 of the result are always zero.

25.1 DC Characteristics

TABLE 25-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Maximum MIPS
			dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302
—	VBOR-3.6V(1)	-40°C to +85°C	40
—	VBOR-3.6V(1)	-40°C to +125°C	40

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below VDDMIN. Refer to Parameter BO10 in Table 25-11 for BOR values.

TABLE 25-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 25-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 18-Pin SOIC	θJA	57	—	°C/W	1
Package Thermal Resistance, 18-pin PDIP	θJA	66	—	°C/W	1
Package Thermal Resistance, 20-pin SSOP	θJA	64	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θJA	34	—	°C/W	1
Package Thermal Resistance, 28-pin SSOP	θJA	71	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θJA	47	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θJA	45	—	°C/W	1
Package Thermal Resistance, 36-Pin VTLA	θJA	29	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 25-17: PLL CLOCK TIMING SPECIFICATIONS (VDD = 3.0V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8	MHz	ECPLL, XTPLL modes
OS51	FSYS	On-Chip VCO System Frequency	100	—	200	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	mS	
OS53	DCLK	CLKO Stability (Jitter)(2)	-3	0.5	3	%	Measured over 100 ms period

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

2: These parameters are characterized by similarity, but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$Peripheral\ Clock\ Jitter = \frac{DCLK}{\sqrt{\left(\frac{FOSC}{Peripheral\ Bit\ Rate\ Clock}\right)}}$$

For example: FOSC = 32 MHz, DCLK = 3%, SPI bit rate clock (i.e., SCK) is 2 MHz.

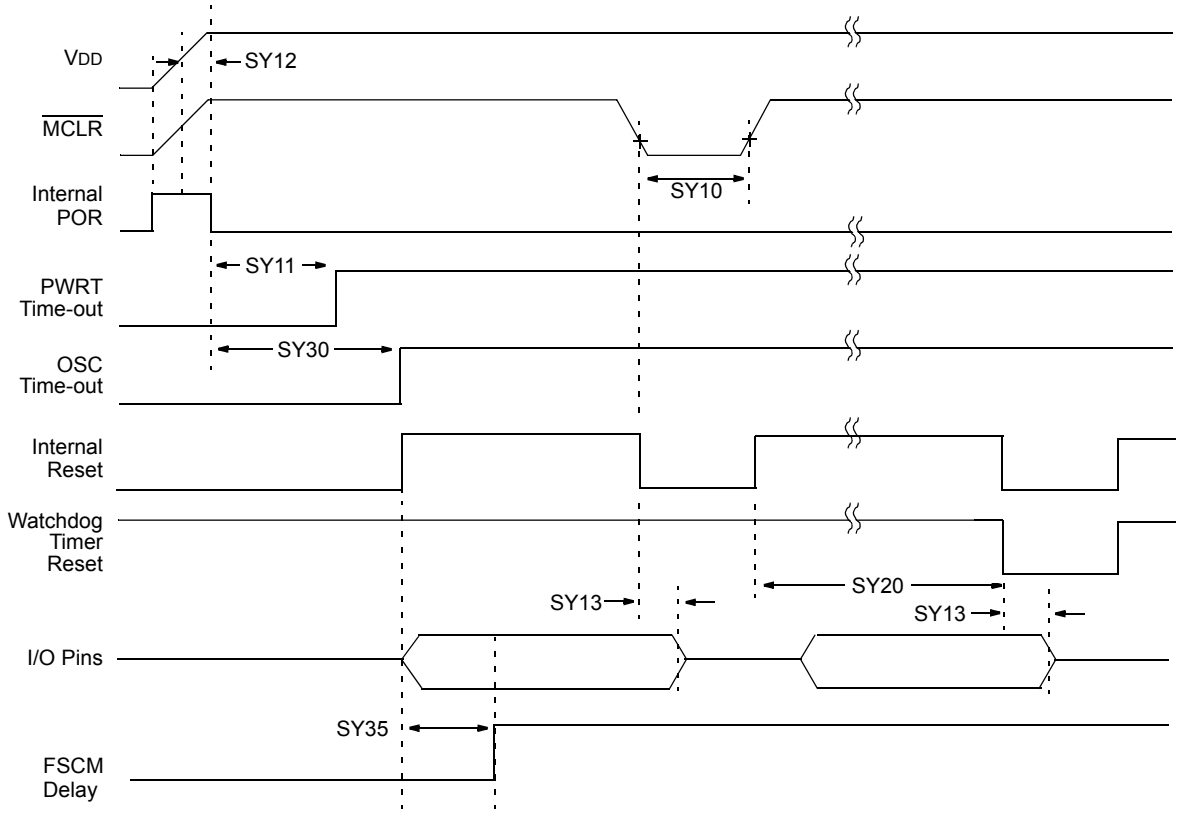
$$SPI\ SCK\ Jitter = \left[\frac{DCLK}{\sqrt{\left(\frac{32\ MHz}{2\ MHz}\right)}}\right] = \left[\frac{3\%}{\sqrt{16}}\right] = \left[\frac{3\%}{4}\right] = 0.75\%$$

TABLE 25-18: AUXILIARY PLL CLOCK TIMING SPECIFICATIONS (VDD = 3.0V TO 3.6V)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
OS56	FHPOUT	On-Chip 16x PLL CCO Frequency	112	118	120	MHz	
OS57	FHPIN	On-Chip 16x PLL Phase Detector Input Frequency	7.0	7.37	7.5	MHz	
OS58	TSU	Frequency Generator Lock Time	—	—	10	µs	

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested in manufacturing.

FIGURE 25-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS



Note: Refer to Figure 25-1 for load conditions.

TABLE 25-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY10	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	μs	-40°C to +125°C
SY11	TPWRT	Power-up Timer Period	—	64	—	ms	-40°C to +125°C
SY12	TPOR	Power-on Reset Delay	3	10	30	μs	-40°C to +125°C
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	
SY30	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 period

Note 1: These parameters are characterized but not tested in manufacturing.
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 26-9: TYPICAL FRC FREQUENCY @ VDD = 3.3V

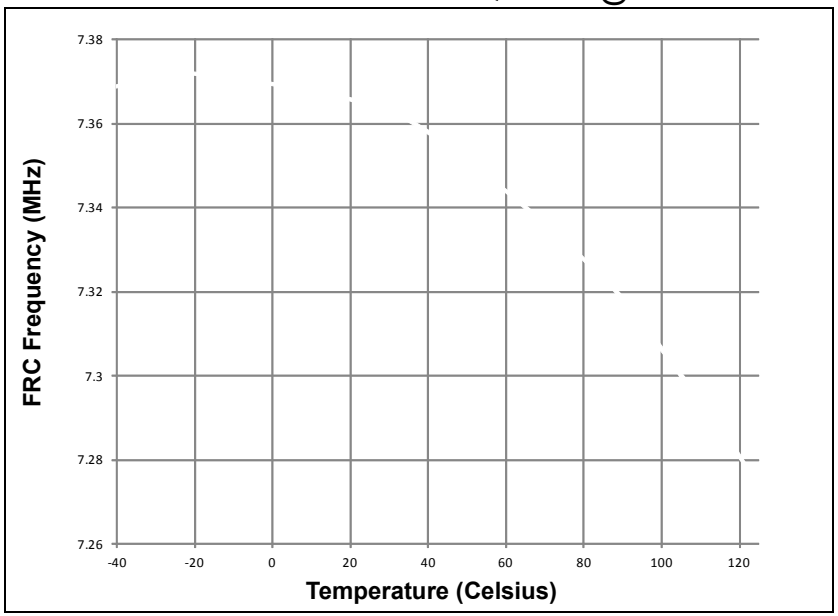


FIGURE 26-10: TYPICAL INTREF @ VDD = 3.3V

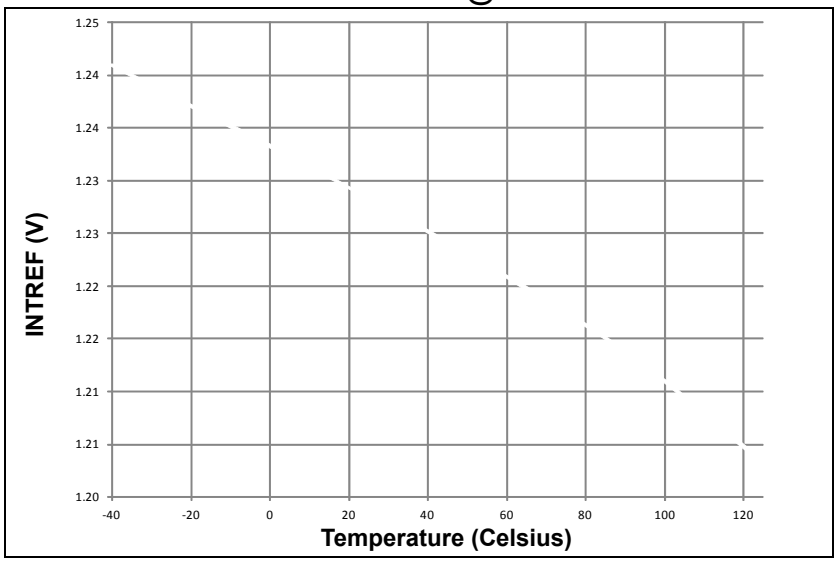
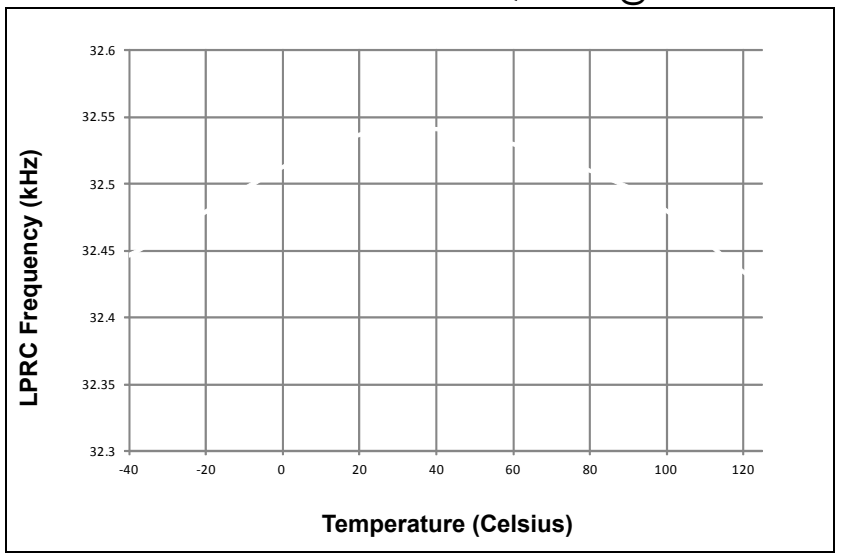
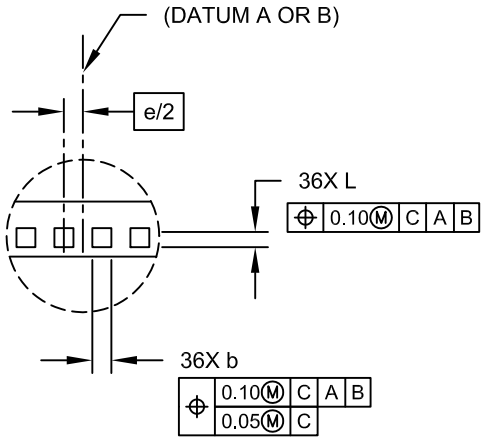


FIGURE 26-11: TYPICAL LPRC FREQUENCY @ VDD = 3.3V

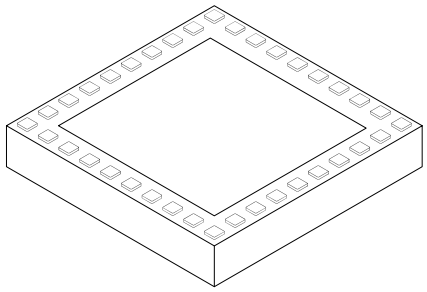


36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		36	
Number of Pins per Side	ND		10	
Number of Pins per Side	NE		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2

U

V

W