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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	6KB (2K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs102a-e-ss

TABLE 4-24: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33FJ06GS001

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680	—	—	INT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR1	0682	—	—	—	—	—	—	—	—	—	—	INT2R<5:0>						003F
RPINR2	0684	—	—	T1CKR<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR3	0686	—	—	—	—	—	—	—	—	—	—	T2CKR<5:0>						003F
RPINR29	06BA	—	—	FLT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR30	06BC	—	—	FLT3R<5:0>						—	—	FLT2R<5:0>						3F3F
RPINR31	06BE	—	—	FLT5R<5:0>						—	—	FLT4R<5:0>						3F3F
RPINR32	06C0	—	—	FLT7R<5:0>						—	—	FLT6R<5:0>						3F3F
RPINR33	06C2	—	—	SYNC1R<5:0>						—	—	FLT8R<5:0>						3F3F
RPINR34	06C4	—	—	—	—	—	—	—	—	—	—	SYNC2R<5:0>						003F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33FJ06GS101A AND dsPIC33FJ06GS102A

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	0680	—	—	INT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR1	0682	—	—	—	—	—	—	—	—	—	—	INT2R<5:0>						003F
RPINR2	0684	—	—	T1CKR<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR3	0686	—	—	—	—	—	—	—	—	—	—	T2CKR<5:0>						003F
RPINR11	0696	—	—	—	—	—	—	—	—	—	—	OCFAR<5:0>						003F
RPINR18	06A4	—	—	U1CTSR<5:0>						—	—	U1RXR<5:0>						3F3F
RPINR20	06A8	—	—	SCK1R<5:0>						—	—	SDI1R<5:0>						3F3F
RPINR21	06AA	—	—	—	—	—	—	—	—	—	—	SS1R<5:0>						003F
RPINR29	06BA	—	—	FLT1R<5:0>						—	—	—	—	—	—	—	—	3F00
RPINR30	06BC	—	—	FLT3R<5:0>						—	—	FLT2R<5:0>						3F3F
RPINR31	06BE	—	—	FLT5R<5:0>						—	—	FLT4R<5:0>						3F3F
RPINR32	06C0	—	—	FLT7R<5:0>						—	—	FLT6R<5:0>						3F3F
RPINR33	06C2	—	—	SYNC1R<5:0>						—	—	FLT8R<5:0>						3F3F
RPINR34	06C4	—	—	—	—	—	—	—	—	—	—	SYNC2R<5:0>						003F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.5 Flash Memory Control Registers

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

R/SO-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
WR ⁽¹⁾	WREN ⁽¹⁾	WRERR ⁽¹⁾	—	—	—	—	—
bit 15			bit 8				

U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ERASE ⁽¹⁾	—	—	NVMOP<3:0> ^(1,2)			
bit 7				bit 0			

Legend:	SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **WR:** Write Control bit⁽¹⁾
 1 = Initiates a Flash memory program or erase operation. The operation is self-timed and the bit is cleared by hardware once operation is complete. This bit can only be set (not cleared) in software.
 0 = Program or erase operation is complete and inactive
- bit 14 **WREN:** Write Enable bit⁽¹⁾
 1 = Enables Flash program/erase operations
 0 = Inhibits Flash program/erase operations
- bit 13 **WRERR:** Write Sequence Error Flag bit⁽¹⁾
 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
 0 = The program or erase operation completed normally
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **ERASE:** Erase/Program Enable bit⁽¹⁾
 1 = Performs the erase operation specified by NVMOP<3:0> on the next WR command
 0 = Performs the program operation specified by NVMOP<3:0> on the next WR command
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits^(1,2)
If ERASE = 1:
 1111 = No operation
 1101 = Erase general segment
 0011 = No operation
 0010 = Memory page erase operation
 0001 = Reserved
 0000 = Reserved

If ERASE = 0:
 1111 = No operation
 1101 = No operation
 0011 = Memory word program operation
 0010 = No operation
 0001 = Reserved
 0000 = Reserved

- Note 1:** These bits can only be reset on a Power-on Reset (POR).
Note 2: All other combinations of NVMOP<3:0> are unimplemented.

6.5 External Reset (EXTR)

The external Reset is generated by driving the $\overline{\text{MCLR}}$ pin low. The $\overline{\text{MCLR}}$ pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to **Section 25.0 “Electrical Characteristics”** for minimum pulse width specifications. The external Reset ($\overline{\text{MCLR}}$) pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the $\overline{\text{MCLR}}$ Reset.

6.5.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate Reset signals to reset multiple devices in the system. This external Reset signal can be directly connected to the $\overline{\text{MCLR}}$ pin to reset the device when the rest of the system is reset.

6.5.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to reset the device, the external Reset pin ($\overline{\text{MCLR}}$) should be tied directly or resistively to VDD. In this case, the $\overline{\text{MCLR}}$ pin will not be used to generate a Reset. The external Reset pin ($\overline{\text{MCLR}}$) does not have an internal pull-up and must not be left unconnected.

6.6 Software RESET Instruction (SWR)

Whenever the RESET instruction is executed, the device will assert $\overline{\text{SYSRST}}$, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the RESET instruction will still remain. $\overline{\text{SYSRST}}$ is released at the next instruction cycle and the Reset vector fetch will commence.

The Software Reset (SWR) flag (instruction) in the Reset Control register (RCON<6>) is set to indicate the software Reset.

6.7 Watchdog Time-out Reset (WDTO)

Whenever a Watchdog Timer time-out occurs, the device will asynchronously assert $\overline{\text{SYSRST}}$. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out (WDTO) flag in the Reset Control (RCON<4>) register is set to indicate the Watchdog Timer Reset. Refer to **Section 22.4 “Watchdog Timer (WDT)”** for more information on Watchdog Reset.

6.8 Trap Conflict Reset

If a lower priority hard trap occurs, while a higher priority trap is being processed, a hard Trap Conflict Reset occurs. The hard traps include exceptions of Priority Level 13 through Level 15, inclusive. The address error (Level 13) and oscillator error (Level 14) traps fall into this category.

The Trap Reset (TRAPR) flag in the Reset Control register (RCON<15>) is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 “Interrupt Controller”** for more information on Trap Conflict Resets.

6.9 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The illegal opcode or Uninitialized W Access Reset (IOPUWR) flag in the Reset Control register (RCON<14>) is set to indicate the illegal condition device Reset.

6.9.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 0x3F, which is an illegal opcode value.

6.9.2 UNINITIALIZED W REGISTER RESET

Any attempt to use the uninitialized W register as an Address Pointer will Reset the device. The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to.

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	ADIF	U1TXIF ⁽¹⁾	U1RXIF ⁽¹⁾	SPI1IF ⁽¹⁾	SPI1EIF ⁽¹⁾	—
bit 15							bit 8

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IF	—	—	—	T1IF	OC1IF ⁽¹⁾	IC1IF ⁽²⁾	INT0IF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **ADIF:** ADC Group Conversion Complete Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 12 **U1TXIF:** UART1 Transmitter Interrupt Flag Status bit⁽¹⁾
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 11 **U1RXIF:** UART1 Receiver Interrupt Flag Status bit⁽¹⁾
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 10 **SPI1IF:** SPI1 Event Interrupt Flag Status bit⁽¹⁾
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 9 **SPI1EIF:** SPI1 Error Interrupt Flag Status bit⁽¹⁾
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 8 **Unimplemented:** Read as '0'
- bit 7 **T2IF:** Timer2 Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 6-4 **Unimplemented:** Read as '0'
- bit 3 **T1IF:** Timer1 Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 2 **OC1IF:** Output Compare Channel 1 Interrupt Flag Status bit⁽¹⁾
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 1 **IC1IF:** Input Capture Channel 1 Interrupt Flag Status bit⁽²⁾
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 **INT0IF:** External Interrupt 0 Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

Note 1: This bit is not implemented in the dsPIC33FJ06GS001 device.

2: This bit is not implemented in dsPIC33FJ06GS001/101A/102A devices.

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 7-21: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	U1RXIP<2:0> ⁽¹⁾			—	SPI1IP<2:0> ⁽¹⁾		
bit 15				bit 8			

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	SPI1EIP<2:0> ⁽¹⁾			—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **U1RXIP<2:0>:** UART1 Receiver Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

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001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **SPI1IP<2:0>:** SPI1 Event Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

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001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SPI1EIP<2:0>:** SPI1 Error Interrupt Priority bits⁽¹⁾

111 = Interrupt is Priority 7 (highest priority interrupt)

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001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: These bits are not implemented in the dsPIC33FJ06GS001 device.

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 7-26: IPC14: INTERRUPT PRIORITY CONTROL REGISTER 14

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	PSEMIP<2:0>			—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'
bit 6-4 **PSEMIP<2:0>:** PWM Special Event Match Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
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•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled
bit 3-0 **Unimplemented:** Read as '0'

REGISTER 7-27: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	U1EIP<2:0> ⁽¹⁾			—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'
bit 6-4 **U1EIP<2:0>:** UART1 Error Interrupt Priority bits⁽¹⁾
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled
bit 3-0 **Unimplemented:** Read as '0'

Note 1: These bits are not implemented in the dsPIC33FJ06GS001 device.

REGISTER 7-35: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR<3:0>			
bit 15				bit 8			

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM<6:0>						
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits

1111 = CPU Interrupt Priority Level is 15

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0001 = CPU Interrupt Priority Level is 1

0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt bits

0111111 = Interrupt vector pending is Number 135

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0000001 = Interrupt vector pending is Number 9

0000000 = Interrupt vector pending is Number 8

10.6 Peripheral Pin Select (PPS)

Peripheral Pin Select configuration enables peripheral set selection and placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, programmers can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Programmers can independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

10.6.1 AVAILABLE PINS

The Peripheral Pin Select feature is used with a range of up to 16 pins. The number of available pins depends on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation, "RPn", in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable pin number.

10.6.2 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of Special Function Registers: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

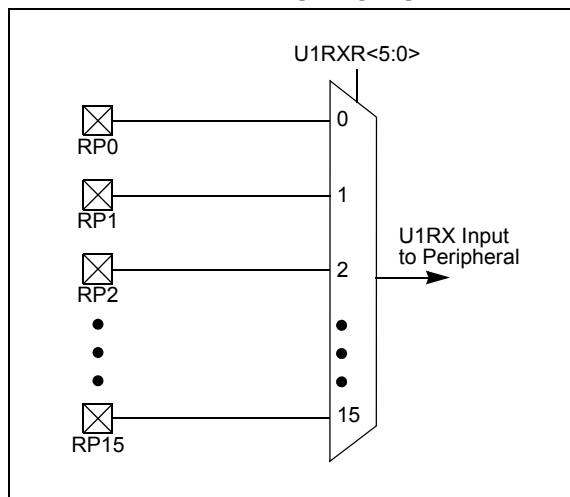
10.6.2.1 Input Mapping

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. A control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 10-1 through Register 10-15). Each register contains sets of 6-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 6-bit value maps the RPn pin with that value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

Figure 10-2 illustrates the remappable pin selection for the U1RX input.

Note: For input mapping only, the Peripheral Pin Select (PPS) functionality does not have priority over the TRISx settings. Therefore, when configuring the RPx pin for input, the corresponding bit in the TRISx register must also be configured for input (i.e., set to '1').

FIGURE 10-2: REMAPPABLE MUX INPUT FOR U1RX



dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 10-12: RPINR31: PERIPHERAL PIN SELECT INPUT REGISTER 31

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT5R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	FLT4R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FLT5R<5:0>:** Assign PWM Fault Input 5 (FLT5) to the Corresponding RPn Pin bits

111111 = Input tied to Vss

100011 = Input tied to RP35

100010 = Input tied to RP34

100001 = Input tied to RP33

100000 = Input tied to RP32

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•

•

000000 = Input tied to RP0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FLT4R<5:0>:** Assign PWM Fault Input 4 (FLT4) to the Corresponding RPn Pin bits

111111 = Input tied to Vss

100011 = Input tied to RP35

100010 = Input tied to RP34

100001 = Input tied to RP33

100000 = Input tied to RP32

•

•

•

000000 = Input tied to RP0

REGISTER 15-14: IOCONx: PWMx I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD<1:0> ⁽¹⁾	OVRENH	OVRENL	
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT<1:0>	FLTDAT<1:0> ⁽²⁾	CLDAT<1:0> ⁽²⁾	SWAP	OSYNC			
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **PENH:** PWMxH Output Pin Ownership bit
 1 = PWM module controls PWMxH pin
 0 = GPIO module controls PWMxH pin
- bit 14 **PENL:** PWMxL Output Pin Ownership bit
 1 = PWM module controls PWMxL pin
 0 = GPIO module controls PWMxL pin
- bit 13 **POLH:** PWMxH Output Pin Polarity bit
 1 = PWMxH pin is active-low
 0 = PWMxH pin is active-high
- bit 12 **POLL:** PWMxL Output Pin Polarity bit
 1 = PWMxL pin is active-low
 0 = PWMxL pin is active-high
- bit 11-10 **PMOD<1:0>:** PWMx I/O Pin Mode bits⁽¹⁾
 11 = PWM I/O pin pair is in the True Independent Output mode
 10 = PWM I/O pin pair is in the Push-Pull Output mode
 01 = PWM I/O pin pair is in the Redundant Output mode
 00 = PWM I/O pin pair is in the Complementary Output mode
- bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
 1 = OVRDAT<1> provides data for output on PWMxH pin
 0 = PWM generator provides data for PWMxH pin
- bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
 1 = OVRDAT<0> provides data for output on PWMxL pin
 0 = PWM generator provides data for PWMxL pin
- bit 7-6 **OVRDAT<1:0>:** Data for PWMxH and PWMxL Pins if Override is Enabled bits
 If OVERENH = 1 then OVRDAT<1> provides data for PWMxH.
 If OVERENL = 1 then OVRDAT<0> provides data for PWMxL.
- bit 5-4 **FLTDAT<1:0>:** State for PWMxH and PWMxL Pins if FLTMOD is Enabled bits⁽²⁾
 IFLTMOD (FCLCONx<15>) = 0, Normal Fault mode:
 If Fault is active, then FLTDAT<1> provides the state for PWMxH.
 If Fault is active, then FLTDAT<0> provides the state for PWMxL.
 IFLTMOD (FCLCONx<15>) = 1, Independent Fault mode:
 If current-limit is active, then FLTDAT<1> provides the state for PWMxH.
 If Fault is active, then FLTDAT<0> provides the state for PWMxL.

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

2: State represents the active/inactive state of the PWM module depending on the POLH and POLL bit settings.

18.1 UART Helpful Tips

1. In multinode, direct-connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (U1MODE<4>), which defines the Idle state, the default of which is logic high, (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received after the device has been initialized to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin, depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the RX pin.
 - b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode, caused by activity on the UxRX pin of the UART module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized. This results in the first character being invalid; this is to be expected.

18.2 UART Resources

Many useful resources related to UART are provided on the Microchip web site (www.microchip.com).

18.2.1 KEY RESOURCES

- **Section 17. “UART”** (DS70188) in the *“dsPIC33F/PIC24H Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33F/PIC24H Family Reference Manual”* Sections
- Development Tools

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 19-5: ADCPC0: ADC CONVERT PAIR CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN1	PEND1	SWTRG1	TRGSRC1<4:0>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQEN0	PEND0	SWTRG0	TRGSRC0<4:0>				
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **IRQEN1:** Interrupt Request Enable 1 bit
1 = Enables IRQ generation when requested conversion of channels AN3 and AN2 is completed
0 = IRQ is not generated
- bit 14 **PEND1:** Pending Conversion Status 1 bit
1 = Conversion of channels AN3 and AN2 is pending; set when selected trigger is asserted
0 = Conversion is complete
- bit 13 **SWTRG1:** Software Trigger 1 bit
1 = Starts conversion of AN3 and AN2 (if selected by the TRGSRCx bits)⁽¹⁾
This bit is automatically cleared by hardware when the PEND1 bit is set.
0 = Conversion has not started
- bit 12-8 **TRGSRC1<4:0>:** Trigger 1 Source Selection bits
Selects trigger source for conversion of analog channels AN3 and AN2.
11111 = Timer2 period match
•
•
•
11011 = Reserved
11010 = PWM Generator 4 current-limit ADC trigger
11001 = Reserved
11000 = PWM Generator 2 current-limit ADC trigger
10111 = PWM Generator 1 current-limit ADC trigger
10110 = Reserved
•
•
•
10010 = Reserved
10001 = PWM Generator 4 secondary trigger is selected
10000 = Reserved
01111 = PWM Generator 2 secondary trigger is selected
01110 = PWM Generator 1 secondary trigger is selected
01101 = Reserved
01100 = Timer1 period match
•
•
•
01000 = Reserved
00111 = PWM Generator 4 primary trigger is selected
00110 = Reserved
00101 = PWM Generator 2 primary trigger is selected
00100 = PWM Generator 1 primary trigger is selected
00011 = PWM Special Event Trigger is selected
00010 = Global software trigger is selected
00001 = Individual software trigger is selected
00000 = No conversion is enabled

Note 1: The trigger source must be set as a global software trigger prior to setting this bit to '1'. If other conversions are in progress, then conversion will be performed when the conversion resources are available.

24.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C® for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICKit™ 3 Debug Express
- Device Programmers
 - PICKit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

24.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

24.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

24.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

24.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

25.1 DC Characteristics

TABLE 25-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Maximum MIPS
			dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302
—	VBOR-3.6V ⁽¹⁾	-40°C to +85°C	40
—	VBOR-3.6V ⁽¹⁾	-40°C to +125°C	40

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is tested but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below V_{DDMIN} . Refer to Parameter BO10 in Table 25-11 for BOR values.

TABLE 25-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $I/O = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	$(T_J - T_A)/\theta_{JA}$			W

TABLE 25-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 18-Pin SOIC	θ_{JA}	57	—	°C/W	1
Package Thermal Resistance, 18-pin PDIP	θ_{JA}	66	—	°C/W	1
Package Thermal Resistance, 20-pin SSOP	θ_{JA}	64	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θ_{JA}	34	—	°C/W	1
Package Thermal Resistance, 28-pin SSOP	θ_{JA}	71	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	47	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	45	—	°C/W	1
Package Thermal Resistance, 36-Pin VTLA	θ_{JA}	29	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

FIGURE 25-19: I2C1 BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

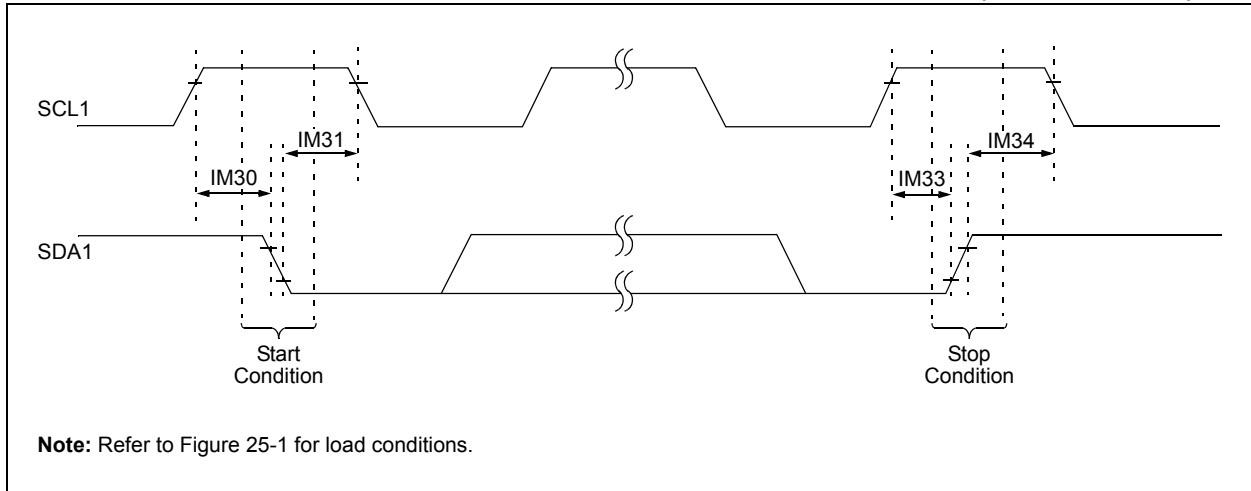


FIGURE 25-20: I2C1 BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

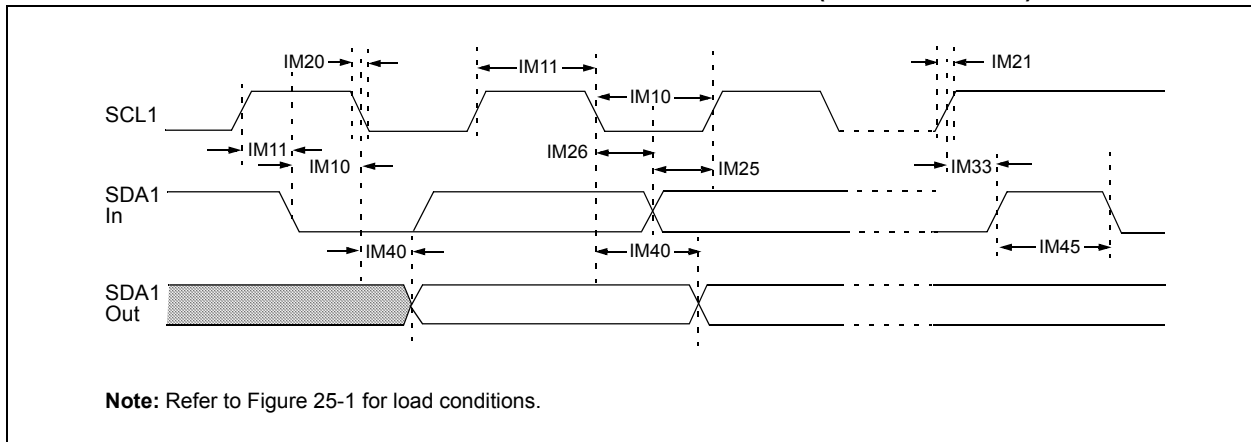


TABLE 25-39: 10-BIT HIGH-SPEED ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS ⁽²⁾			Standard Operating Conditions: 3.0V and 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
Dynamic Performance							
AD30	THD	Total Harmonic Distortion	—	-73	—	dB	
AD31	SINAD	Signal to Noise and Distortion	—	58	—	dB	
AD32	SFDR	Spurious Free Dynamic Range	—	-73	—	dB	
AD33	FNYQ	Input Signal Bandwidth	—	—	1	MHz	
AD34	ENOB	Effective Number of Bits	—	9.4	—	bits	

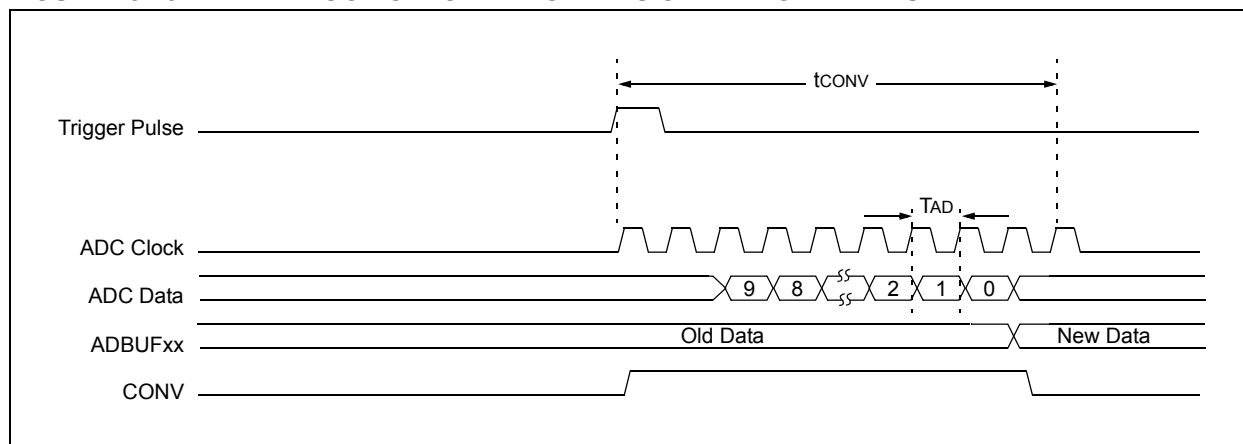
- Note 1:** The Analog-to-Digital conversion result never decreases with an increase in input voltage and has no missing codes.
- Note 2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules, such as the ADC, etc., will function, but with degraded performance below VDDMIN. Refer to Parameter BO10 in Table 25-11 for BOR values.
- Note 3:** These parameters are characterized by similarity, but are not tested in manufacturing.

TABLE 25-40: 10-BIT HIGH-SPEED ADC MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50b	TAD	ADC Clock Period	35.8	—	—	ns	
Conversion Rate							
AD55b	tCONV	Conversion Time	—	14 TAD	—	—	
AD56b	FCNV	Throughput Rate					
		Devices with Single SAR	—	—	2.0	Msp/s	
Timing Parameters							
AD63b	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On	1.0	—	10	μs	

- Note 1:** These parameters are characterized but not tested in manufacturing.

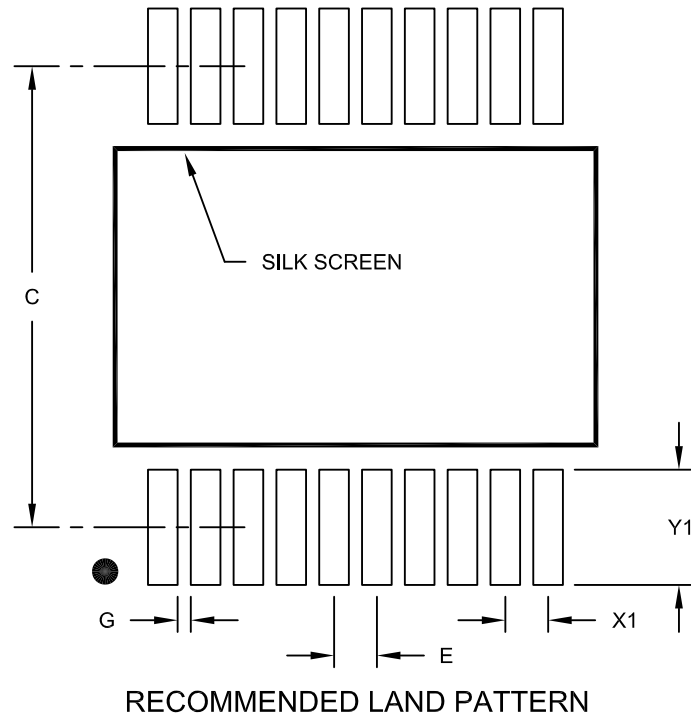
FIGURE 25-23: ANALOG-TO-DIGITAL CONVERSION TIMING PER INPUT



dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

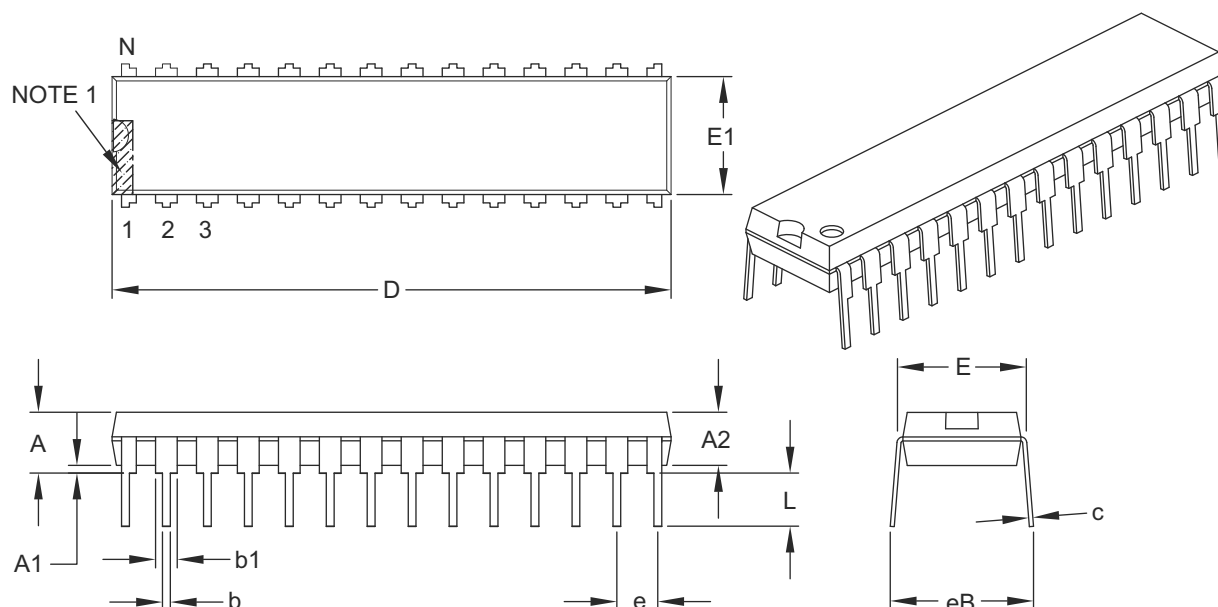
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

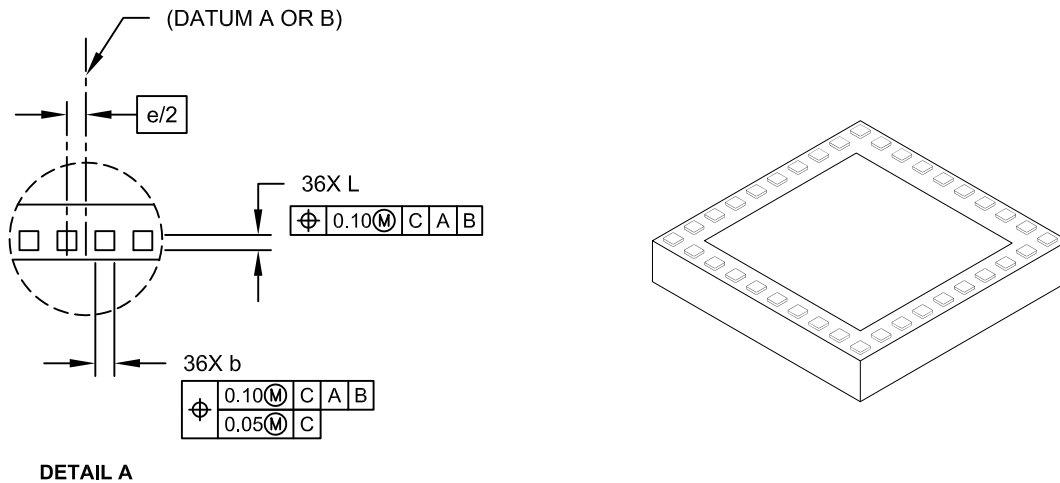
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	36		
Number of Pins per Side	ND	10		
Number of Pins per Side	NE	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2