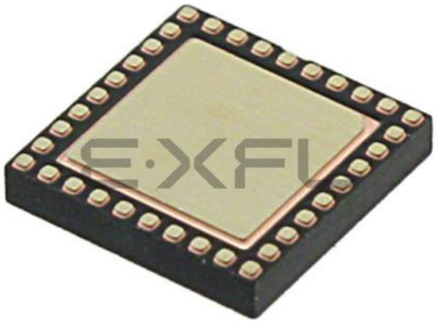

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

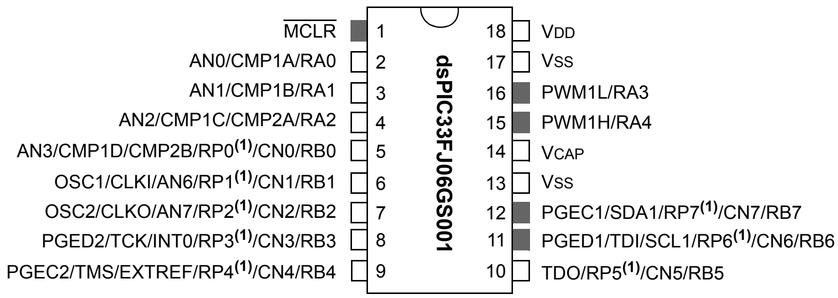
Applications of "Embedded - Microcontrollers"

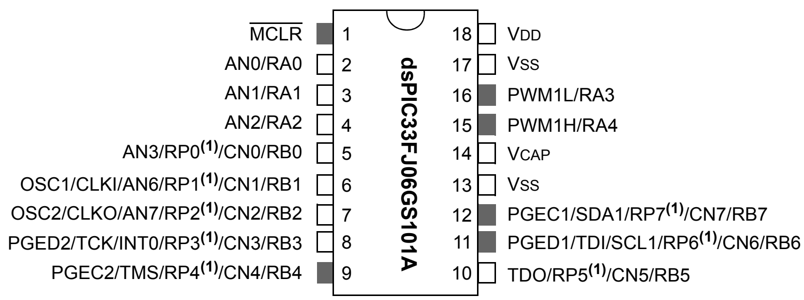
Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	6KB (2K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs102a-e-tl

Pin Diagrams

18-Pin SOIC, PDIP

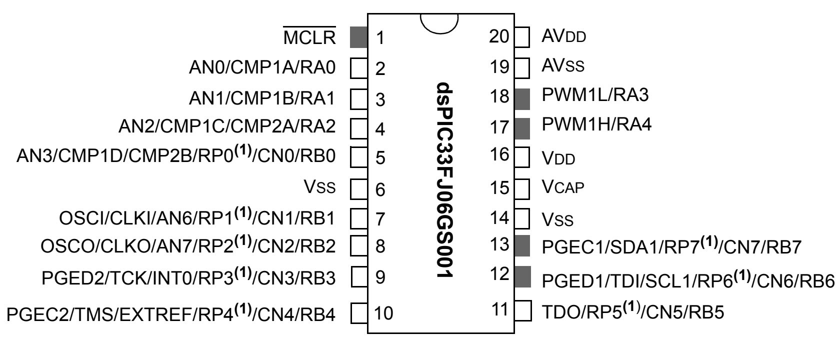
■ = Pins are up to 5V tolerant

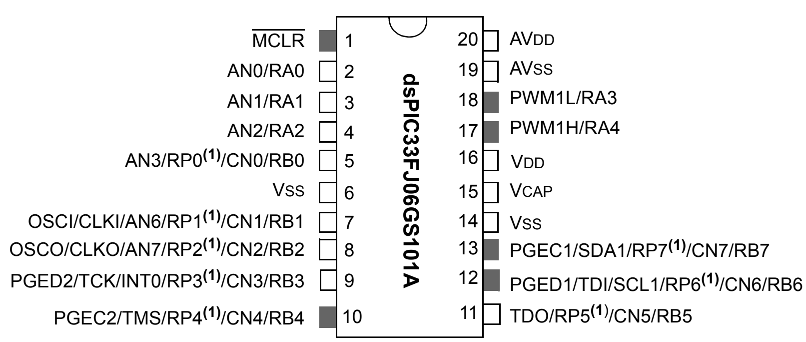




20-Pin SSOP

■ = Pins are up to 5V tolerant





Note 1: The RPn pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
AN0-AN7	I	Analog	No	Analog input channels.
CLKI	I	ST/CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
CN0-CN15	I	ST	No	Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
IC1	I	ST	Yes	Capture Input 1.
OCFA	I	ST	Yes	Compare Fault A input (for Compare Channel 1).
OC1	O	—	Yes	Compare Output 1.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15(1)	I/O	ST	No	PORTB is a bidirectional I/O port.
RP0-RP15(1)	I/O	ST	No	Remappable I/O pins.
T1CK	I	ST	Yes	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
$\overline{\text{U1CTS}}$	I	ST	Yes	UART1 Clear-to-Send.
$\overline{\text{U1RTS}}$	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	Yes	SPI1 data in.
SDO1	O	—	Yes	SPI1 data out.
$\overline{\text{SS1}}$	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
TMS	I	TTL	No	JTAG Test mode select pin.
TCK	I	TTL	No	JTAG test clock input pin.
TDI	I	TTL	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic; PPS = Peripheral Pin Select; — = Does not apply

Note 1: Not all pins are available on all devices. Refer to the specific device in the **"Pin Diagrams"** section for availability.

2: This pin is available on dsPIC33FJ09GS302 devices only.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS Capable	Description
CMP1A CMP1B CMP1C CMP1D CMP2A CMP2B CMP2C CMP2D	I I I I I I I I	Analog Analog Analog Analog Analog Analog Analog Analog	No No No No No No No No	Comparator 1 Channel A. Comparator 1 Channel B. Comparator 1 Channel C. Comparator 1 Channel D. Comparator 2 Channel A. Comparator 2 Channel B. Comparator 2 Channel C. Comparator 2 Channel D.
DACOUT	O	—	No	DAC output voltage.
ACMP1-ACMP2	O	—	Yes	DAC trigger to PWM module.
ISRC1(2) ISRC2(2) ISRC3(2) ISRC4(2)	O O O O	— — — —	No No No No	Constant Current Source Output 1. Constant Current Source Output 2. Constant Current Source Output 3. Constant Current Source Output 4.
EXTREF	I	Analog	No	External voltage reference input for the reference DACs.
REFCLKO	O	—	Yes	REFCLKO output signal is a postscaled derivative of the system clock.
FLT1-FLT8	I	ST	Yes	Fault inputs to PWM module.
SYNCI1-SYNCI2 SYNCO1 PWM1L PWM1H PWM2L PWM2H PWM4L PWM4H	I O O O O O O O	ST — — — — — — —	Yes Yes No No No No Yes Yes	External synchronization signal to PWM master time base. PWM master time base for external device synchronization. PWM1 low output. PWM1 high output. PWM2 low output. PWM2 high output. PWM4 low output. PWM4 high output.
PGED1 PGEC1 PGED2 PGEC2 PGED3(1) PGEC3(1)	I/O I I/O I I/O I	ST ST ST ST ST ST	No No No No No No	Data I/O pin for programming/debugging Communication Channel 1. Clock input pin for programming/debugging Communication Channel 1. Data I/O pin for programming/debugging Communication Channel 2. Clock input pin for programming/debugging Communication Channel 2. Data I/O pin for programming/debugging Communication Channel 3. Clock input pin for programming/debugging Communication Channel 3.
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times. AVDD is connected to VDD on 18 and 28-pin devices.
AVSS	P	P	No	Ground reference for analog modules. AVSS is connected to VSS on 18 and 28-pin devices.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-Transistor Logic; Analog = Analog input; P = Power; PPS = Peripheral Pin Select; I = Input; O = Output; — = Does not apply

Note 1: Not all pins are available on all devices. Refer to the specific device in the **“Pin Diagrams”** section for availability.

2: This pin is available on dsPIC33FJ09GS302 devices only.

3.0 CPU

> **Note 1:** This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS70204) in the "*dsPIC33F/PIC24H Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies from device to device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

The dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a Data, Address or Address Offset register. The sixteenth working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

There are two classes of instruction: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the devices are capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program-to-data space mapping feature lets any instruction access program space as if it were data space.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits, right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The `MAC` instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

3.5 Arithmetic Logic Unit (ALU)

The ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-Bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.5.1 MULTIPLIER

Using the high-speed, 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.5.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.6 DSP Engine

The DSP engine consists of a high-speed, 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 devices feature a single-cycle instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources can be used concurrently by the same instruction (for example, ED, EDAC).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are `ADD`, `SUB` and `NEG`.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or Integer DSP Multiply (IF)
- Signed or Unsigned DSP Multiply (US)
- Conventional or Convergent Rounding (RND)
- Automatic Saturation On/Off for ACCA (SATA)
- Automatic Saturation On/Off for ACCB (SATB)
- Automatic Saturation On/Off for Writes to Data Memory (SATDW)
- Accumulator Saturation mode Selection (ACCSAT)

A block diagram of the DSP engine is shown in Figure 3-3.

TABLE 3-1: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write Back
`CLR`	$A = 0$	Yes
`ED`	$A = (x - y)^2$	No
`EDAC`	$A = A + (x - y)^2$	No
`MAC`	$A = A + (x * y)$	Yes
`MAC`	$A = A + x^2$	No
`MOVSAC`	No change in A	Yes
`MPY`	$A = x * y$	No
`MPY`	$A = x^2$	No
`MPY.N`	$A = -x * y$	No
`MSC`	$A = A - x * y$	Yes

FIGURE 4-4: DATA MEMORY MAP FOR THE dsPIC33FJ09GS302 DEVICE WITH 1 KB RAM

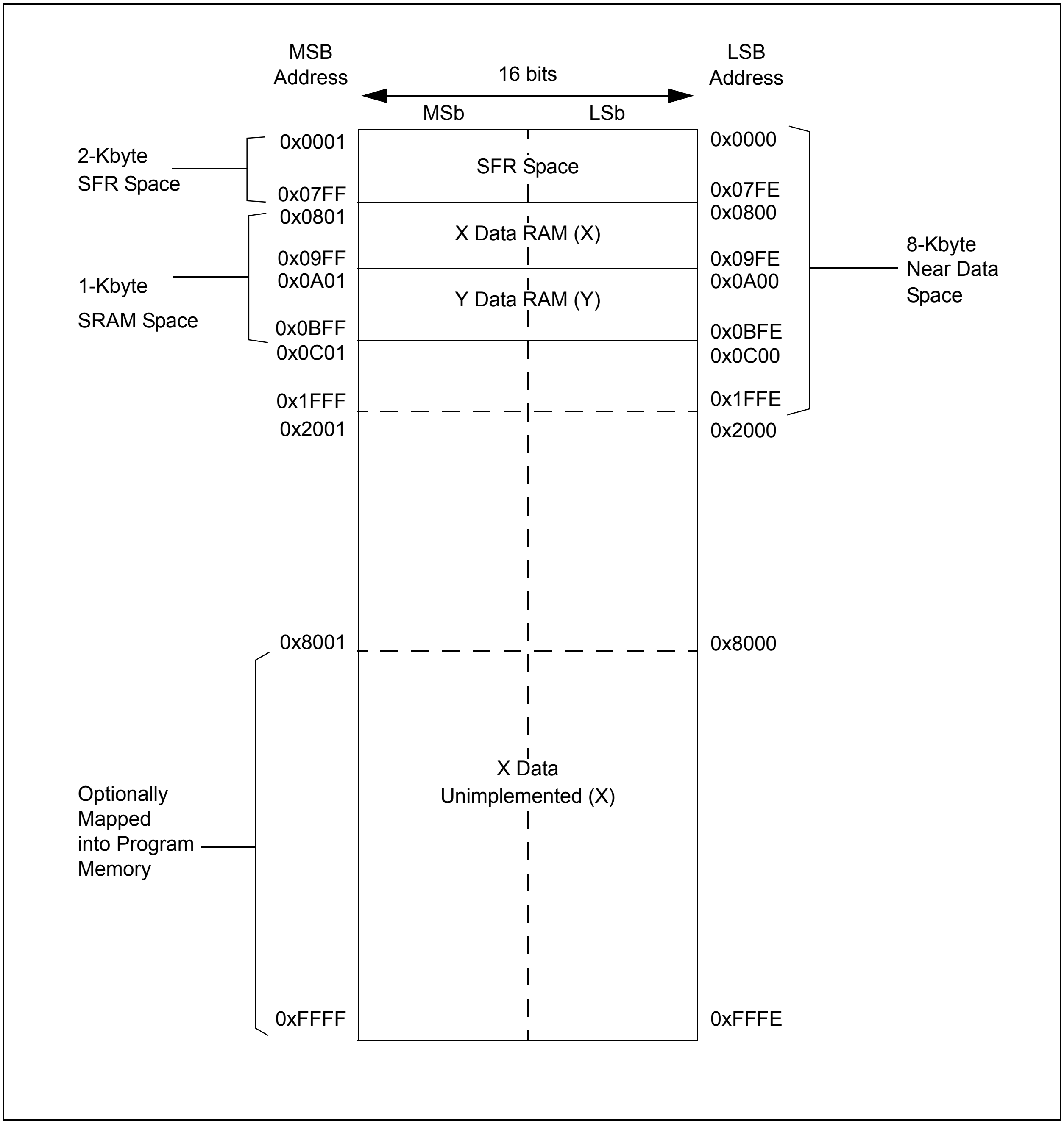


TABLE 4-8: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33FJ09GS302 DEVICES ONLY

File Name	SFR Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0080	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	—	—	ADIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	—	T2IF	—	—	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0086	—	—	INT2IF	—	—	—	—	—	—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS3	008A	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	008C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIF	—	0000
IFS5	008E	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	JTAGIF	0000
IFS6	0090	ADCP1IF	ADCP0IF	—	—	—	—	—	—	AC2IF	—	—	—	—	—	PWM4IF	—	0000
IFS7	0092	—	—	—	—	—	—	—	—	—	—	—	ADCP6IF	—	—	ADCP3IF	ADCP2IF	0000
IEC0	0094	—	—	ADIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	—	T2IE	—	—	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	—	—	INT2IE	—	—	—	—	—	—	—	—	INT1IE	CNIE	AC1IE	MI2C1IE	SI2C1IE	0000
IEC3	009A	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	009C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U1EIE	—	0000
IEC5	009E	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	JTAGIE	0000
IEC6	00A0	ADCP1IE	ADCP0IE	—	—	—	—	—	—	AC2IE	—	—	—	—	—	PWM4IE	—	0000
IEC7	00A2	—	—	—	—	—	—	—	—	—	—	—	ADCP6IE	—	—	ADCP3IE	ADCP2IE	0000
IPC0	00A4	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	00A6	—	T2IP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC2	00A8	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	—	—	—	4440
IPC3	00AA	—	—	—	—	—	—			—	ADIP<2:0>			—	U1TXIP<2:0>			0044
IPC4	00AC	—	CNIP<2:0>			—	AC1IP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	00AE	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC7	00B2	—	—	—	—	—	—	—	—	—	INT2IP<2:0>			—	—	—	—	0040
IPC14	00C0	—	—	—	—	—	—	—	—	—	PSEMIP<2:0>			—	—	—	—	0040
IPC16	00C4	—	—	—	—	—	—	—	—	—	U1EIP<2:0>			—	—	—	—	0040
IPC20	00CC	—	—	—	—	—	—	—	—	—	—	—	—	—	JTAGIP<2:0>			0004
IPC23	00D2	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	00D4	—	—	—	—	—	—	—	—	—	PWM4IP<2:0>			—	—	—	—	0040
IPC25	00D6	—	AC2IP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC27	00DA	—	ADCP1IP<2:0>			—	ADCP0IP<2:0>			—	—			—	—	—	—	4400
IPC28	00DC	—	—	—	—	—	—	—	—	—	ADCP3IP<2:0>			—	ADCP2IP<2:0>			0044
IPC29	00DE	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCP6IP<2:0>			0004
INTTREG	00E0	—	—	—	—	ILR<3:0>				—	VECNUM<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

TABLE 4-16: I2C1 REGISTER MAP

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	Transmit Register								00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator Register									0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	AMSK<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-17: UART1 REGISTER MAP FOR dsPIC33FJ06GS101A, dsPIC33FJ06GS102A, dsPIC33FJ06GS202A AND dsPIC33FJ09GS302

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: SPI1 REGISTER MAP FOR dsPIC33FJ06GS101A, dsPIC33FJ06GS102A, dsPIC33FJ06GS202A AND dsPIC33FJ09GS302

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	—	—	—	—	SPIROV	—	—	—	—	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	—	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.7.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This option provides transparent access to stored constant data from the data space without the need to use special instructions (such as TBLRDL or TBLRDH).

Program space access through the data space occurs if the Most Significant bit of the data space EA is '1' and program space visibility is enabled by setting the PSV bit in the Core Control register (CORCON<2>). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. By incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add a cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address 0x8000 and higher maps directly into a corresponding program memory address (see Figure 4-10), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space location used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

Note:	PSV access is temporarily disabled during table reads/writes.

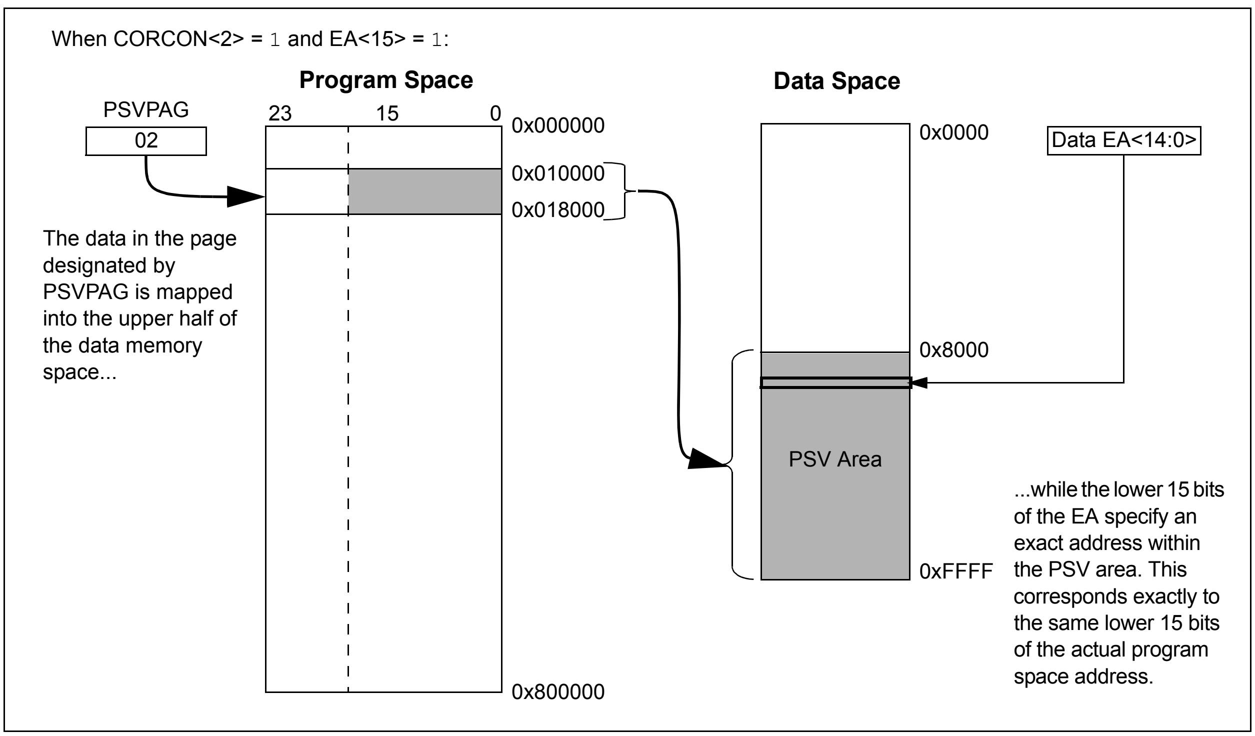
For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions require one instruction cycle in addition to the specified execution time. All other instructions require two instruction cycles in addition to the specified execution time.

For operations that use PSV, and are executed inside a REPEAT loop, these instances require two instruction cycles in addition to the specified execution time of the instruction:

- Execution in the first iteration
- Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction using PSV to access data, to execute in a single cycle.

FIGURE 4-10: PROGRAM SPACE VISIBILITY OPERATION



6.1 Reset Control Register

REGISTER 6-1: RCON: RESET CONTROL REGISTER[1]

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	—	—	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN[2]	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13-10 **Unimplemented:** Read as ‘0’

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has NOT occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset Pin ($\overline{\text{MCLR}}$) bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag (Instruction) bit
1 = A `RESET` instruction has been executed
0 = A `RESET` instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit[2]
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is ‘1’ (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 10-5: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	IC1R<5:0>(1)					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **IC1R<5:0>:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits(1)

111111 = Input tied to Vss
100011 = Input tied to RP35
100010 = Input tied to RP34
100001 = Input tied to RP33
100000 = Input tied to RP32
•
•
•
00000 = Input tied to RP0

Note 1: These bits are not implemented in dsPIC33FJ06GS001/101A/102A devices.

12.0 TIMER2 FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. "Timers"** (DS70205) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Timer2 is a Type B timer with an external clock input (TxCK) that is always synchronized to the internal device clock and the clock synchronization is performed after the prescaler.

The Timer2 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous Counter mode, the input clock is derived from the external clock input at the TxCK pin.

The Timer modes are determined by the following bits:

- TCS (TxCON<1>): Timer Clock Source Control bit
- TGATE (TxCON<6>): Timer Gate Control bit

The Timer control bit settings for different operating modes are given in Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

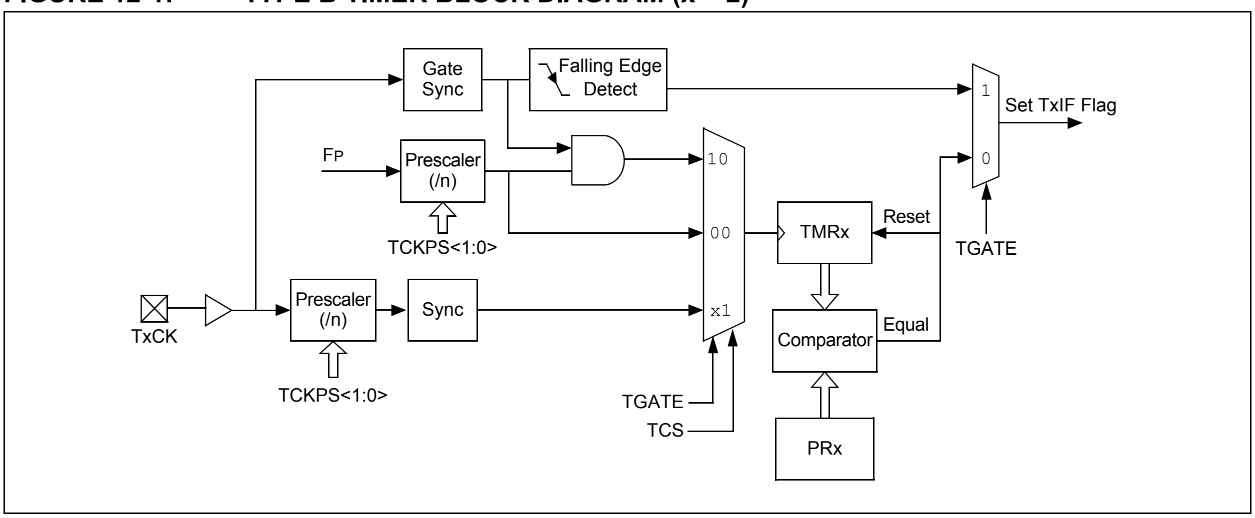
Mode	TCS	TGATE
Timer	0	0
Gated Timer	0	1
Synchronous Counter	1	x

12.1 16-Bit Operation

To configure any of the timers for individual 16-bit operation:

1. Select the timer prescaler ratio using the TCKPS<1:0> bits.
2. Set the Clock and Gating modes using the TCS and TGATE bits.
3. Load the Timer Period value into the PRx register.
4. If interrupts are required, set the Timerx Interrupt Enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
5. Set the TON bit.

FIGURE 12-1: TYPE B TIMER BLOCK DIAGRAM (x = 2)



13.1 Input Capture Registers

REGISTER 13-1: IC1CON: INPUT CAPTURE 1 CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR(1)	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **ICSIDL:** Input Capture Module Stop in Idle Control bit
1 = Input capture module halts in CPU Idle mode
0 = Input capture module continues to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as ‘0’

bit 7 **ICTMR:** Input Capture Timer Select bit(1)
1 = TMR2 contents are captured on capture event
0 = Reserved

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Empty Status bit (read-only)
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode. Rising edge detect only; all other control bits are not applicable.
110 = Unused (module disabled)
101 = Capture mode, every 16th rising edge
100 = Capture mode, every 4th rising edge
011 = Capture mode, every rising edge
010 = Capture mode, every falling edge
001 = Capture mode, every edge (rising and falling). ICI<1:0> bits do not control interrupt generation for this mode.
000 = Input capture module is turned off

Note 1: This bit is not available in dsPIC33FJ06GS001/101A/102A devices.

REGISTER 15-6: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,3)
1 = Center-Aligned mode is enabled
0 = Center-Aligned mode is disabled

bit 1 **XPRES:** External PWM Reset Control bit(4)
1 = Current-limit source resets time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWM time base

bit 0 **IUE:** Immediate Update Enable bit
1 = Updates to the active MDC/PDCx/SDCx registers are immediate
0 = Updates to the active MDC/PDCx/SDCx registers are synchronized to the PWM time base

Note 1: Software must clear the interrupt status here and the corresponding IFSx bit in the interrupt controller.
2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
3: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.
4: To operate in External Period Reset mode, configure the CLMOD (FCLCONx<8>) bit = 0 and ITB (PWMCONx<9>) bit = 1.

REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)(2)
111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
•
•
•
000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)(2)
11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: This bit is not used in Framed SPI modes. Program this bit to ‘0’ for the Framed SPI modes (FRMEN = 1).
2: Do not set both Primary and Secondary prescalers to a value of 1:1.
3: This bit must be cleared when FRMEN = 1.

18.3 UART Registers

REGISTER 18-1: U1MODE: UART1 MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN[1,3]	—	USIDL[3]	IREN[2,3]	RTSMD[3]	—	UEN<1:0>[3]	
bit 15							bit 8

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE[3]	LPBACK[3]	ABAUD[3]	URXINV[3]	BRGH[3]	PDSEL<1:0>[3]		STSEL[3]
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **UARTEN:** UART1 Enable bit[1,3]
- 1 = UART1 is enabled; all UART1 pins are controlled by UART1, as defined by UEN<1:0>
- 0 = UART1 is disabled; all UART1 pins are controlled by port latches; UART1 power consumption is minimal

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **USIDL:** Stop in Idle Mode bit[3]
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit[2,3]
- 1 = IrDA® encoder and decoder are enabled
- 0 = IrDA® encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{U1RTS}}$ Pin bit[3]
- 1 = $\overline{\text{U1RTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{U1RTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **UEN<1:0>:** UART1 Pin Enable bits[3]
- 11 = U1TX, U1RX and BCLK pins are enabled and used; $\overline{\text{U1CTS}}$ pin is controlled by port latches
- 10 = U1TX, U1RX, $\overline{\text{U1CTS}}$ and $\overline{\text{U1RTS}}$ pins are enabled and used
- 01 = U1TX, U1RX and $\overline{\text{U1RTS}}$ pins are enabled and used; $\overline{\text{U1CTS}}$ pin is controlled by port latches
- 00 = U1TX and U1RX pins are enabled and used; $\overline{\text{U1CTS}}$ and $\overline{\text{U1RTS}}$/BCLK pins are controlled by port latches

bit 7 **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit[3]
- 1 = UART1 will continue to sample the U1RX pin; interrupt is generated on falling edge; bit is cleared in hardware on following rising edge
- 0 = No wake-up is enabled

bit 6 **LPBACK:** UART1 Loopback Mode Select bit[3]
- 1 = Enable Loopback mode
- 0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit[3]
- 1 = Enable baud rate measurement on the next character – requires reception of a Sync field (0x55) before other data; cleared in hardware upon completion
- 0 = Baud rate measurement is disabled or completed

Note 1: Refer to **Section 17. “UART”** (DS70188) in the *“dsPIC33F/PIC24H Family Reference Manual”* for information on enabling the UART module for receive or transmit operation.
2: This feature is only available for the 16x BRG mode (BRGH = 0).
3: This bit is not available in the dsPIC33FJ06GS001 device.

TABLE 25-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
	V_{IL}	**Input Low Voltage**					
DI10		I/O Pins	V_{SS}	—	0.2 V_{DD}	V	
DI15		$\overline{MCLR}$	V_{SS}	—	0.2 V_{DD}	V	
DI16		I/O Pins with OSC1	V_{SS}	—	0.2 V_{DD}	V	
DI18		SDA1, SCL1	V_{SS}	—	0.3 V_{DD}	V	SMBus disabled
DI19		SDA1, SCL1	V_{SS}	—	0.8	V	SMBus enabled
	V_{IH}	**Input High Voltage**					
DI20		I/O Pins Not 5V Tolerant(4)	0.7 V_{DD}	—	V_{DD}	V	
DI21		I/O Pins 5V Tolerant(4)	0.7 V_{DD}	—	5.5	V	
DI28		SDA1, SCL1	0.7 V_{DD}	—	5.5	V	SMBus disabled
DI29		SDA1, SCL1	2.1	—	5.5	V	SMBus enabled
	I_{CNPU}	**CNx Pull-up Current**					
DI30			—	250	—	μA	V_{DD} = 3.3V, V_{PIN} = V_{SS}
	I_{IL}	**Input Leakage Current(2,3,4)**					
DI50		I/O Pins: 4x Sink Driver Pins RA0-RA2, RB0-RB2, RB5-RB10, RB15	—	—	±2	μA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance
		16x Sink Driver Pins RA3, RA4, RB3, RB4, RB11-RB14	—	—	±8	μA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance
DI55		$\overline{MCLR}$	—	—	±2	μA	$V_{SS} \le V_{PIN} \le V_{DD}$
DI56		OSC1	—	—	±2	μA	$V_{SS} \le V_{PIN} \le V_{DD}$, XT and HS modes

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See the **“Pin Diagrams”** section for the list of 5V tolerant I/O pins.

5: V_{IL} source < (V_{SS} – 0.3); characterized but not tested.

6: Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V; characterized but not tested.

7: Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins, not excluded under I_{ICL} or I_{ICH} conditions, are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit; characterized but not tested.

25.2 AC Characteristics and Timing Parameters

This section defines dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 AC characteristics and timing parameters.

TABLE 25-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Operating voltage V_{DD} range as described in Table 25-1.

FIGURE 25-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

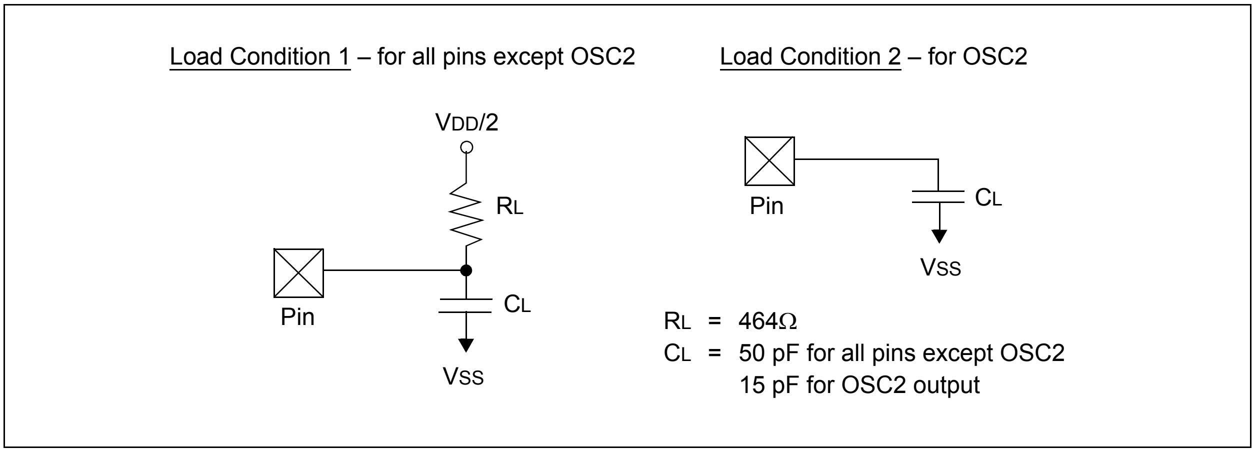
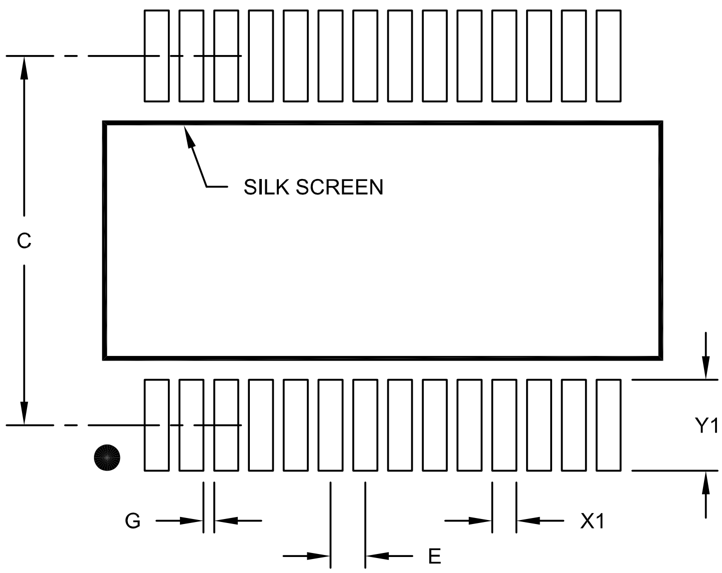


TABLE 25-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	C_{OSCO}	OSC2 Pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	C_{IO}	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	C_B	SCL1, SDA1	—	—	400	pF	In I^{2}C™ mode

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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Fax: 86-24-2334-2393

China - Shenzhen
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Fax: 86-755-8203-1760

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Fax: 86-27-5980-5118

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Fax: 86-29-8833-7256

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Fax: 81-66-152-9310

Japan - Yokohama
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Fax: 81-45-471-6122

Korea - Daegu
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Fax: 82-53-744-4302

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Fax: 82-2-558-5932 or 82-2-558-5934

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Fax: 60-3-6201-9859

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