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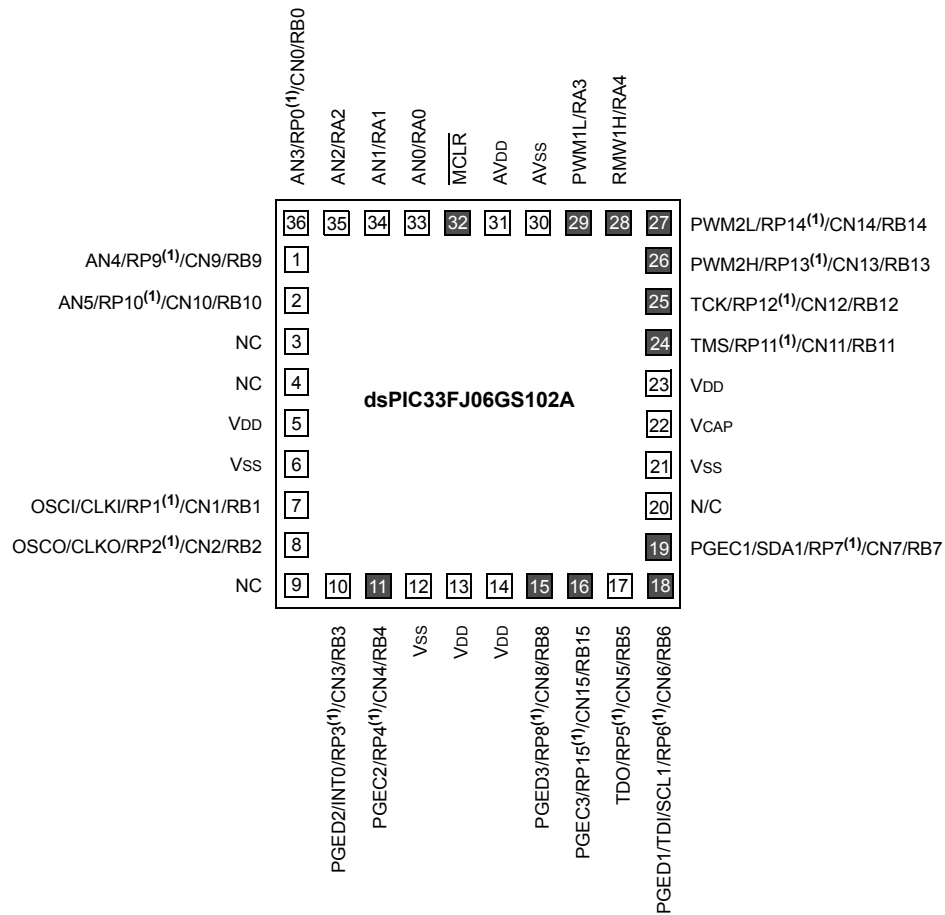
Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	6KB (2K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs202at-i-mm

Pin Diagrams (Continued)

36-Pin VTLA

■ = Pins are up to 5V tolerant



- Note** 1: The RPN pins can be used by any remappable peripheral. See **Table 1** for the list of available peripherals.
 2: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to V_{SS} externally.

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2.5 ICSP™ Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins, are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and Input Voltage High (VIH) and Input Voltage Low (VIL) pin requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins), programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site (www.microchip.com):

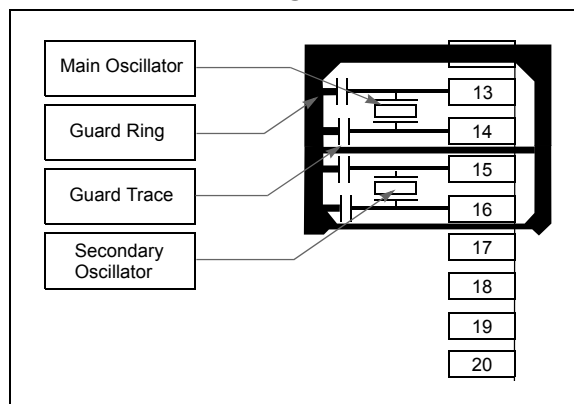
- “Using MPLAB® ICD 3” (poster) (DS51765)
- “Multi-Tool Design Advisory” (DS51764)
- “MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide” (DS51616)
- “Using MPLAB® REAL ICE™” (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 “Oscillator Configuration”** for details).

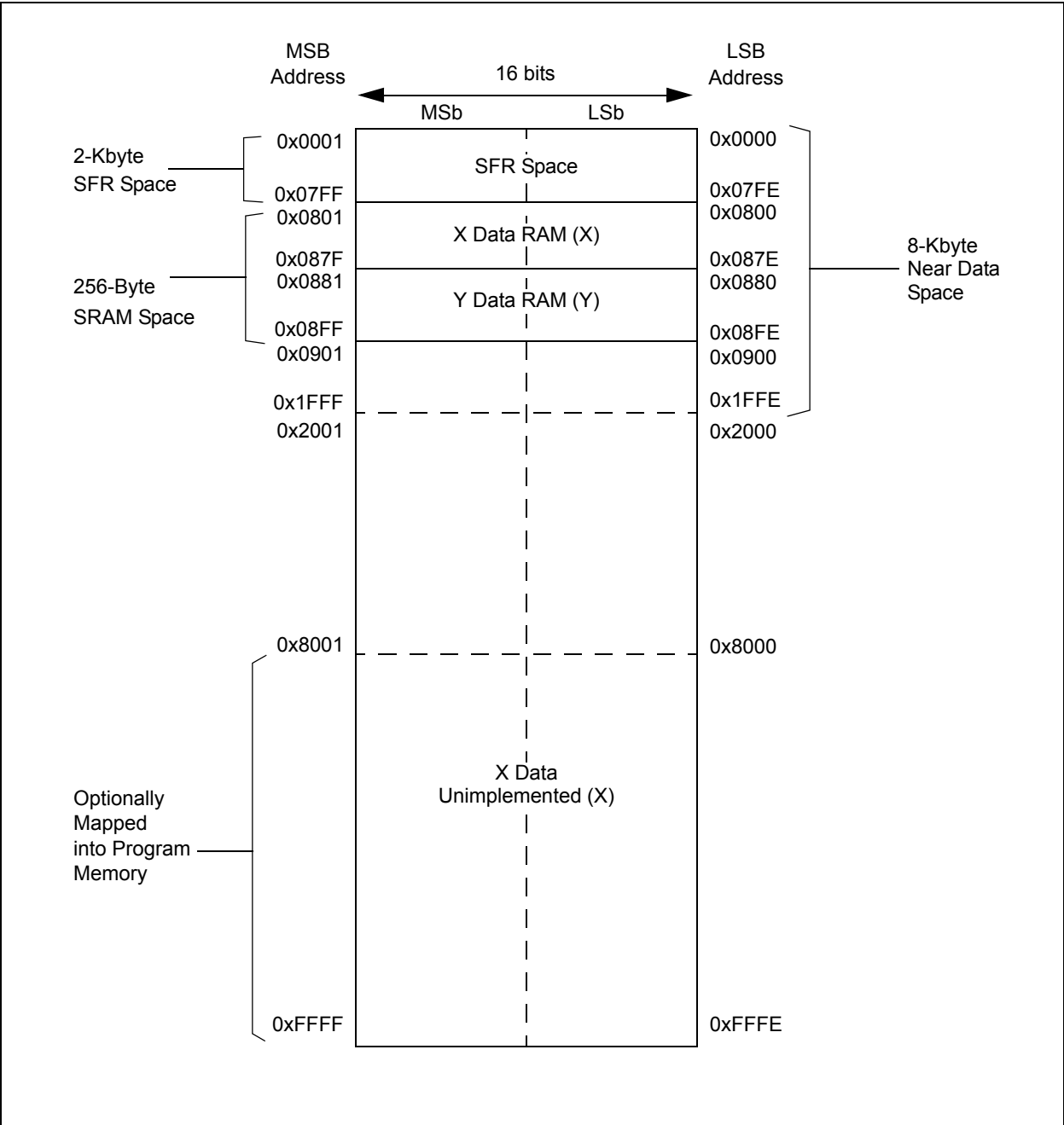
The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

FIGURE 4-3: DATA MEMORY MAP FOR dsPIC33FJ06GS001/101A/102A DEVICES WITH 256 BYTES OF RAM



6.5 External Reset (EXTR)

The external Reset is generated by driving the MCLR pin low. The MCLR pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to **Section 25.0 “Electrical Characteristics”** for minimum pulse width specifications. The external Reset (MCLR) pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the MCLR Reset.

6.5.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate Reset signals to reset multiple devices in the system. This external Reset signal can be directly connected to the MCLR pin to reset the device when the rest of the system is reset.

6.5.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to reset the device, the external Reset pin (MCLR) should be tied directly or resistively to VDD. In this case, the MCLR pin will not be used to generate a Reset. The external Reset pin (MCLR) does not have an internal pull-up and must not be left unconnected.

6.6 Software RESET Instruction (SWR)

Whenever the `RESET` instruction is executed, the device will assert `SYSRST`, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the `RESET` instruction will still remain. `SYSRST` is released at the next instruction cycle and the Reset vector fetch will commence.

The Software Reset (SWR) flag (instruction) in the Reset Control register (RCON<6>) is set to indicate the software Reset.

6.7 Watchdog Time-out Reset (WDTO)

Whenever a Watchdog Timer time-out occurs, the device will asynchronously assert `SYSRST`. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out (WDTO) flag in the Reset Control (RCON<4>) register is set to indicate the Watchdog Timer Reset. Refer to **Section 22.4 “Watchdog Timer (WDT)”** for more information on Watchdog Reset.

6.8 Trap Conflict Reset

If a lower priority hard trap occurs, while a higher priority trap is being processed, a hard Trap Conflict Reset occurs. The hard traps include exceptions of Priority Level 13 through Level 15, inclusive. The address error (Level 13) and oscillator error (Level 14) traps fall into this category.

The Trap Reset (TRAPR) flag in the Reset Control register (RCON<15>) is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 “Interrupt Controller”** for more information on Trap Conflict Resets.

6.9 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The illegal opcode or Uninitialized W Access Reset (IOPUWR) flag in the Reset Control register (RCON<14>) is set to indicate the illegal condition device Reset.

6.9.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 0x3F, which is an illegal opcode value.

6.9.2 UNINITIALIZED W REGISTER RESET

Any attempt to use the uninitialized W register as an Address Pointer will Reset the device. The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to.

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 7-9: IFS5: INTERRUPT FLAG STATUS REGISTER 5

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
PWM2IF ⁽¹⁾	PWM1IF	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	JTAGIF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **PWM2IF:** PWM2 Interrupt Flag Status bit⁽¹⁾

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 14 **PWM1IF:** PWM1 Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 13-1 **Unimplemented:** Read as '0'

bit 0 **JTAGIF:** JTAG Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

Note 1: This bit is not implemented in dsPIC33FJ06GS001/101A devices.

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 7-11: IFS7: INTERRUPT FLAG STATUS REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	—	ADCP6IF	—	—	ADCP3IF ⁽¹⁾	ADCP2IF ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **ADCP6IF:** ADC Pair 6 Conversion Done Interrupt Flag Status bit

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **ADCP3IF:** ADC Pair 3 Conversion Done Interrupt Flag Status bit⁽¹⁾

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

bit 0 **ADCP2IF:** ADC Pair 2 Conversion Done Interrupt Flag Status bit⁽²⁾

1 = Interrupt request has occurred

0 = Interrupt request has not occurred

Note 1: This bit is not implemented in dsPIC33FJ06GS102A/202A devices.

2: This bit is not implemented in dsPIC33FJ06GS001/101A devices.

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 7-24: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—	INT1IP<2:0>		
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

REGISTER 7-25: IPC7: INTERRUPT PRIORITY CONTROL REGISTER 7

U-0	U-1	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	INT2IP<2:0>			—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **INT2IP<2:0>:** External Interrupt 2 Priority bits

111 = Interrupt is Priority 7 (highest priority interrupt)

•
•
•

001 = Interrupt is Priority 1

000 = Interrupt source is disabled

bit 3-0 **Unimplemented:** Read as '0'

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 10-3: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T1CKR<5:0>					
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **T1CKR<5:0>:** Assign Timer1 External Clock (T1CK) to the Corresponding RPn Pin bits

111111 = Input tied to Vss
 100011 = Input tied to RP35
 100010 = Input tied to RP34
 100001 = Input tied to RP33
 100000 = Input tied to RP32

•
•
•

00000 = Input tied to RP0

bit 7-0 **Unimplemented:** Read as '0'

dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302

REGISTER 15-7: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8> ⁽²⁾							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0> ⁽²⁾							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PDCx<15:0>**: PWMx Generator # Duty Cycle Value bits⁽²⁾

- Note 1:** In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL. The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period-0x0008.
- 2:** As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSBs.

REGISTER 15-8: SDCx: PWMx SECONDARY DUTY CYCLE REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<15:8> ⁽²⁾							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<7:0> ⁽²⁾							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **SDCx<15:0>**: Secondary Duty Cycle for PWMxL Output Pin bits⁽²⁾

- Note 1:** The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle. The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period-0x0008.
- 2:** As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSB to 3 LSBs.

REGISTER 17-2: I2C1STAT: I2C1 STATUS REGISTER (CONTINUED)

- bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.
- bit 2 **R_W:** Read/Write Information bit (when operating as I²C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware is set or clear after reception of I²C device address byte.
- bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2C1RCV is full
0 = Receive is not complete, I2C1RCV is empty
Hardware is set when I2C1RCV is written with received byte. Hardware is clear when software reads I2C1RCV.
- bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit is in progress, I2C1TRN is full
0 = Transmit is complete, I2C1TRN is empty
Hardware is set when software writes I2C1TRN. Hardware is clear at completion of data transmission.

18.3 UART Registers

REGISTER 18-1: U1MODE: UART1 MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN ^(1,3)	—	USIDL ⁽³⁾	IREN ^(2,3)	RTSMD ⁽³⁾	—	UEN<1:0> ⁽³⁾	
bit 15						bit 8	

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE ⁽³⁾	LPBACK ⁽³⁾	ABAUD ⁽³⁾	URXINV ⁽³⁾	BRGH ⁽³⁾	PDSEL<1:0> ⁽³⁾		STSEL ⁽³⁾
bit 7						bit 0	

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **UARTEN:** UART1 Enable bit^(1,3)
 1 = UART1 is enabled; all UART1 pins are controlled by UART1, as defined by UEN<1:0>
 0 = UART1 is disabled; all UART1 pins are controlled by port latches; UART1 power consumption is minimal
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **USIDL:** Stop in Idle Mode bit⁽³⁾
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **IREN:** IrDA[®] Encoder and Decoder Enable bit^(2,3)
 1 = IrDA[®] encoder and decoder are enabled
 0 = IrDA[®] encoder and decoder are disabled
- bit 11 **RTSMD:** Mode Selection for U1RTS Pin bit⁽³⁾
 1 = U1RTS pin is in Simplex mode
 0 = U1RTS pin is in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UART1 Pin Enable bits⁽³⁾
 11 = U1TX, U1RX and BCLK pins are enabled and used; U1CTS pin is controlled by port latches
 10 = U1TX, U1RX, U1CTS and U1RTS pins are enabled and used
 01 = U1TX, U1RX and U1RTS pins are enabled and used; U1CTS pin is controlled by port latches
 00 = U1TX and U1RX pins are enabled and used; U1CTS and U1RTS/BCLK pins are controlled by port latches
- bit 7 **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit⁽³⁾
 1 = UART1 will continue to sample the U1RX pin; interrupt is generated on falling edge; bit is cleared in hardware on following rising edge
 0 = No wake-up is enabled
- bit 6 **LPBACK:** UART1 Loopback Mode Select bit⁽³⁾
 1 = Enable Loopback mode
 0 = Loopback mode is disabled
- bit 5 **ABAUD:** Auto-Baud Enable bit⁽³⁾
 1 = Enable baud rate measurement on the next character – requires reception of a Sync field (0x55) before other data; cleared in hardware upon completion
 0 = Baud rate measurement is disabled or completed

Note 1: Refer to **Section 17. “UART”** (DS70188) in the “dsPIC33F/PIC24H Family Reference Manual” for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

3: This bit is not available in the dsPIC33FJ06GS001 device.

REGISTER 19-2: ADSTAT: ADC STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	R/C-0, HS	U-0	U-0	R/C-0, HS	R/C-0, HS	R/C-0, HS	R/C-0, HS
—	P6RDY	—	—	P3RDY ⁽¹⁾	P2RDY ⁽²⁾	P1RDY	P0RDY
bit 7				bit 0			

Legend:	C = Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-7 **Unimplemented:** Read as '0'
- bit 6 **P6RDY:** Conversion Data for Pair 6 Ready bit
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3 **P3RDY:** Conversion Data for Pair 3 Ready bit⁽¹⁾
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.
- bit 2 **P2RDY:** Conversion Data for Pair 3 Ready bit⁽²⁾
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.
- bit 1 **P1RDY:** Conversion Data for Pair 1 Ready bit
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.
- bit 0 **P0RDY:** Conversion Data for Pair 0 Ready bit
Bit is set when data is ready in buffer, cleared when a '0' is written to this bit.

- Note 1:** This bit is not implemented in dsPIC33FJ06GS102A/202A devices.
- 2:** This bit is not implemented in dsPIC33FJ06GS001/101A devices.

21.3 Current Source Control Register

REGISTER 21-1: ISRCCON: CONSTANT CURRENT SOURCE CONTROL REGISTER⁽¹⁾

R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
ISRCEN	—	—	—	—	OUTSEL<2:0>		
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	ISRCCAL<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ISRCEN:** Current Source Enable bit

1 = Current source is enabled

0 = Current source is disabled

bit 14-11 **Unimplemented:** Read as '0'

bit 10-8 **OUTSEL<2:0>:** Output Current Select bits

111 = Reserved

110 = Reserved

101 = Reserved

100 = Select input pin, ISRC4 (AN4)

011 = Select input pin, ISRC3 (AN5)

010 = Select input pin, ISRC2 (AN6)

001 = Select input pin, ISRC1 (AN7)

000 = No output is selected

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ISRCCAL<5:0>:** Current Source Calibration bits

The calibration value must be copied from Flash address, 0x800840, into these bits. Refer to the Constant Current Source Calibration Register (Register 22-1) in **Section 22.0 "Special Features"** for more information.

Note 1: This register is available in the dsPIC33FJ09GS302 device only.

24.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C® for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
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- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

24.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

24.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

24.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

24.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

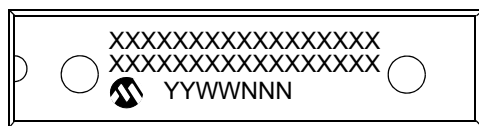
24.10 PICkit 3 In-Circuit Debugger/Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

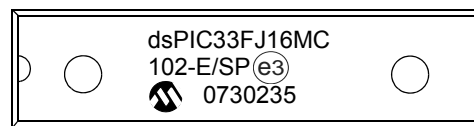
The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

27.1 Package Marking Information (Continued)

28-Lead SPDIP



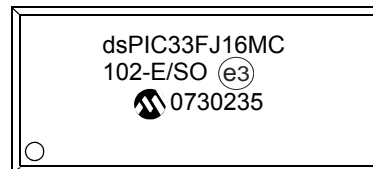
Example



28-Lead SOIC



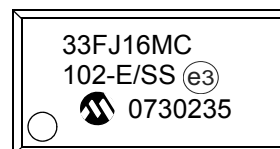
Example



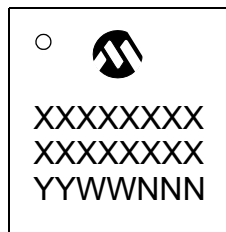
28-Lead SSOP



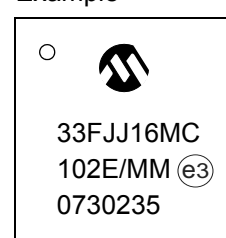
Example



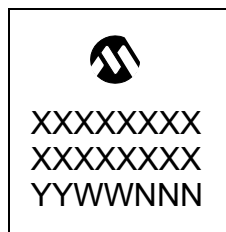
28-Lead QFN-S



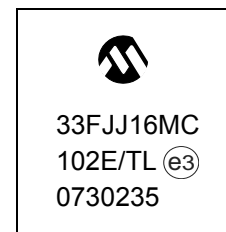
Example



36-Lead VTLA



Example



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