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#### Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	9KB (3K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj09gs302-e-so

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### 3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. The output of the 17-bit x 17-bit multiplier/scaler is a 33-bit value that is sign-extended to 40 bits. Integer data is inherently represented as a signed 2's complement value, where the Most Significant bit (MSb) is defined as a sign bit. The range of an N-bit 2's complement integer is  $-2^{N-1}$  to  $2^{N-1} - 1$ .

- For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF) including 0
- For a 32-bit integer, the data range is
  -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF)

When the multiplier is configured for fractional multiplication, the data is represented as a 2's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit 2's complement fraction with this implied radix point is -1.0 to  $(1 - 2^{1-N})$ . For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518x10<sup>-5</sup>. In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product that has a precision of 4.65661 x 10<sup>-10</sup>.

The same multiplier is used to support the MCU multiply instructions, which include integer 16-bit signed, unsigned and mixed-sign multiply operations.

The MUL instruction can be directed to use byte or word-sized operands. Byte operands will direct a 16-bit result, and word operands will direct a 32-bit result to the specified register(s) in the W array.

# 3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/ subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its preaccumulation source and post-accumulation destination. For the ADD and LAC instructions, the data to be accumulated or loaded can be optionally scaled using the barrel shifter prior to accumulation.

# 3.6.2.1 Adder/Subtracter, Overflow and Saturation

The adder/subtracter is a 40-bit adder with an optional zero input into one side, and either true or complement data into the other input.

- In the case of addition, the Carry/Borrow input is active-high and the other input is true data (not complemented)
- In the case of subtraction, the Carry/Borrow input is active-low and the other input is complemented

The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS register:

- Overflow from bit 39: This is a catastrophic overflow in which the sign of the accumulator is destroyed
- Overflow into guard bits, 32 through 39: This is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block that controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described previously and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value to saturate.

Six STATUS register bits support saturation and overflow:

- · OA: ACCA overflowed into guard bits
- OB: ACCB overflowed into guard bits
- SA: ACCA saturated (bit 31 overflow and saturation) or

ACCA overflowed into guard bits and saturated (bit 39 overflow and saturation)

SB: ACCB saturated (bit 31 overflow and saturation)

ACCB overflowed into guard bits and saturated (bit 39 overflow and saturation)

- · OAB: Logical OR of OA and OB
- · SAB: Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when set and the corresponding Overflow Trap Enable bits (OVATE, OVBTE) in the INTCON1 register are set (refer to **Section 7.0 "Interrupt Controller"**). This allows the user application to take immediate action, for example, to correct system gain.

The SA and SB bits are modified each time data passes through the adder/subtracter, but can only be cleared by the user application. When set, they indicate that the accumulator has overflowed its maximum range (bit 31 for 32-bit saturation or bit 39 for 40-bit saturation) and will be saturated (if saturation is enabled). When saturation is not enabled, SA and SB default to bit 39 overflow and thus, indicate that a catastrophic overflow has occurred. If the COVTE bit in the INTCON1 register is set, SA and SB bits will generate an arithmetic warning trap when saturation is disabled.

The Overflow and Saturation Status bits can optionally be viewed in the STATUS Register (SR) as the logical OR of OA and OB (in bit OAB) and the logical OR of SA and SB (in bit SAB). Programmers can check one bit in the STATUS Register to determine if either accumulator has overflowed, or one bit to determine if either accumulator has saturated. This is useful for complex number arithmetic, which typically uses both accumulators.

The device supports three Saturation and Overflow modes:

- Bit 39 Overflow and Saturation: When bit 39 overflow and saturation occurs, the saturation logic loads the maximally positive 9.31 (0x7FFFFFFF) or maximally negative 9.31 value (0x800000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user application. This condition is referred to as 'super saturation' and provides protection against erroneous data or unexpected algorithm problems (such as gain calculations).
- Bit 31 Overflow and Saturation: When bit 31 overflow and saturation occurs, the saturation logic then loads the maximally positive 1.31 value (0x007FFFFFF) or maximally negative 1.31 value (0x008000000) into the target accumulator. The SA or SB bit is set and remains set until cleared by the user application. When this Saturation mode is in effect, the guard bits are not used, so the OA, OB or OAB bits are never set.
- Bit 39 Catastrophic Overflow: Bit 39 Overflow Status bit, from the adder, is used to set the SA or SB bit, which remains set until cleared by the user application. No saturation operation is performed, and the accumulator is allowed to overflow, destroying its sign. If the COVTE bit in the INTCON1 register is set, a catastrophic overflow can initiate a trap exception.

### 3.6.3 ACCUMULATOR 'WRITE BACK'

The MAC class of instructions (with the exception of MPY, MPY.N, ED and EDAC) can optionally write a rounded version of the high word (bits 31 through 16) of the accumulator that is not targeted by the instruction into data space memory. The write is performed across the X bus into combined X and Y address space. The following addressing modes are supported:

- W13, Register Direct: The rounded contents of the non-target accumulator are written into W13 as a 1.15 fraction.
- [W13] + = 2, Register Indirect with Post-Increment: The rounded contents of the non-target accumulator are written into the address pointed to by W13 as a 1.15 fraction. W13 is then incremented by 2 (for a word write).

### 3.6.3.1 Round Logic

The round logic is a combinational block that performs a conventional (biased) or convergent (unbiased) round function during an accumulator write (store). The Round mode is determined by the state of the RND bit in the CORCON register. It generates a 16-bit, 1.15 data value that is passed to the data space write saturation logic. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word is simply discarded.

Conventional rounding zero-extends bit 15 of the accumulator and adds it to the ACCxH word (bits 16 through 31 of the accumulator).

- If the ACCxL word (bits 0 through 15 of the accumulator) is between 0x8000 and 0xFFFF (0x8000 included), ACCxH is incremented
- If ACCxL is between 0x0000 and 0x7FFF, ACCxH is left unchanged

A consequence of this algorithm is that over a succession of random rounding operations, the value tends to be biased slightly positive.

Convergent (or unbiased) rounding operates in the same manner as conventional rounding, except when ACCxL equals 0x8000. In this case, the Least Significant bit (bit 16 of the accumulator) of ACCxH is examined:

- If it is '1', ACCxH is incremented
- If it is '0', ACCxH is not modified

Assuming that bit 16 is effectively random in nature, this scheme removes any rounding bias that may accumulate.

The SAC and SAC.R instructions store either a truncated (SAC), or rounded (SAC.R) version of the contents of the target accumulator to data memory via the X bus, subject to data saturation (see **Section 3.6.3.2 "Data Space Write Saturation**"). For the MAC class of instructions, the accumulator writeback operation functions in the same manner, addressing combined MCU (X and Y) data space though the X bus. For this class of instructions, the data is always subject to rounding.

#### 3.6.3.2 Data Space Write Saturation

In addition to adder/subtracter saturation, writes to data space can also be saturated, but without affecting the contents of the source accumulator. The data space write saturation logic block accepts a 16-bit, 1.15 fractional value from the round logic block as its input, together with overflow status from the original source (accumulator) and the 16-bit round adder. These inputs are combined and used to select the appropriate 1.15 fractional value as output to write to data space memory.

If the SATDW bit in the CORCON register is set, data (after rounding or truncation) is tested for overflow and adjusted accordingly:

- For input data greater than 0x007FFF, data written to memory is forced to the maximum positive 1.15 value, 0x7FFF
- For input data less than 0xFF8000, data written to memory is forced to the maximum negative 1.15 value, 0x8000

The Most Significant bit of the source (bit 39) is used to determine the sign of the operand being tested.

If the SATDW bit in the CORCON register is not set, the input data is always passed through unmodified under all conditions.

#### 3.6.4 BARREL SHIFTER

The barrel shifter can perform up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts in a single cycle. The source can be either of the two DSP accumulators or the X bus (to support multi-bit shifts of register or memory data).

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

The barrel shifter is 40 bits wide, thereby obtaining a 40-bit result for DSP shift operations and a 16-bit result for MCU shift operations. Data from the X bus is presented to the barrel shifter between bit positions 16 and 31 for right shifts, and between bit positions 0 and 15 for left shifts.

## 4.5 Modulo Addressing

Modulo Addressing mode is a method used to provide an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or program space (since the data pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

#### 4.5.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y	space	Modulo	Addressing	EA	
	calculations		assume	word-sized	data	
	(LSb of every EA is always clear).					

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

#### 4.5.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that will operate with Modulo Addressing:

- If XWM = 15, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 15, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than '15' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '15' and the YMODEN bit is set at MODCON<14>.

#### FIGURE 4-6: MODULO ADDRESSING OPERATION EXAMPLE



<b>REGISTER 7</b>	-9: IFS5: I	NTERRUPT	FLAG STAT	US REGIST	ER 5		
R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
PWM2IF <sup>(1)</sup>	PWM1IF				—		
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—			—	—	—		JTAGIF
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15	PWM2IF: PW	M2 Interrupt F	ag Status bit <sup>(</sup>	1)			
	1 = Interrupt r	equest has oc	curred				
	0 = Interrupt r	request has not	occurred				
bit 14	PWM1IF: PW	M1 Interrupt F	ag Status bit				
	1 = Interrupt r	equest has oc	curred				
	0 = Interrupt r	equest has not	ccurred				
bit 13-1	Unimplemen	ted: Read as '	0'				
bit 0	JTAGIF: JTA	G Interrupt Flag	g Status bit				
	1 = Interrupt r	equest has oc	curred				
	0 = Interrupt r	request has not	occurred				

Note 1: This bit is not implemented in dsPIC33FJ06GS001/101A devices.

REGISTER	7-31. IPC2	D. INTERRUP		CONTROL	REGISTER 2	)	
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
		AC2IP<2:0>(1)					_
bit 15	·					·	bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	_	_	—	_	_	_
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplei	mented bit, read	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	'0' = Bit is cleared x = Bit is unknown		
bit 15	Unimpleme	nted: Read as '	0,		(4)		
bit 14-12	AC2IP<2:0>	Analog Compa	arator 2 Inter	rupt Priority bits	;(1)		
	111 = Interr	upt is Priority 7 (	highest prior	ity)			
	•						
	•						

#### DECISTED 7 21. IDC25, INTERRURT REIORITY CONTROL RECIETER 25

000 = Interrupt source is disabled

001 = Interrupt is Priority 1

bit 11-0 Unimplemented: Read as '0'

Note 1: These bits are not implemented in dsPIC33FJ06GS101A/102A devices.

<b>REGISTER 8-</b>	3: PLLFI	BD: PLL FEE	DBACK DIV	ISOR REGIS	STER <sup>(1)</sup>		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
_	_	—	—	—	—		PLLDIV8
bit 15							bit 8
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
			PLLDI	V<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimplemented bit, rea		id as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-9 bit 8-0	Unimplemen PLLDIV<8:0> 111111111 =	ted: Read as '( •: PLL Feedbac = 513 = 50 (default) = 4 = 3 = 2	o' ck Divisor bits	(also denoted	as 'M', PLL mul	tiplier)	

Note 1: This register is reset only on a Power-on Reset (POR).

### 9.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 9.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device will wake-up from Idle mode on any of these events:

- · Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction, or the first instruction in the ISR.

#### 9.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

## 9.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this may not be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate. Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

# 9.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers will have no effect and read values will be invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC<sup>®</sup> DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

**Note:** If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

#### 10.6.2.3 Virtual Pins

Four virtual RPn pins (RP32, RP33, RP34 and RP35) are supported, which are identical in functionality to all other RPn pins, with the exception of pinouts. These four pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP32 and the PWM Fault input can be configured for RP32 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

# 10.6.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. dsPIC33F devices include three features to prevent alterations to the peripheral map:

- · Control register lock sequence
- Continuous state monitoring
- Configuration bit pin select lock

#### 10.6.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

- 1. Write 0x46 to OSCCON<7:0>.
- 2. Write 0x57 to OSCCON<7:0>.
- 3. Clear (or set) IOLOCK as a single operation.



Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence, followed by an update to all control registers, then locked with a second lock sequence.

#### 10.6.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset will be triggered.

#### 10.6.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC<5>) Configuration bit blocks the IOLOCK bit from being cleared, after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute and the Peripheral Pin Select Control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

### 14.1 Output Compare Modes

Configure the Output Compare modes by setting the appropriate Output Compare Mode (OCM<2:0>) bits in the Output Compare Control (OC1CON<2:0>) register. Table 14-1 lists the different bit settings for the Output Compare modes. Figure 14-2 illustrates the output compare operation for various modes. The user

TABLE 14-1: OUTPUT COMPARE MODES

application must disable the associated timer when writing to the Output Compare Control registers to avoid malfunctions.

Note:	Refer to Section 13. "Output Compare"							
	(DS70209) in the "dsPIC33F/PIC24H							
	Family Reference Manual" for OC1R and							
	OC1RS register restrictions.							

OCM<2:0>	Mode	OC1 Pin Initial State	OC1 Interrupt Generation	
000	Module Disabled	Controlled by GPIO register		
001	Active-Low One-Shot	0	OC1 rising edge	
010	Active-High One-Shot	1	OC1 falling edge	
011	Toggle	Current output is maintained	OC1 rising and falling edge	
100	Delayed One-Shot	0	OC1 falling edge	
101	Continuous Pulse	0	OC1 falling edge	
110	PWM without Fault Protection	<ul><li>'0' if OC1R is zero,</li><li>'1' if OC1R is non-zero</li></ul>	No interrupt	
111	PWM with Fault Protection	<ul><li>'0' if OC1R is zero,</li><li>'1' if OC1R is non-zero</li></ul>	OCFA falling edge for OC1 to OC4	





#### REGISTER 15-4: SEVTCMP: PWM SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVTCN	IP <15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	SE	EVTCMP <7:3>	—	—	—		
bit 7							bit 0
I a manual.							

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 SEVTCMP<15:3>: Special Event Compare Count Value bits bit 2-0 Unimplemented: Read as '0'

#### REGISTER 15-5: MDC: PWM MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDC<	15:8> <sup>(1,2)</sup>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MDC	<7:0> <sup>(1,2)</sup>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimplemented bit, read as '0'			
-n = Value at P	OR	'1' = Bit is set '0' = Bit is cleared x = Bit is unl			x = Bit is unkr	nown	

bit 15-0 MDC<15:0>: Master PWM Duty Cycle Value bits<sup>(1,2)</sup>

**Note 1:** The smallest pulse width that can be generated on the PWM output corresponds to a value of 0x0009, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWM period (0 ns-40 ns, depending on the mode of operation), the PWM duty cycle resolution will degrade from 1 LSb to 3 LSbs.

# 16.0 SERIAL PERIPHERAL INTERFACE (SPI)

- Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/ 202A and dsPIC33FJ09GS302 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 18. "Serial Peripheral Interface (SPI)" (DS70206) of the "dsPIC33F/ PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters, etc. The SPI module is compatible with Motorola<sup>®</sup> SPI and SIOP.

Each SPI module consists of a 16-bit shift register, SPIxSR (where x = 1 or 2), used for shifting data in and out, and a buffer register, SPIxBUF. A control register, SPIxCON, configures the module. Additionally, a status register, SPIxSTAT, indicates status conditions.

The serial interface consists of 4 pins:

- · SDIx (serial data input)
- · SDOx (serial data output)
- · SCKx (shift clock input or output)
- SSx (active-low slave select)

In Master mode operation, SCKx is a clock output; in Slave mode, it is a clock input.



#### FIGURE 16-1: SPI MODULE BLOCK DIAGRAM

# 18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

- Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/ 202A and dsPIC33FJ09GS302 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "UART" (DS70188) in the "dsPIC33F/PIC24H Family Reference Manual", which is available on the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Universal Asynchronous Receiver Transmitter (UART) module is a serial I/O module. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the U1CTS and U1RTS pins, and also includes an IrDA<sup>®</sup> encoder and decoder.

Note:	The dsPIC33FJ06GS001 device does not
	have a UART module.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission through the U1TX and U1RX pins
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware flow control option with U1CTS and U1RTS pins
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 10 Mbps to 38 bps at 40 MIPS
- 4-deep First-In First-Out (FIFO) transmit data buffer
- · 4-deep FIFO receive data buffer
- · Parity, framing and buffer overrun error detection
- Support for 9-bit mode with address detect (9th bit = 1)
- · Transmit and Receive interrupts
- Separate interrupt for all UART error conditions
- · Loopback mode for diagnostic support
- · Support for Sync and Break characters
- Support for automatic baud rate detection
- IrDA encoder and decoder logic
- 16x baud clock output for IrDA<sup>®</sup> support

A simplified block diagram of the UART module is shown in Figure 18-1. The UART module consists of these key hardware elements:

- BRG
- · Asynchronous transmitter
- · Asynchronous receiver

### FIGURE 18-1: UART SIMPLIFIED BLOCK DIAGRAM



# 20.0 HIGH-SPEED ANALOG COMPARATOR

- Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS001/101A/102A/ 202A and dsPIC33FJ09GS302 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 45. "High-Speed Analog Comparator" (DS70296) in the "dsPIC33F/PIC24H Family Reference Manual", which is available on the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The high-speed analog comparator module monitors current and/or voltage transients that may be too fast for the CPU and ADC to capture.

### 20.1 Features Overview

The SMPS comparator module offers the following major features:

- · Eight selectable comparator inputs
- · Up to two analog comparators
- · 10-bit DAC for each analog comparator
- · Programmable output polarity
- Interrupt generation capability

- DACOUT pin to provide DAC output
- DACOUT amplifier (1x, 1.8x)
- Selectable hysteresis
- DAC has three ranges of operation:
  - AVDD/2
  - Internal Reference (INTREF)
  - External Reference (EXTREF)
- · ADC sample and convert trigger capability
- · Disable capability reduces power consumption
- · Functional support for PWM module:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

### 20.2 Module Description

Figure 20-1 shows a functional block diagram of one analog comparator from the high-speed analog comparator module. The analog comparator provides high-speed operation with a typical delay of 20 ns. The comparator has a typical offset voltage of  $\pm 5$  mV. The negative input of the comparator is always connected to the DAC circuit. The positive input of the comparator is connected to an analog multiplexer that selects the desired source pin.

The analog comparator input pins are typically shared with pins used by the Analog-to-Digital Converter (ADC) module. Both the comparator and the ADC can use the same pins at the same time. This capability enables a user to measure an input voltage with the ADC and detect voltage transients with the comparator.



FIGURE 20-1: HIGH-SPEED ANALOG COMPARATOR MODULE BLOCK DIAGRAM

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	_		—	CMREF	<9:8> <sup>(1)</sup>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CMREF	<sup>=</sup> <7:0> <sup>(1)</sup>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-10	Unimplemen	ted: Read as 'o	)'				
bit 9-0	CMREF<9:0>	Comparator F	Reference Vo	ltage Select bit	ts <sup>(1)</sup>		
	1111111111	= (CMREF * II	NTREF/1024)	or (CMREF *	(AVDD/2)/1024)	volts dependir	ng on RANGE
		bit or (CMRE	EF * EXTREF	/1024) if EXTF	REF is set		
	•						
	•						
	•						
	0000000000	= 0.0 volts					

# REGISTER 20-2: CMPDACx: COMPARATOR DAC CONTROL x REGISTER

**Note 1:** These bits are not implemented in dsPIC33FJ06GS101A/102A devices.

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all table reads and writes and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note:	For more details	on the inst	ruction set,
	refer to the "16	6-Bit MCU	and DSC
	Programmer's	Reference	Manual"
	(DS70157).		

Field	Description
#text	Means "literal defined by text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m></n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.W	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word-addressed instructions) $\in \{015\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x00000x1FFF}
lit1	1-bit unsigned literal $\in \{0,1\}$
lit4	4-bit unsigned literal $\in \{015\}$
lit5	5-bit unsigned literal $\in \{031\}$
lit8	8-bit unsigned literal $\in$ {0255}
lit10	10-bit unsigned literal $\in$ {0255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal $\in \{016384\}$
lit16	16-bit unsigned literal $\in \{065535\}$
lit23	23-bit unsigned literal $\in$ {08388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal $\in$ {-512511}
Slit16	16-bit signed literal ∈ {-3276832767}
Slit6	6-bit signed literal $\in$ {-1616}
Wb	Base W register ∈ {W0W15}
Wd	Destination W register $\in$ { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

TABLE 23-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

	20 40.						
рс сн	ARACTER	ISTICS <sup>(1)</sup>	Standard Opera Operating tempe	rature: -	anditions (unless) $40^{\circ}C \le TA \le +85^{\circ}$ $-40^{\circ}C \le TA \le +125^{\circ}$	s other C for In 5°C for	<b>wise stated)</b> dustrial Extended
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Comments
DA11	Rload	Resistive Output Load Impedance	ЗK		—	Ohm	
_	CLOAD	Output Load Capacitance	—	_	35	pF	Including output pin capacitance
DA12	Ιουτ	Output Current Drive Strength	200	300	—	μA	Sink and source
DA13	VRANGE	Output Drive Voltage Range at Current Drive of 200 mA	AVss + 250 mV	_	AVDD - 900 mV	V	
DA14	VLRANGE	Output Drive Voltage Range at Reduced Current Drive of 50 mA	AVss + 5 mV	_	AVDD – 500 mV	V	
DA15	IDD	Current Consumed when Module Is Enabled	_	—	1.3 x Iout	μA	Module will always con- sume this current even if no load is connected to the output
DA16	ROUTON	Output Impedance when Module is Enabled		820	_	Ohms	
DA30	VOFFSET	Input Offset Voltage	—	±10	10	mV	

# TABLE 25-43: DAC OUTPUT (DACOUT PIN) DC SPECIFICATIONS

**Note 1:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below VDDMIN. Refer to Parameter BO10 in Table 25-11 for BOR values.

#### TABLE 25-44: DAC GAIN STAGE TO COMPARATOR SPECIFICATIONS

DC CHAF	RACTERIS	TICS <sup>(1)</sup>		<b>Standa</b> (unless Operati	rd Opera otherwis ng tempe	ting Con se state rature: 	nditions d) $40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $40^{\circ}C \le TA \le +125^{\circ}C$ for Extended
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DA15	IDD	Current Consumed when Module Is Enabled.	_	60	_	μA	Module will always consume this current even if no load is connected to the output
DA32	G	Amplifier Gain	—	1.0	_	_	
			—	1.8		_	
DA33	GBWP	Gain Bandwidth Product	_	2.0		MHz	At 1 pF load capacitance. Measured with sine wave output signal of 1V peak-to-peak with a midpoint value of 1.2V. Voltage excursion from 0.7 to 1.7V.
DA34	SR	Slew Rate	—	5		V/µs	Slew rate between 10% and 90% of AVDD
DA07	Ts	Settling Time		200	_	ns	Settling time to 3%

**Note 1:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below VDDMIN. Refer to Parameter BO10 in Table 25-11 for BOR values.

# 26.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.



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