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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90352espmc-gs-180e1

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Part Number Parameter	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
16-bit Input capture	6 channels Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge) , signals an interrupt.			
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width×12 Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN interface	1 channel Compliant with CAN standard Version2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External interrupt	8 channels Can be used rising edge, falling edge, starting up by "H"/"L" level input, external interrupt, extended intelligent I/O services (EI ² OS) and DMA.			
D/A converter	—			
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F352E(S) and MB90F352TE(S) only)			
Corresponding evaluation name	MB90V340E-102		MB90V340E-101	

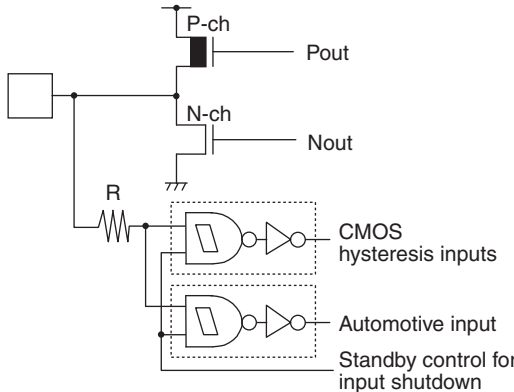
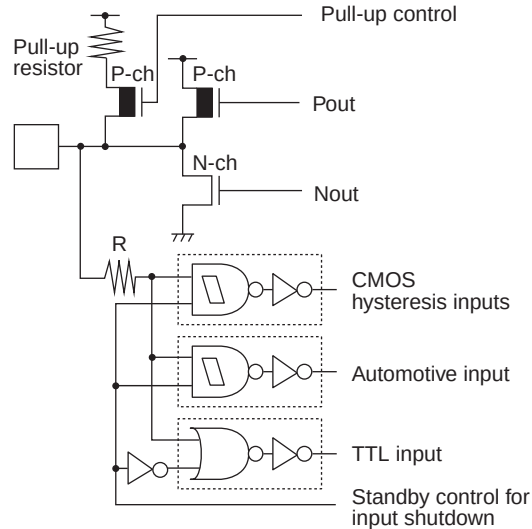
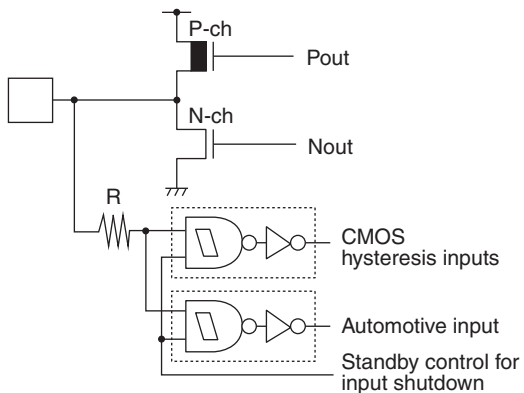
* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

3. Packages and Product Correspondence

Package	MB90V340E-101 MB90V340E-102 MB90V340E-103 MB90V340E-104	MB90351E (S) , MB90351TE (S) MB90F351E (S) , MB90F351TE (S) MB90352E (S) , MB90352TE (S) MB90F352E (S) , MB90F352TE (S) MB90356E (S) , MB90356TE (S) MB90F356E (S) , MB90F356TE (S) MB90357E (S) , MB90357TE (S) MB90F357E (S) , MB90F357TE (S)
PGA-299C-A01	○	×
FPT-64P-M23 (12.0 mm □ , 0.65 mm pitch)	×	○
FPT-64P-M24 (10.0 mm □ , 0.50 mm pitch)	×	○

○ : Yes, × : No

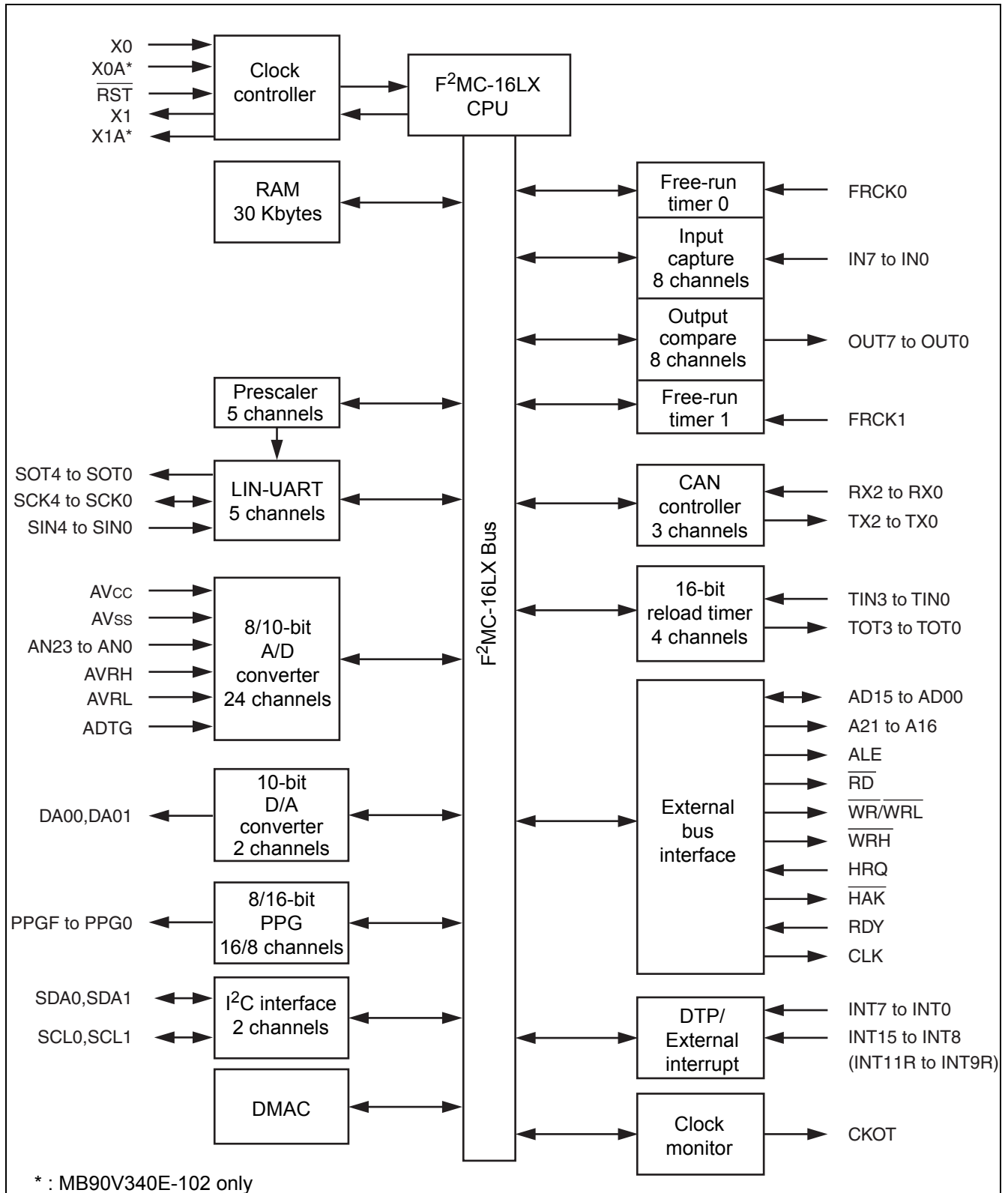
Note : Refer to "[Package Dimensions](#)" for detail of each package.

Type	Circuit	Remarks
F		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis inputs (With input shutdown function when is standby) ■ Automotive input (With the standby-time input shutdown function)
G		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ TTL input (With the standby-time input shutdown function) ■ Programmable pull-up resistor: approx. $50 \text{ k}\Omega$
H		■ CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function)

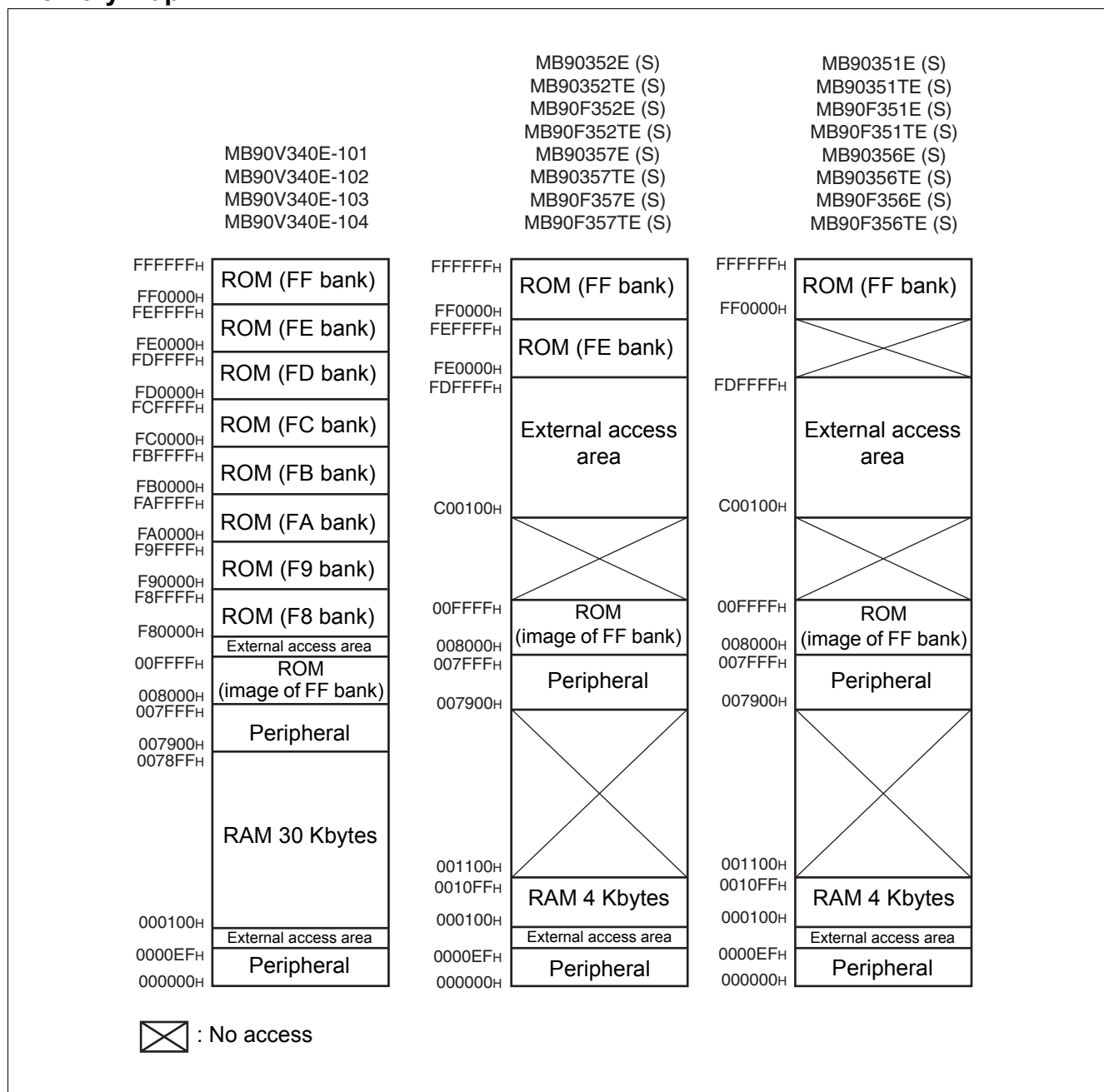
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8. Block Diagrams

■ MB90V340E-101/102



9. Memory Map



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.

For example, an attempt to access 00C00_H practically accesses the value at FFC00_H in ROM.

The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

The image between FF800_H and FFFFF_H is visible in bank 00, while the image between FF000_H and FF7FF_H is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
000058 _H to 00005B _H	Reserved				
00005C _H	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B
00005D _H	Output Compare Control Status Register 5	OCS5	R/W		0XX00000 _B
00005E _H	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
00005F _H	Output Compare Control Status Register 7	OCS7	R/W		0XX00000 _B
000060 _H	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 _B
000061 _H	Timer Control Status Register 0	TMCSR0	R/W		XXXX0000 _B
000062 _H	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 _B
000063 _H	Timer Control Status Register 1	TMCSR1	R/W		XXXX0000 _B
000064 _H	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000 _B
000065 _H	Timer Control Status Register 2	TMCSR2	R/W		XXXX0000 _B
000066 _H	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000 _B
000067 _H	Timer Control Status Register 3	TMCSR3	R/W		XXXX0000 _B
000068 _H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	000XXXX0 _B
000069 _H	A/D Control Status Register 1	ADCS1	R/W		0000000X _B
00006A _H	A/D Data Register 0	ADCR0	R		00000000 _B
00006B _H	A/D Data Register 1	ADCR1	R		XXXXXX00 _B
00006C _H	ADC Setting Register 0	ADSR0	R/W		00000000 _B
00006D _H	ADC Setting Register 1	ADSR1	R/W		00000000 _B
00006E _H	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low Voltage/CPU Operation Detection Reset	00111000 _B
00006F _H	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	XXXXXXXX1 _B
000070 _H to 00007F _H	Reserved				
000080 _H to 00008F _H	Reserved for CAN controller 1. Refer to "CAN Controllers"				
000090 _H to 00009A _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007950 _H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000 _B
007951 _H	Serial Control Register 3	SCR3	W, R/W		00000000 _B
007952 _H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000 _B
007953 _H	Serial Status Register 3	SSR3	R,R/W		00001000 _B
007954 _H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX _B
007955 _H	Extended Status Control Register 3	ESCR3	R/W		00000100 _B
007956 _H	Baud Rate Generator Register 30	BGR30	R/W		00000000 _B
007957 _H	Baud Rate Generator Register 31	BGR31	R/W		00000000 _B
007958 _H , 007959 _H	Reserved				
007960 _H	Clock supervisor Control Register	CSVCR	R, R/W	Clock Supervisor	00011100 _B
007961 _H to 00796D _H	Reserved				
00796E _H	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXX0 _B
00796F _H	Reserved				
007970 _H	I ² C Bus Status Register 0	IBSR0	R	I ² C Interface 0	00000000 _B
007971 _H	I ² C Bus Control Register 0	IBCR0	W,R/W		00000000 _B
007972 _H	I ² C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 _B
007973 _H		ITBAH0	R/W		00000000 _B
007974 _H	I ² C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 _B
007975 _H		ITMKH0	R/W		00111111 _B
007976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
007977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
007978 _H	I ² C data register 0	IDAR0	R/W	00000000 _B	
007979 _H , 00797A _H	Reserved				
00797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
00797C _H to 0079A1 _H	Reserved				
0079A2 _H	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000 _B
0079A3 _H	Flash Write Control Register 1	FWR1	R/W		00000000 _B
0079A4 _H	Sector Change Setting Register 0	SSR0	R/W		00XXXXX0 _B
0079A5 _H to 0079C1 _H	Reserved				
0079C2 _H	Clock modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 _B

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Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C80 _H to 007C87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
007C88 _H to 007C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
007C90 _H to 007C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
007C98 _H to 007C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
007CA0 _H to 007CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
007CA8 _H to 007CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
007CB0 _H to 007CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
007CB8 _H to 007CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
007CC0 _H to 007CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
007CC8 _H to 007CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
007CD0 _H to 007CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
007CD8 _H to 007CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
007CE0 _H to 007CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
007CE8 _H to 007CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B

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($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Sym- bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCLS}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During stopping clock supervisor, At sub sleep $T_A = +25^{\circ}\text{C}$	—	20	50	μA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep $T_A = +25^{\circ}\text{C}$	—	60	200	μA	MB90356E MB90F356E MB90357E MB90F357E
			$V_{CC} = 5.0\text{ V}$, Internal CR oscillation/ 4 division, At sub sleep $T_A = +25^{\circ}\text{C}$	—	60	200	μA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, At sub sleep $T_A = +25^{\circ}\text{C}$	—	70	150	μA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During operating clock supervisor, At sub sleep $T_A = +25^{\circ}\text{C}$	—	110	300	μA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			$V_{CC} = 5.0\text{ V}$, Internal CR oscillation/ 4 division, At sub sleep $T_A = +25^{\circ}\text{C}$	—	110	300	μA	MB90356TES MB90F356TES MB90357TES MB90F357TES

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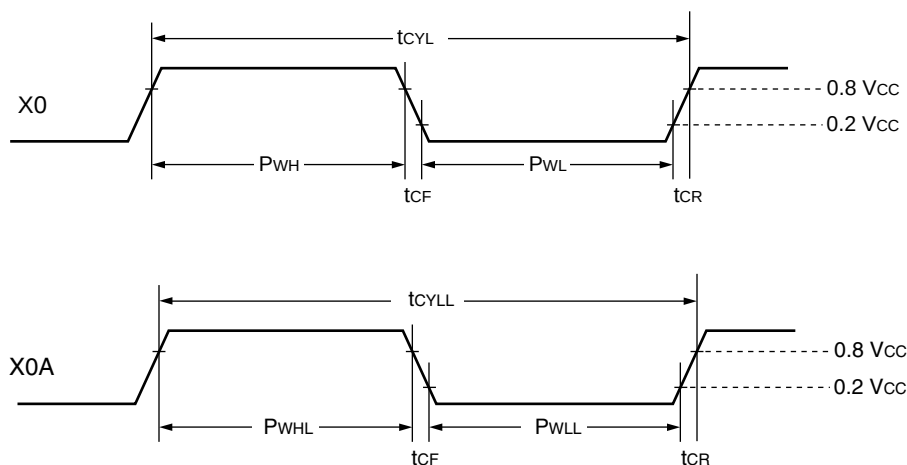
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($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

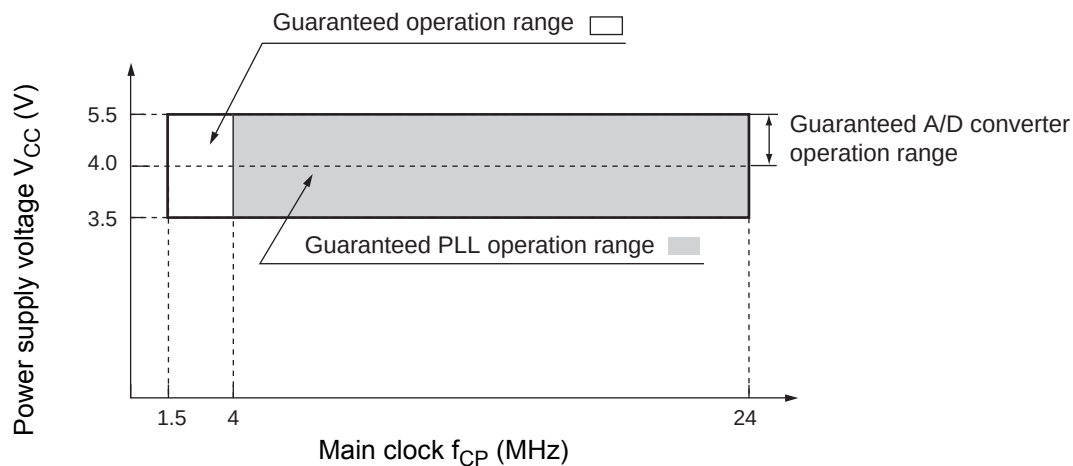
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	μs	When using sub clock

*: The limitation is in the range of the clock frequency when PLL is used. Use within the range in graph of “- PLL guaranteed operation range External clock frequency and internal operation clock frequency”.

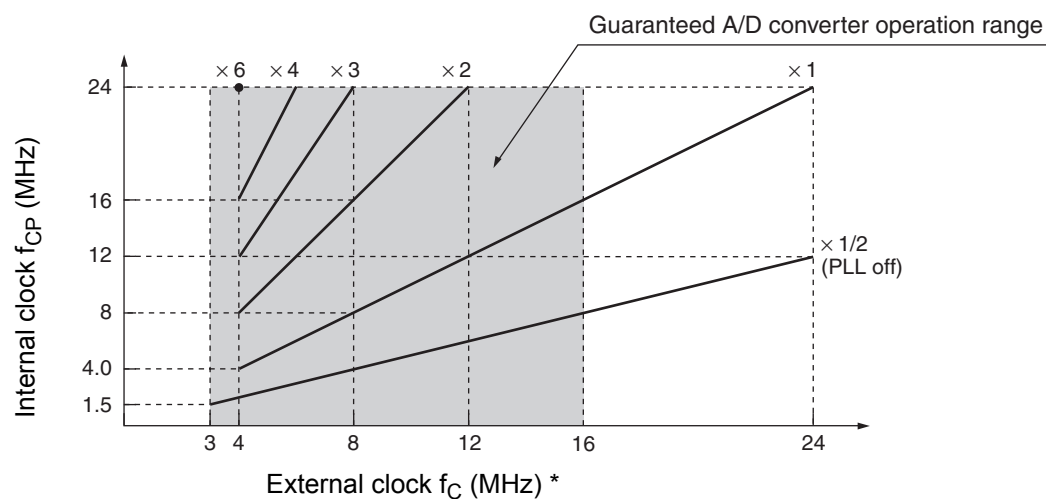
• Clock Timing



• PLL guaranteed operation range



Guaranteed operation range of MB90350E series



* : When using crystal oscillator or ceramic oscillator, the maximum clock frequency is 16 MHz.

External clock frequency and internal operation clock frequency

13.4.2 Reset Standby Input

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{\text{RST}}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 μs		μs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	μs	In Main timer mode and PLL timer mode

13.4.5 Bus Timing (Read)

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns
Valid address $\rightarrow$ ALE $\downarrow$ time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns
ALE $\downarrow \rightarrow$ Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns
Valid address $\rightarrow \overline{RD} \downarrow$ time	t_{AVRL}	A21 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns
Valid address $\rightarrow$ Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$(n^*+3/2) t_{CP} - 20$	—	ns
$\overline{RD} \downarrow \rightarrow$ Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$(n^*+3/2) t_{CP} - 50$	ns
$\overline{RD} \uparrow \rightarrow$ Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns
$\overline{RD} \uparrow \rightarrow$ ALE $\uparrow$ time	t_{RHLL}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns
$\overline{RD} \uparrow \rightarrow$ Address valid time	t_{RHAX}	$\overline{RD}$, A21 to A16		$t_{CP}/2 - 10$	—	ns
Valid address $\rightarrow$ CLK $\uparrow$ time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns
$\overline{RD} \downarrow \rightarrow$ CLK $\uparrow$ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	—	ns
ALE $\downarrow \rightarrow \overline{RD} \downarrow$ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns

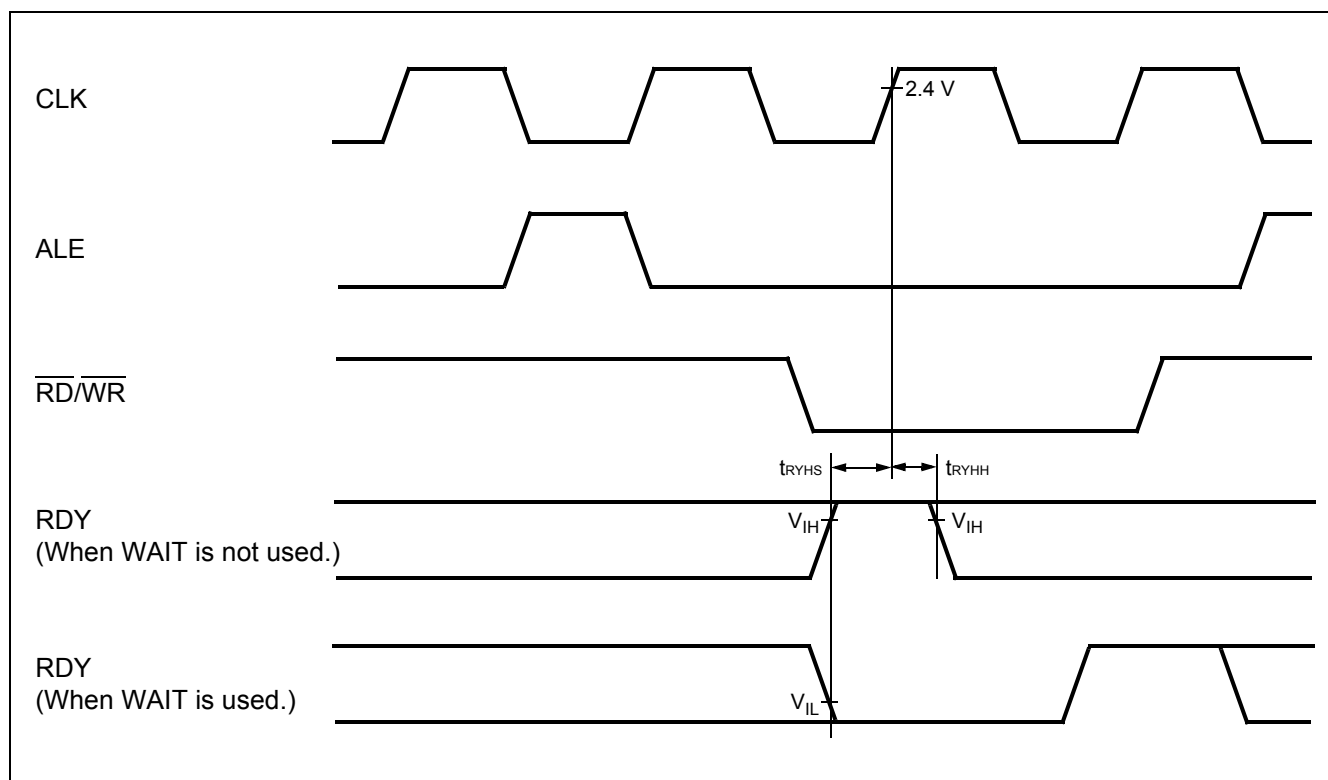
* : Number of ready cycles

13.4.7 Ready Input Timing

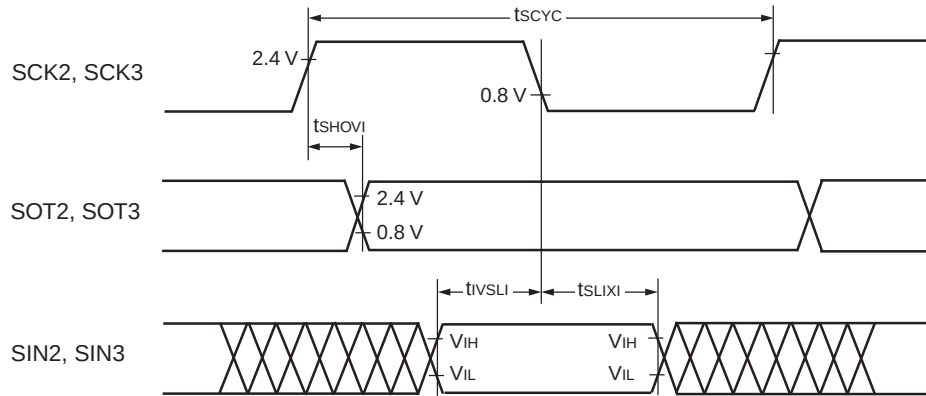
($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	45	—	ns	$f_{CP} = 16\text{ MHz}$
				32	—	ns	$f_{CP} = 24\text{ MHz}$
RDY hold time	t_{RYHH}	RDY		0	—	ns	

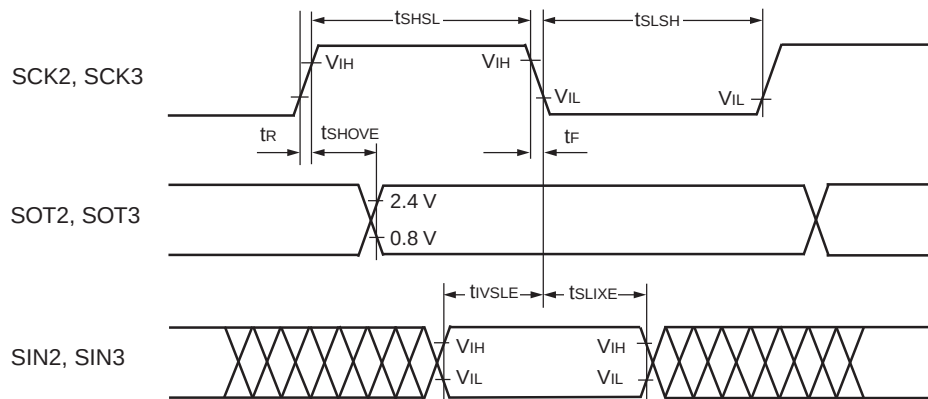
Note : If the RDY set-up time is insufficient, use the auto-ready function.



• Internal Shift Clock Mode



• External Shift Clock Mode



■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal clock operation output pins are $CL = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCK2, SCK3 SOT2, SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLI}	SCK2, SCK3 SIN2, SIN3		$t_{CP} + 80$	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	t_{SOVLI}	SCK2, SCK3 SOT2, SOT3		$3 t_{CP} - 70$	—	ns

Notes : • C_L is load capacity value of pins when testing.

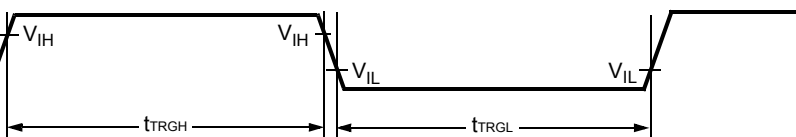
• t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

13.4.10 Trigger Input Timing

 $(T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, f_{CP} \leq 24\text{ MHz}, V_{SS} = AV_{SS} = 0\text{ V})$

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	$5 t_{CP}$	—	ns

INT8 to INT15,
INT9R to INT11R,
ADTG

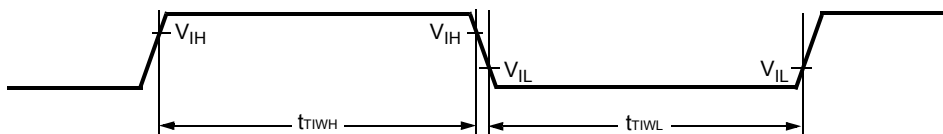


13.4.11 Timer Related Resource Input Timing

 $(T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, f_{CP} \leq 24\text{ MHz}, V_{SS} = AV_{SS} = 0\text{ V})$

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN1, TIN3, IN0, IN1, IN4 to IN7	—	$4 t_{CP}$	—	ns

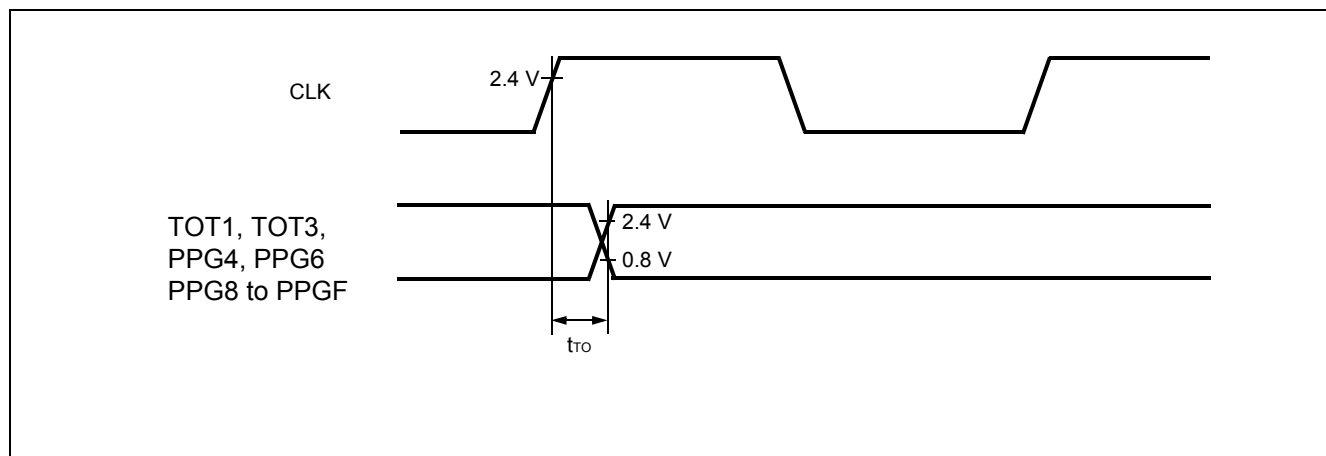
TIN1, TIN3,
IN0, IN1,
IN4 to IN7



13.4.12 Timer Related Resource Output Timing

 $(T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, f_{CP} \leq 24\text{ MHz}, V_{SS} = AV_{SS} = 0\text{ V})$

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK $\uparrow$ $\rightarrow$ T _{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns



13.4.13 I²C Timing

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	$R = 1.7\text{ k}\Omega$, $C = 50\text{ pF}^{*1}$	0	100	0	400	kHz
Hold time for (repeated) START condition SDA $\downarrow \rightarrow$ SCL $\downarrow$	t_{HDSTA}		4.0	—	0.6	—	μs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	μs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL $\uparrow \rightarrow$ SDA $\downarrow$	t_{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL $\downarrow \rightarrow$ SDA $\downarrow \uparrow$	t_{HDDAT}		0	3.45^{*2}	0	0.9^{*3}	μs
Data set-up time SDA $\downarrow \uparrow \rightarrow$ SCL $\uparrow$	t_{SUDAT}		250^{*5}	—	100^{*5}	—	ns
Set-up time for STOP condition SCL $\uparrow \rightarrow$ SDA $\uparrow$	t_{SUSTO}		4.0	—	0.6	—	μs
Bus free time between STOP condition and START condition	t_{BUS}		4.7	—	1.3	—	μs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} has to meet at least that the device does not exceed the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C -bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250\text{ ns}$ must be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

*5 : Refer to "• Note of SDA, SCL set-up time".

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Flash memory Data Retention Time	Average $T_A = +85^{\circ}\text{C}$	20	—	—	year	*

* : Corresponding value comes from the technology reliability evaluation result.

(Using Arrhenius equation to translate high temperature measurements test result into normalized value at +85°C)

14. Ordering Information

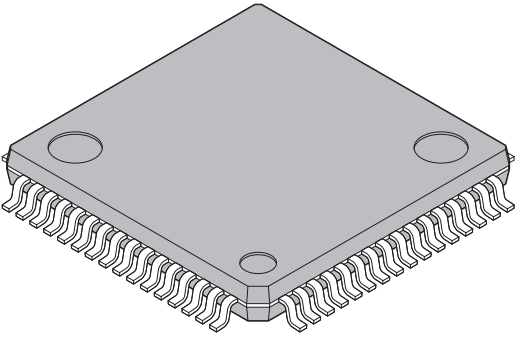
Part number	Package	Remarks
MB90F351EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC		
MB90F351TEPMC		
MB90F351TESPMC		
MB90F356EPMC		
MB90F356ESPMC		
MB90F356TEPMC		
MB90F356TESPMC		
MB90F352EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC		
MB90F352TEPMC		
MB90F352TESPMC		
MB90F357EPMC		
MB90F357ESPMC		
MB90F357TEPMC		
MB90F357TESPMC		
MB90351EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC		
MB90351TEPMC		
MB90351TESPMC		
MB90356EPMC		
MB90356ESPMC		
MB90356TEPMC		
MB90356TESPMC		
MB90352EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC		
MB90352TEPMC		
MB90352TESPMC		
MB90357EPMC		
MB90357ESPMC		
MB90357TEPMC		
MB90357TESPMC		

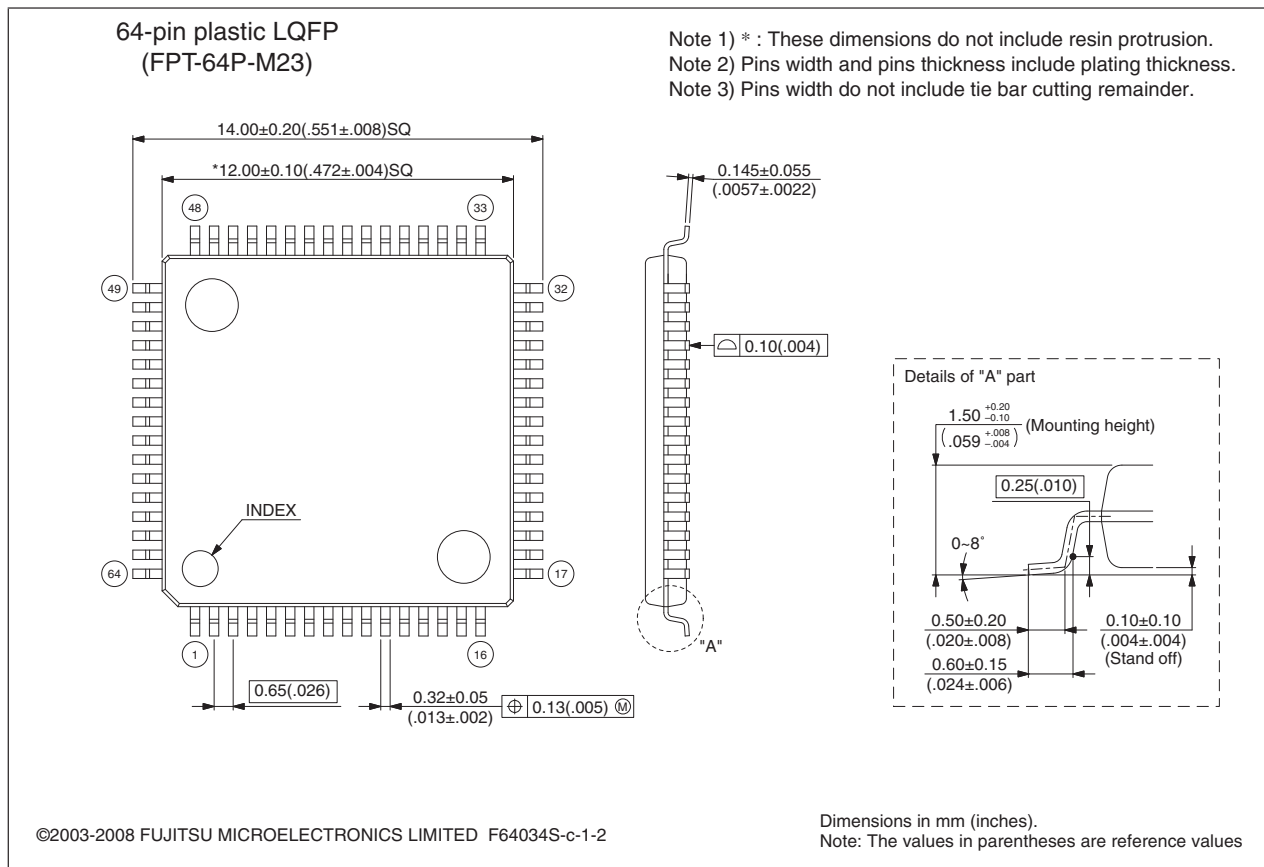
(Continued)

(Continued)

Part number	Package	Remarks
MB90F351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □ 0.50 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC1		
MB90F351TEPMC1		
MB90F351TESPMC1		
MB90F356EPMC1		
MB90F356ESPMC1		
MB90F356TEPMC1		
MB90F356TESPMC1		
MB90F352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □ 0.50 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC1		
MB90F352TEPMC1		
MB90F352TESPMC1		
MB90F357EPMC1		
MB90F357ESPMC1		
MB90F357TEPMC1		
MB90F357TESPMC1		
MB90351EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □ 0.50 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC1		
MB90351TEPMC1		
MB90351TESPMC1		
MB90356EPMC1		
MB90356ESPMC1		
MB90356TEPMC1		
MB90356TESPMC1		
MB90352EPMC1	64-pin plastic LQFP FPT-64P-M24 10.0 mm □ 0.50 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC1		
MB90352TEPMC1		
MB90352TESPMC1		
MB90357EPMC1		
MB90357ESPMC1		
MB90357TEPMC1		
MB90357TESPMC1		
MB90V340E-101CR	299-pin ceramic PGA PGA-299C-A01	Device for evaluation
MB90V340E-102CR		
MB90V340E-103CR		
MB90V340E-104CR		

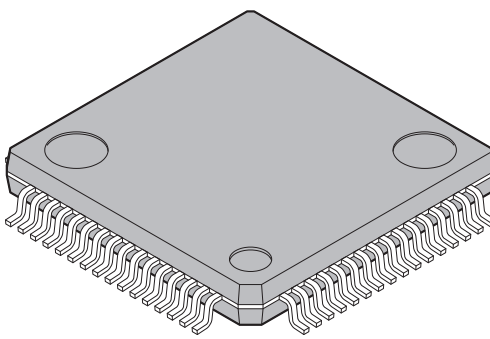
14.1 Package Dimensions

64-pin plastic LQFP  (FPT-64P-M23)	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65



(Continued)

(Continued)

64-pin plastic LQFP  (FPT-64P-M24)	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP64-10×10-0.50

