Infineon Technologies - MB90352ESPMC-GS-191E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90352espmc-gs-191e1

- 8/16-bit PPG timer : 8-bit ∞ 10 channels or 16-bit × 6 channels
- 16-bit reload timer : 2 channels (only Evaluation products has 4 channels)
- 16- bit input/output timer
  - 16-bit free-run timer : 2 channels (FRT0 : ICU0/1, FRT1 : ICU4/5/6/7, OCU4/5/6/7)
  - 16- bit input capture: (ICU) : 6 channels
  - 16-bit output compare : (OCU) : 4 channels

FULL-CAN interface: 1 channel

- Compliant with CAN standard Version2.0 Part A and Part B
- 16 message buffers are built-in
- CAN wake-up function

LIN-UART: 2 channels

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

I^2C interface: 1 channel

Up to 400 kbps transfer rate

DTP/External interrupt: 8 channels, CAN wakeup: 1 channel

Module for activation of extended intelligent I/O service (EI^2OS), DMA, and generation of external interrupt by external input.

Delay interrupt generator module

Generates interrupt request for task switching.

8/10-bit A/D converter: 15 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3 µs (at 24 MHz machine clock, including sampling time)

Address matching detection (Program patch) function

- Address matching detection for 6 address pointers.

Capable of changing input voltage level for port

- Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)
- TTL level (corresponds to external bus pins only, initial level of these pins is TTL in external bus mode)

Low voltage/CPU operation detection reset (devices with T-suffix)

- Detects low voltage (4.0 V ± 0.3 V) and resets automatically
- Resets automatically when program is runaway and counter is not cleared within interval time
  (approx. 262 ms : external 4 MHz)

Dual operation Flash memory (only devices 128 Kbytes Flash memory)

- Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.

Supported T_A = + 125°C

The maximum operating frequency is 24 MHz* : (at T_A = +125°C) .

Flash security function

- Protects the content of Flash memory
  (MB90F352x, MB90F357x only)

External bus interface

- 4 Mbytes external memory space
  MB90F351E(S), MB90F351TE(S), MB90F352E(S), MB90F352TE(S) : External bus Interface can not be used in internal vector mode. It can be used only in external vector mode.

* : If used exceeding T_A = + 105 °C, be sure to contact Cypress for reliability limitations.

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Part Number / Parameter	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-101	MB90V340E-102
16-bit output compare	4 channels				8 channels	
	Signals an interrupt when 16-bit free-run Timer matches output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit input capture	6 channels				8 channels	
	Retains 16-bit free-run timer value by (rising edge, falling edge, or the both edges), signals an interrupt.					
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width×12 8-bit reload registers for H pulse width×12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN interface	1 channel				3 channels	
	Compliant with CAN standard Version 2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by “H”/“L” level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—				2 channels	
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash memory	—					
Corresponding evaluation name	MB90V340E-102		MB90V340E-101		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ MASK ROM products/Evaluation products

Parameter \ Part Number	MB90356E MB90357E	MB90356TE MB90357TE	MB90356ES MB90357ES	MB90356TES MB90357TES	MB90V340E-103	MB90V340E-104
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64 Kbytes :MB90356E(S), MB90356TE(S) 128 Kbytes :MB90357E(S), MB90357TE(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes		No		No	Yes
Clock supervisor	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40°C to +125°C				—	
Package	LQFP-64				PGA-299	
LIN-UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 kbps)	1 channel				2 channels	
A/D converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit reload timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				Free-run Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. Free-run Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

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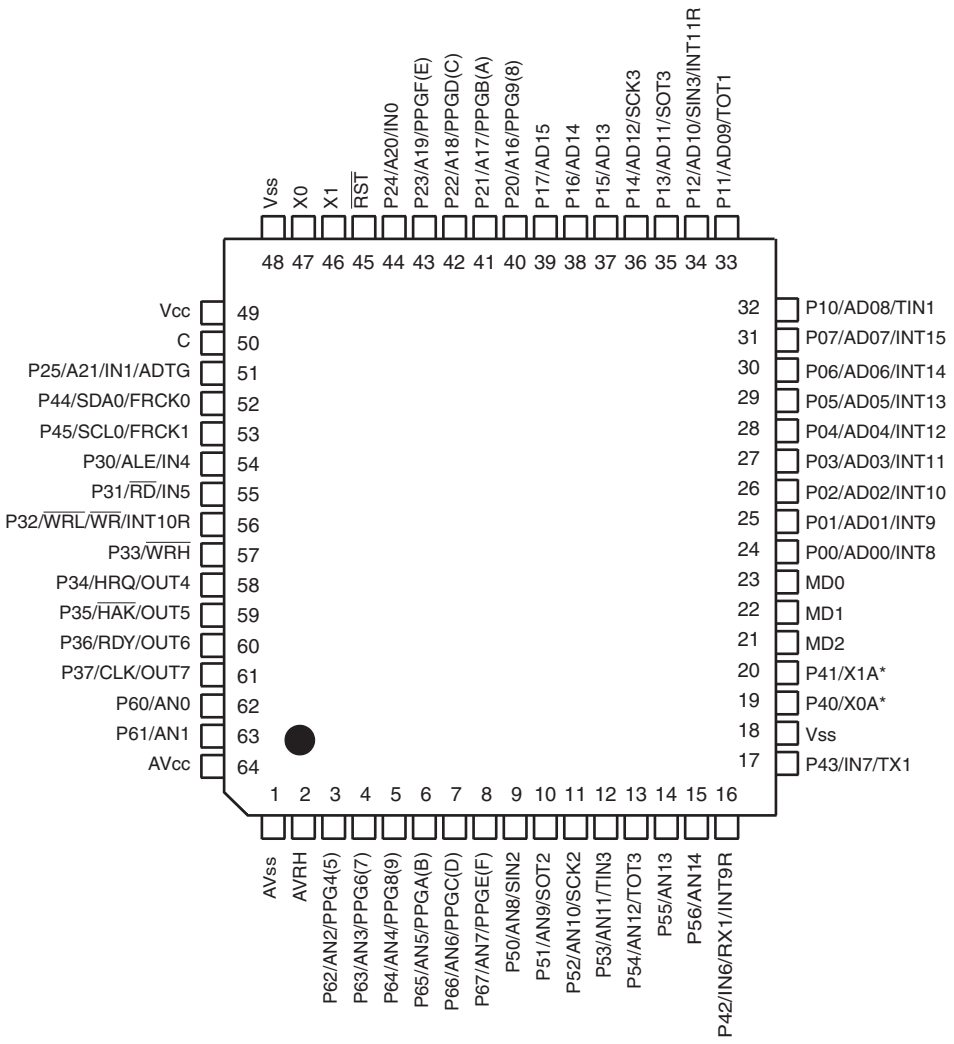
4. Pin Assignments

■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S) , MB90F352TE (S) , MB90356E (S) , MB90356TE (S) , MB90F356E (S) , MB90F356TE (S) , MB90357E (S) , MB90357TE (S) , MB90F357E (S) , MB90F357TE (S)

(TOP VIEW)



(FPT-64P-M23, FPT-64P-M24)

* : Devices without S-suffix : X0A, X1A
Devices with S-suffix : P40, P41

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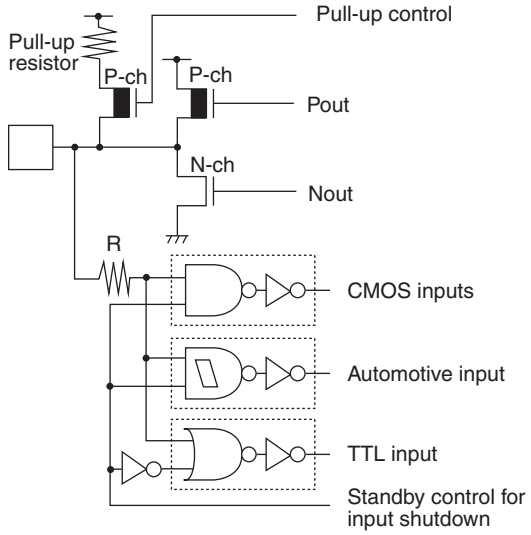
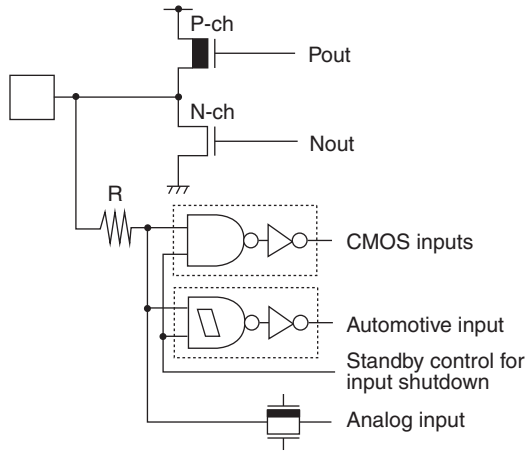
Type	Circuit	Remarks
N		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ TTL input (With the standby-time input shutdown function) ■ Programmable pull-up resistor: approx. 50 kΩ
O		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ Analog input for A/D converter

7. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions :

■A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.

■A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.

■The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage (V_{CC}) .

2. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused I/O pins should be set to the output state and can be left open, or the input state with the above described connection.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

9. Turning-on sequence of power supply to A/D converter and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}) .Turn-off the digital power after turning off the A/D converter power
supply and analog inputs. In this case, make sure that the power supply voltage does not exceed the rated voltage of the A/D converter (turning on/of the analog and digital power supplies simultaneously is acceptable).

10. Connection of unused pins of A/D converter if A/D converter is not used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

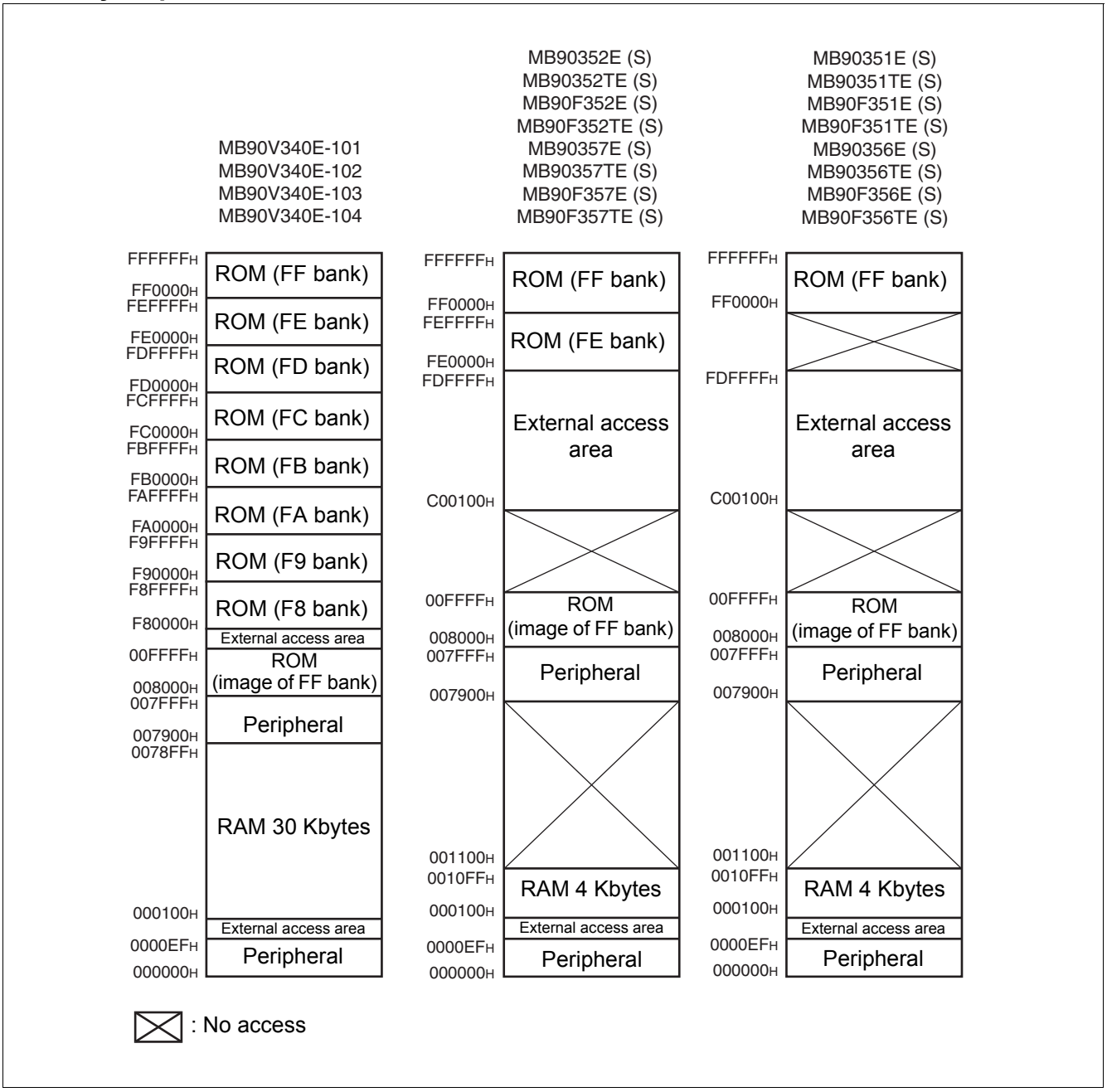
11. Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at
50 µs or more (0.2 V to 2.7 V) .

12. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/
60 MHz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

9. Memory Map



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access $00C000_H$ practically accesses the value at $FFC000_H$ in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
000038_H	PPG 4 Operation Mode Control Register	PPGC4	W, R/W	16-bit Programmable Pulse Generator 4/5	$0X000XX1_B$
000039_H	PPG 5 Operation Mode Control Register	PPGC5	W, R/W		$0X000001_B$
$00003A_H$	PPG 4/5 Count Clock Select Register	PPG45	R/W		$000000X0_B$
$00003B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000_B
$00003C_H$	PPG 6 Operation Mode Control Register	PPGC6	W, R/W	16-bit Programmable Pulse Generator 6/7	$0X000XX1_B$
$00003D_H$	PPG 7 Operation Mode Control Register	PPGC7	W, R/W		$0X000001_B$
$00003E_H$	PPG 6/7 Count Clock Select Register	PPG67	R/W		$000000X0_B$
$00003F_H$	Reserved				
000040_H	PPG 8 Operation Mode Control Register	PPGC8	W, R/W	16-bit Programmable Pulse Generator 8/9	$0X000XX1_B$
000041_H	PPG 9 Operation Mode Control Register	PPGC9	W, R/W		$0X000001_B$
000042_H	PPG 8/9 Count Clock Select Register	PPG89	R/W		$000000X0_B$
000043_H	Reserved				
000044_H	PPG A Operation Mode Control Register	PPGCA	W, R/W	16-bit Programmable Pulse Generator A/B	$0X000XX1_B$
000045_H	PPG B Operation Mode Control Register	PPGCB	W, R/W		$0X000001_B$
000046_H	PPG A/B Count Clock Select Register	PPGAB	R/W		$000000X0_B$
000047_H	Reserved				
000048_H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit Programmable Pulse Generator C/D	$0X000XX1_B$
000049_H	PPG D Operation Mode Control Register	PPGCD	W,R/W		$0X000001_B$
$00004A_H$	PPG C/D Count Clock Select Register	PPGCD	R/W		$000000X0_B$
$00004B_H$	Reserved				
$00004C_H$	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit Programmable Pulse Generator E/F	$0X000XX1_B$
$00004D_H$	PPG F Operation Mode Control Register	PPGCF	W,R/W		$0X000001_B$
$00004E_H$	PPG E/F Count Clock Select Register	PPGEF	R/W		$000000X0_B$
$00004F_H$	Reserved				
000050_H	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	00000000_B
000051_H	Input Capture Edge Register 0/1	ICE01	R/W, R		$XXX0X0XX_B$
000052_H, 000053_H	Reserved				
000054_H	Input Capture Control Status Register 4/5	ICS45	R/W	Input Capture 4/5	00000000_B
000055_H	Input Capture Edge Register 4/5	ICE45	R		$XXXXXXXX_B$
000056_H	Input Capture Control Status Register 6/7	ICS67	R/W	Input Capture 6/7	00000000_B
000057_H	Input Capture Edge Register 6/7	ICE67	R/W, R		$XXX000XX_B$

(Continued)

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Address CAN1	Register	Abbreviation	Access	Initial Value
$007D00_H$	Control status register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007D01_H$				
$007D02_H$	Last event indicator register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007D03_H$				
$007D04_H$	Receive/transmit error counter	RTEC	R	00000000_B 00000000_B
$007D05_H$				
$007D06_H$	Bit timing register	BTR	R/W	11111111_B $X1111111_B$
$007D07_H$				
$007D08_H$	IDE register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D09_H$				
$007D0A_H$	Transmit RTR register	TRTRR	R/W	00000000_B 00000000_B
$007D0B_H$				
$007D0C_H$	Remote frame receive waiting register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D0D_H$				
$007D0E_H$	Transmit interrupt enable register	TIER	R/W	00000000_B 00000000_B
$007D0F_H$				
$007D10_H$	Acceptance mask select register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D11_H$				
$007D12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D13_H$				
$007D14_H$	Acceptance mask register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D15_H$				
$007D16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D17_H$				
$007D18_H$	Acceptance mask register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007D19_H$				
$007D1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007D1B_H$				

List of Message Buffers (ID Registers)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C00_H$ to $007C1F_H$	General-purpose RAM	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C20_H$	ID register 0	IDR0	R/W	$XXXXXXXX_B$
$007C21_H$				$XXXXXXXX_B$
$007C22_H$				$XXXXXXXX_B$
$007C23_H$				$XXXXXXXX_B$
$007C24_H$	ID register 1	IDR1	R/W	$XXXXXXXX_B$
$007C25_H$				$XXXXXXXX_B$
$007C26_H$				$XXXXXXXX_B$
$007C27_H$				$XXXXXXXX_B$
$007C28_H$	ID register 2	IDR2	R/W	$XXXXXXXX_B$
$007C29_H$				$XXXXXXXX_B$
$007C2A_H$				$XXXXXXXX_B$
$007C2B_H$				$XXXXXXXX_B$
$007C2C_H$	ID register 3	IDR3	R/W	$XXXXXXXX_B$
$007C2D_H$				$XXXXXXXX_B$
$007C2E_H$				$XXXXXXXX_B$
$007C2F_H$				$XXXXXXXX_B$
$007C30_H$	ID register 4	IDR4	R/W	$XXXXXXXX_B$
$007C31_H$				$XXXXXXXX_B$
$007C32_H$				$XXXXXXXX_B$
$007C33_H$				$XXXXXXXX_B$
$007C34_H$	ID register 5	IDR5	R/W	$XXXXXXXX_B$
$007C35_H$				$XXXXXXXX_B$
$007C36_H$				$XXXXXXXX_B$
$007C37_H$				$XXXXXXXX_B$
$007C38_H$	ID register 6	IDR6	R/W	$XXXXXXXX_B$
$007C39_H$				$XXXXXXXX_B$
$007C3A_H$				$XXXXXXXX_B$
$007C3B_H$				$XXXXXXXX_B$
$007C3C_H$	ID register 7	IDR7	R/W	$XXXXXXXX_B$
$007C3D_H$				$XXXXXXXX_B$
$007C3E_H$				$XXXXXXXX_B$
$007C3F_H$				$XXXXXXXX_B$

(Continued)

Address CAN1	Register	Abbreviation	Access	Initial Value
$007C80_H$ to $007C87_H$	Data register 0 (8 bytes)	DTR0	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C88_H$ to $007C8F_H$	Data register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C90_H$ to $007C97_H$	Data register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007C98_H$ to $007C9F_H$	Data register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CA0_H$ to $007CA7_H$	Data register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CA8_H$ to $007CAF_H$	Data register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CB0_H$ to $007CB7_H$	Data register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CB8_H$ to $007CBF_H$	Data register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CC0_H$ to $007CC7_H$	Data register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CC8_H$ to $007CCF_H$	Data register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CD0_H$ to $007CD7_H$	Data register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CD8_H$ to $007CDF_H$	Data register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CE0_H$ to $007CE7_H$	Data register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007CE8_H$ to $007CEF_H$	Data register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

(Continued)

12. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS corresponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
Reserved	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
Reserved	N	—	#12	FFFFCC$_H$		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4$_H$		
I^{2}C	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Reserved	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG 4/5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 6/7	N	—	#22	FFFFA4$_H$		
PPG 8/9/C/D	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	—	#24	FFFF9C$_H$		
Timebase Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
Free-run Timer 0 / free-run Timer 1	N	—	#30	FFFF84$_H$		
Input Capture 4/5	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0/1	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 6/7	Y1	9	#34	FFFF74$_H$		
Reserved	N	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
Reserved	N	11	#36	FFFF6C$_H$		
UART 3 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 3 TX	Y1	13	#38	FFFF64$_H$		

(Continued)

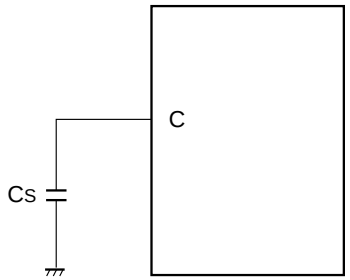
13.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	−40	—	+125	°C	*

* : If used exceeding T_A = +105°C, be sure to contact Cypress for reliability limitations.

″ C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(T_A = −40°C to +125°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output “L” voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output “L” voltage	V_{OLI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	− 1	—	+ 1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P25, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory devices
Power supply current	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	48	60	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At writing Flash memory.	—	53	65	mA	Flash memory devices
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At erasing Flash memory.	—	58	70	mA	Flash memory devices
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	25	35	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, At Main Timer mode	—	0.3	0.8	mA	Devices without “T”-suffix
				—	0.4	1.0	mA	Devices with “T”-suffix
	I_{CTSPLL} [6]		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	

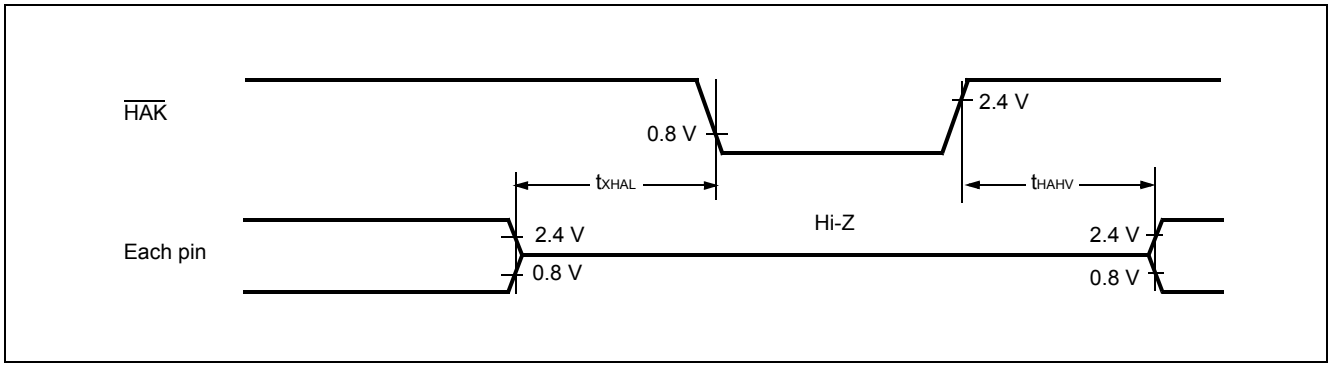
(Continued)

13.4.8 Hold Timing

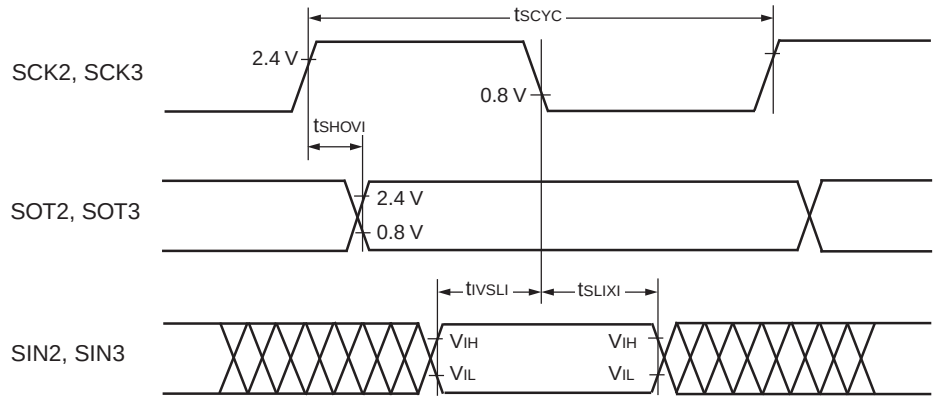
(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units
				Min	Max	
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	–	30	t_{CP}	ns
$\overline{HAK}$ ↑ time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns

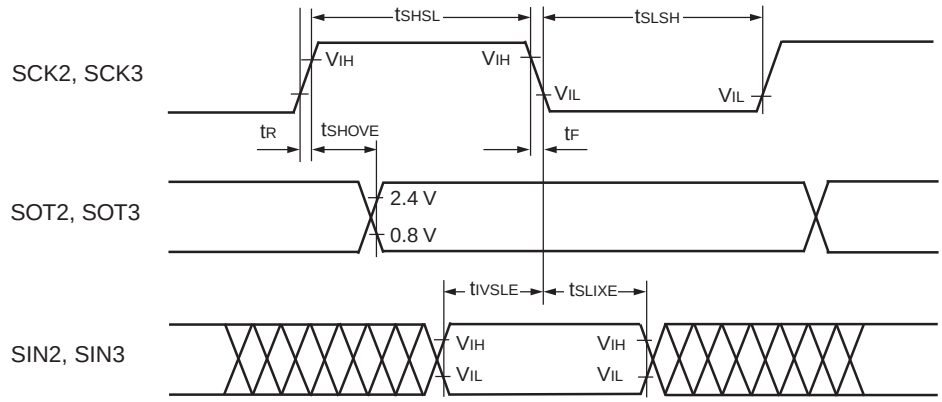
Note : There is more than 1 machine cycle from when HRQ pin reads in until the $\overline{HAK}$ is changed.



• Internal Shift Clock Mode



• External Shift Clock Mode



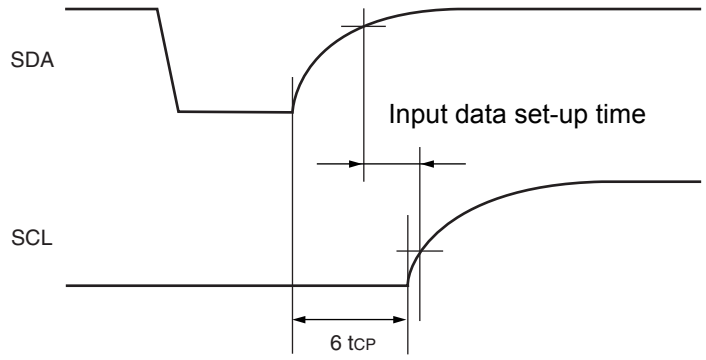
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal clock operation output pins are CL = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2, SCK3 SOT2, SOT3		–50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK2, SCK3 SIN2, SIN3		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2, SCK3 SOT2, SOT3		3 t_{CP} – 70	—	ns

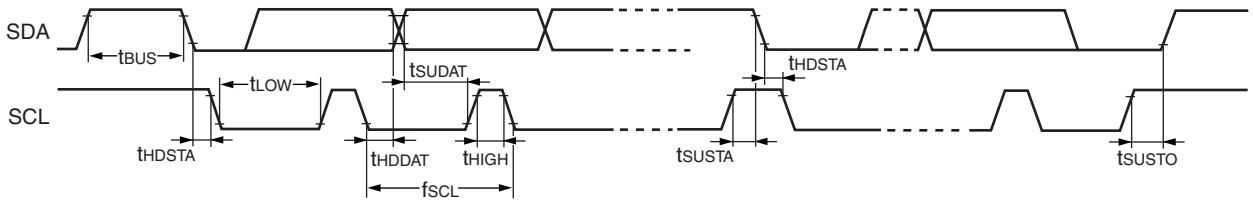
Notes : • C_L is load capacity value of pins when testing.
• t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

• Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition



13.5 A/D Converter

(T_A = −40°C to +125°C, 3.0 V ≤ AVRH, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	AV_{SS} − 1.5×LSB	AV_{SS} + 0.5×LSB	AV_{SS} + 2.5×LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN14	AVRH − 3.5×LSB	AVRH − 1.5×LSB	AVRH + 0.5×LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0				4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	×	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2				4.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN14	− 0.3	—	+ 0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AV_{SS}	—	AVRH	V	
Reference voltage range	—	AVRH	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between channels	—	AN0 to AN14	—	—	4	LSB	

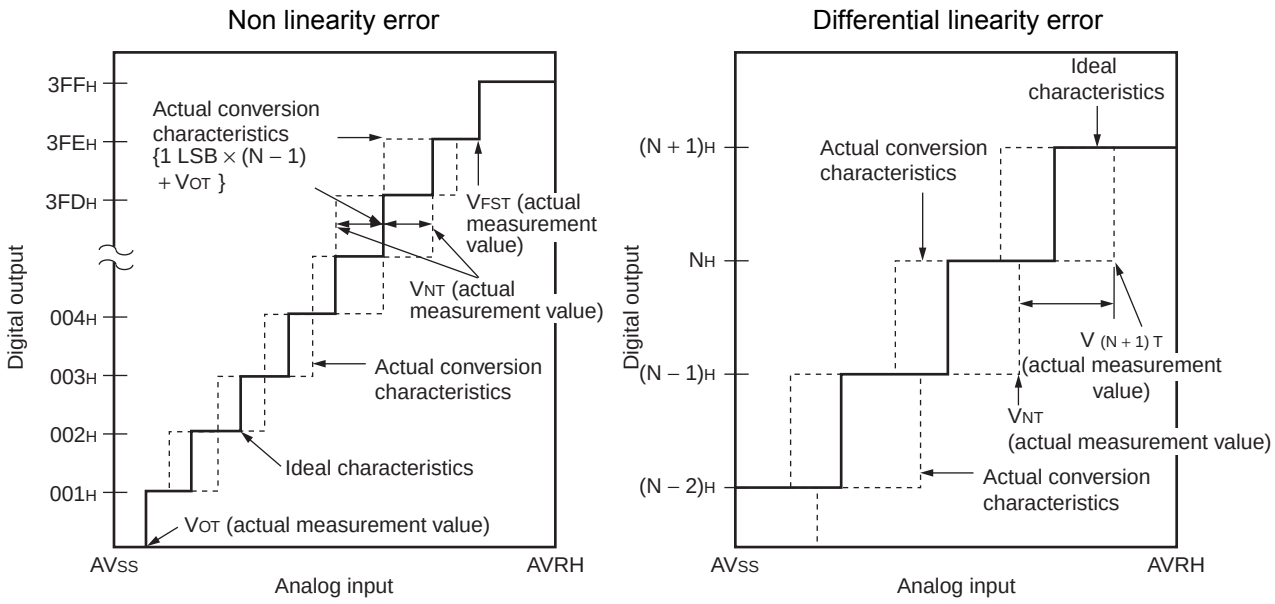
* : If A/D converter is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Notes on A/D Converter Section

■ About the external impedance of the analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting
A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H".
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$".

13.7 Flash Memory Program/Erase Characteristics

■ Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25°C V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10000	—	—	cycle	

15. Major Changes

Page	Section	Change Results
—	—	The following names are changed. UART → LIN-UART 16-bit I/O timer → 16-bit free-run timer
26	Handling Devices	Added the section ”13. Serial Communication”.
51	Electrical Characteristics Absolute Maximum Ratings	Changed the maximum value of power consumption.
63	Electrical Characteristics AC Characteristics	Changed the "(4) Clock Output Timing". Changed the Minimum value of cycle time. (41.76 → 41.67)
69 to 73		Changed the notation of “(9) LIN-UART”.
78	A/D Converter	Changed the notation of “Zero reading voltage” and “full scale reading voltage”.
85	Ordering Information	Changed the part number; MB90V340E-101 → MB90V340E-101CR MB90V340E-102 → MB90V340E-102CR MB90V340E-103 → MB90V340E-103CR MB90V340E-104 → MB90V340E-104CR

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90350E Series F^{2}MC-16LX 16-bit Microcontrollers Document Number: 002-04493				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	10/12/2006	Migrated to Cypress and assigned document number 002-04993. No change to document contents or format.
*A	5193077	AKIH	04/07/2016	Updated to Cypress template