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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90352espmc-gs-198e1

- 8/16-bit PPG timer : 8-bit ∞ 10 channels or 16-bit \times 6 channels
- 16-bit reload timer : 2 channels (only Evaluation products has 4 channels)
- 16-bit input/output timer
 - 16-bit free-run timer : 2 channels (FRT0 : ICU0/1, FRT1 : ICU4/5/6/7, OCU4/5/6/7)
 - 16-bit input capture: (ICU) : 6 channels
 - 16-bit output compare : (OCU) : 4 channels

FULL-CAN interface: 1 channel

- Compliant with CAN standard Version2.0 Part A and Part B
- 16 message buffers are built-in
- CAN wake-up function

LIN-UART: 2 channels

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

I²C interface: 1 channel

Up to 400 kbps transfer rate

DTP/External interrupt: 8 channels, CAN wakeup: 1 channel

Module for activation of extended intelligent I/O service (EI²OS), DMA, and generation of external interrupt by external input.

Delay interrupt generator module

Generates interrupt request for task switching.

8/10-bit A/D converter: 15 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3 μ s (at 24 MHz machine clock, including sampling time)

Address matching detection (Program patch) function

- Address matching detection for 6 address pointers.

Capable of changing input voltage level for port

- Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)
- TTL level (corresponds to external bus pins only, initial level of these pins is TTL in external bus mode)

Low voltage/CPU operation detection reset (devices with T-suffix)

- Detects low voltage (4.0 V \pm 0.3 V) and resets automatically
- Resets automatically when program is runaway and counter is not cleared within interval time (approx. 262 ms : external 4 MHz)

Dual operation Flash memory (only devices 128 Kbytes Flash memory)

- Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.

Supported T_A = + 125°C

The maximum operating frequency is 24 MHz* : (at T_A = +125°C) .

Flash security function

- Protects the content of Flash memory (MB90F352x, MB90F357x only)

External bus interface

- 4 Mbytes external memory space
MB90F351E(S), MB90F351TE(S), MB90F352E(S), MB90F352TE(S) : External bus Interface can not be used in internal vector mode. It can be used only in external vector mode.

* : If used exceeding T_A = + 105 °C, be sure to contact Cypress for reliability limitations.

(Continued)

Part Number Parameter	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
16-bit Input capture	6 channels Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge) , signals an interrupt.			
8/16-bit programmable pulse generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width×12 Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN interface	1 channel Compliant with CAN standard Version2.0 Part A and Part B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame 16 prioritized message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External interrupt	8 channels Can be used rising edge, falling edge, starting up by "H"/"L" level input, external interrupt, extended intelligent I/O services (EI ² OS) and DMA.			
D/A converter	—			
I/O ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F352E(S) and MB90F352TE(S) only)			
Corresponding evaluation name	MB90V340E-102		MB90V340E-101	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

■ MASK ROM products/Evaluation products

<div>Part Number</div> <div>Parameter</div>	MB90351E MB90352E	MB90351TE MB90352TE	MB90351ES MB90352ES	MB90351TES MB90352TES	MB90V340E-1 01	MB90V340E-1 02
Type	MASK ROM products				Evaluation products	
CPU	F ² MC-16LX CPU					
System clock	PLL clock multiplication circuit (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64 Kbytes : MB90351E(S), MB90351TE(S) 128 Kbytes : MB90352E(S), MB90352TE(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No		No	Yes
Clock supervisor	No					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40°C to +125°C				—	
Package	LQFP-64				PGA-299	
LIN-UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
	1 channel				2 channels	
A/D converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit reload timer	2 channels				4 channels	
	Operation clock frequency : fsys/2 ¹ , fsys/2 ³ , fsys/2 ⁵ (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.				Free-run Timer 0 corresponds to ICU0/1/2/3, OCU0/1/2/3. Free-run Timer 1 corresponds to ICU4/5/6/7, OCU4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ , fsys/2 ⁵ , fsys/2 ⁶ , fsys/2 ⁷ (fsys = Machine clock frequency)					

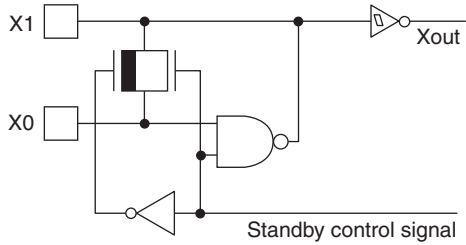
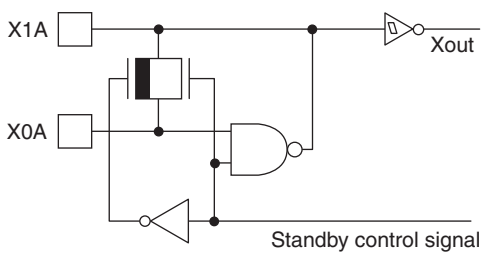
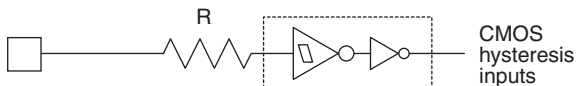
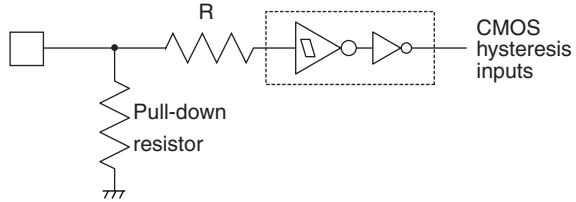
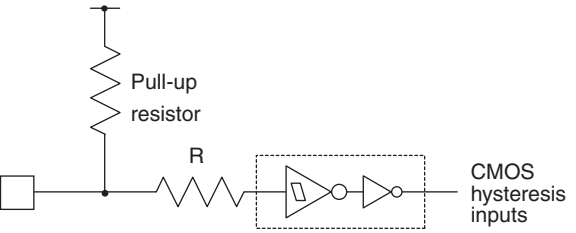
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■ MASK ROM products/Evaluation products

<div>Part Number</div> <div>Parameter</div>	MB90356E MB90357E	MB90356TE MB90357TE	MB90356ES MB90357ES	MB90356TES MB90357TES	MB90V340E-1 03	MB90V340E-1 04
CPU	F ² MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64 Kbytes :MB90356E(S), MB90356TE(S) 128 Kbytes :MB90357E(S), MB90357TE(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes		No		No	Yes
Clock supervisor	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40°C to +125°C				—	
Package	LQFP-64				PGA-299	
LIN-UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
	1 channel				2 channels	
A/D converter	15 channels				24 channels	
16-bit reload timer (4 channels)	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit free-run timer (2 channels)	Operation clock frequency : fsys/2 ¹ , fsys/2 ³ , fsys/2 ⁵ (fsys = Machine clock frequency) Supports External Event Count function.				Free-run Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. Free-run Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.					
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ , fsys/2 ⁵ , fsys/2 ⁶ , fsys/2 ⁷ (fsys = Machine clock frequency)					

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6. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 M Ω
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 M Ω
C		■ MASK ROM device CMOS hysteresis input pin ■ Flash memory device CMOS input pin
D		■ MASK ROM device CMOS hysteresis input pin Pull-down resistor value: approx. 50 k Ω ■ Flash memory device CMOS input pin No Pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 k Ω

(Continued)

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

9. Turning-on sequence of power supply to A/D converter and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , $AVRH$) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}). Turn-off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the power supply voltage does not exceed the rated voltage of the A/D converter (turning on/of the analog and digital power supplies simultaneously is acceptable).

10. Connection of unused pins of A/D converter if A/D converter is not used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

11. Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μ s or more (0.2 V to 2.7 V).

12. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/ 60 MHz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

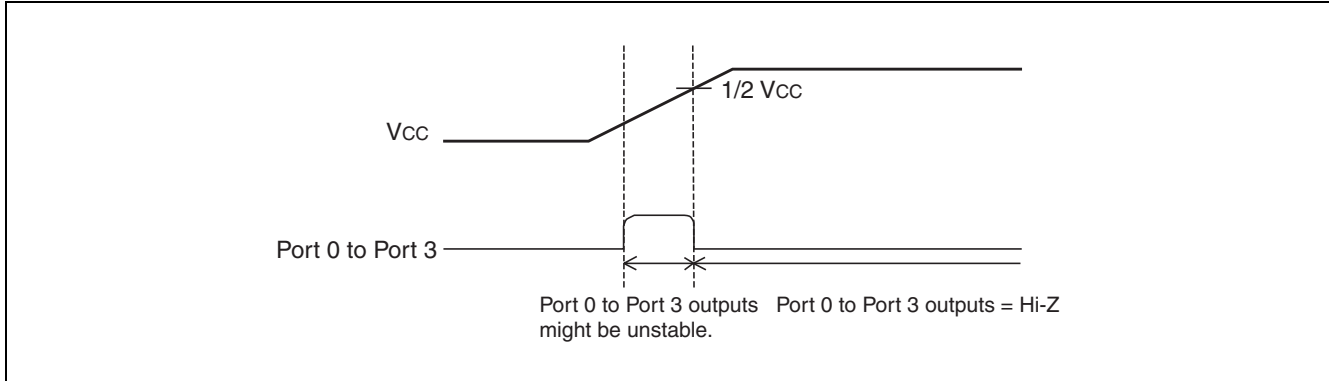
13. Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

14. Port 0 to port 3 output during power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable regardless of reset inputs.



15. Setting using CAN function

To use CAN function, please set "1" to DIRECT bit of CAN direct mode register (CDMR).

16. Flash security function

The security byte is located in the area of the Flash memory. If protection code 01_H is written in the security byte, the Flash memory is in the protected state by security.

Therefore please do not write 01_H in this address if you do not use the security function.

Please refer to following table for the address of the security byte.

Product name	Flash memory size	Address for security bit
MB90F352E(S) MB90F352TE(S) MB90F357E(S) MB90F357TE(S)	Embedded 1 Mbit Flash memory	FE0001 _H

17. Operation with $T_A = +105^\circ\text{C}$ or more

If used exceeding $T_A = +105^\circ\text{C}$, please contact Cypress sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.

The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

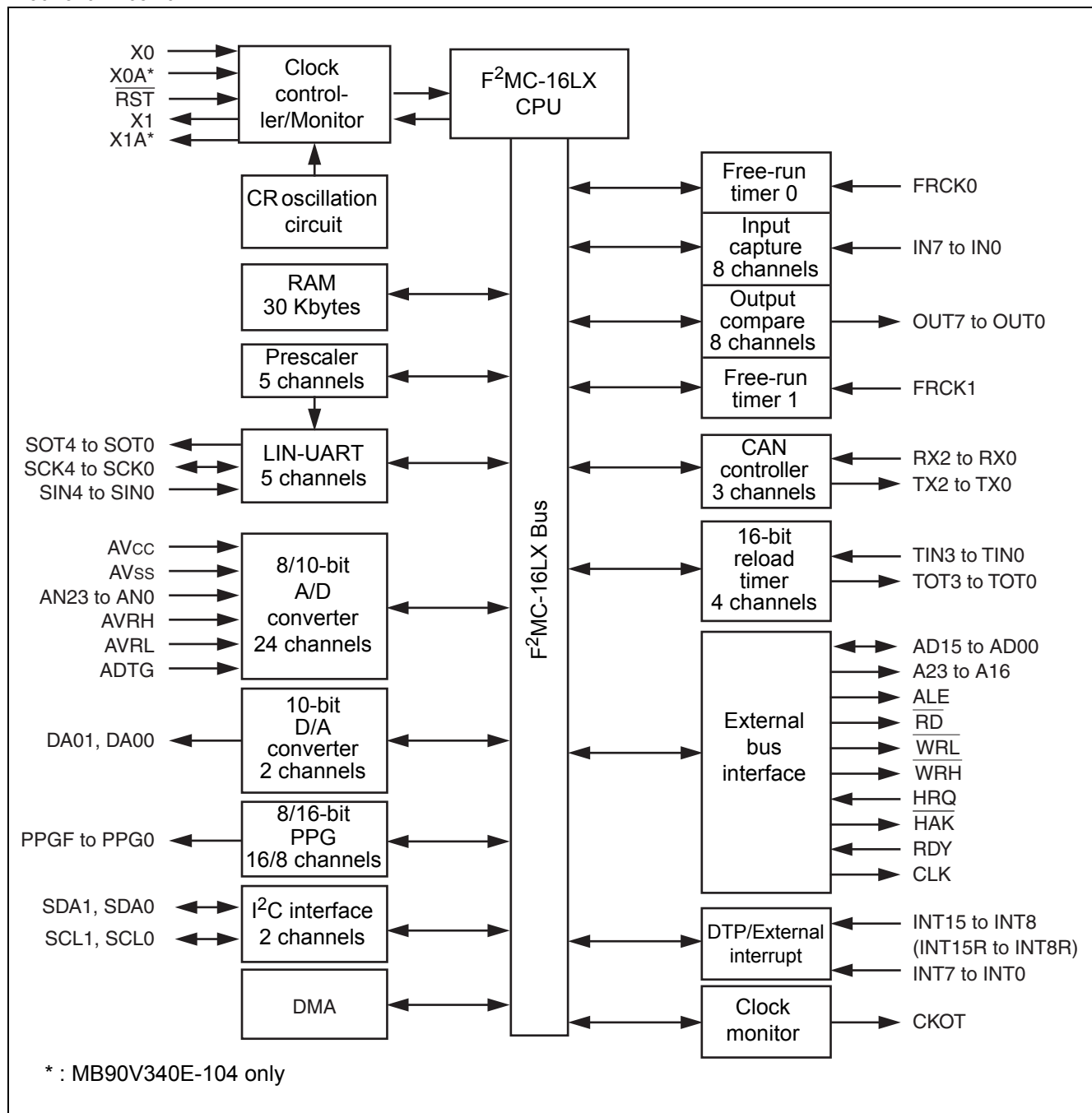
(1) Low voltage detection reset circuit

Detection voltage
4.0 V \pm 0.3 V

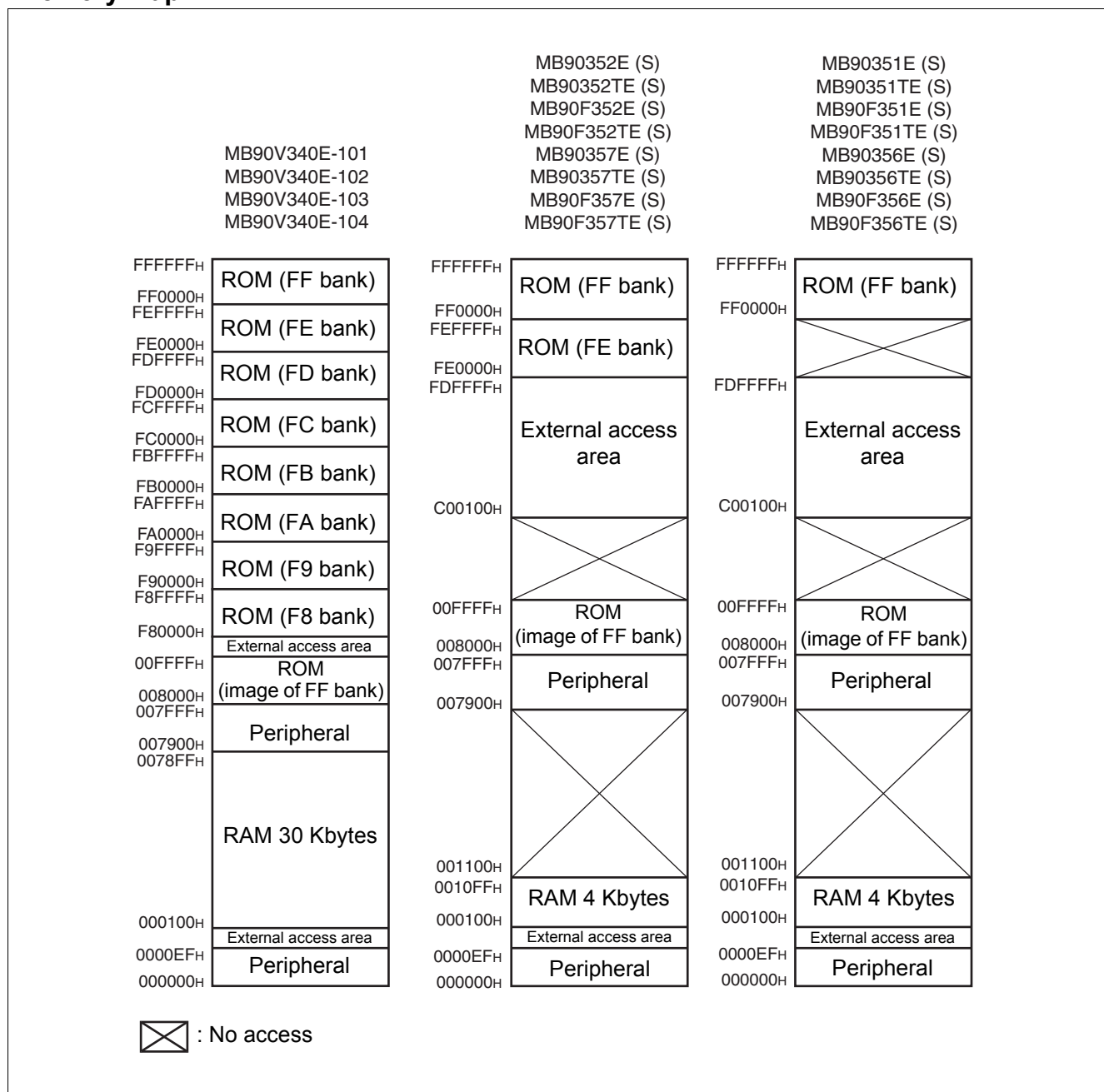
When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to "1" and an internal reset signal is output.

Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.

■ MB90V340E-103/104



9. Memory Map



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.

For example, an attempt to access 00C00_H practically accesses the value at FFC00_H in ROM.

The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

The image between FF800_H and FFFFF_H is visible in bank 00, while the image between FF000_H and FF7FF_H is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
00009B _H	DMA Descriptor Channel Specification Register	DCSR	R/W	DMA	00000000 _B
00009C _H	DMA Status Register L Register	DSRL	R/W		00000000 _B
00009D _H	DMA Status Register H Register	DSRH	R/W		00000000 _B
00009E _H	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 _B
00009F _H	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXX0 _B
0000A0 _H	Low-power Consumption Mode Control Register	LPMCR	W,R/W	Low Power Consumption Control Circuit	00011000 _B
0000A1 _H	Clock Selection Register	CKSCR	R,R/W	Low Power Consumption Control Circuit	11111100 _B
0000A2 _H , 0000A3 _H	Reserved				
0000A4 _H	DMA Stop Status Register	DSSR	R/W	DMA	00000000 _B
0000A5 _H	Automatic Ready Function Selection Register	ARSR	W	External Memory Access	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W		00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
0000A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXX111 _B
0000A9 _H	Timebase Timer Control Register	TBTC	W,R/W	Timebase timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H	Reserved				
0000AC _H	DMA Enable Register L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable Register H Register	DERH	R/W		00000000 _B
0000AE _H	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B

(Continued)

List of Control Registers

Address	Register	Abbreviation	Access	Initial Value
CAN1				
000080 _H	Message buffer enable register	BVALR	R/W	00000000 _B 00000000 _B
000081 _H				
000082 _H	Transmit request register	TREQR	R/W	00000000 _B 00000000 _B
000083 _H				
000084 _H	Transmit cancel register	TCANR	W	00000000 _B 00000000 _B
000085 _H				
000086 _H	Transmission complete register	TCR	R/W	00000000 _B 00000000 _B
000087 _H				
000088 _H	Receive complete register	RCR	R/W	00000000 _B 00000000 _B
000089 _H				
00008A _H	Remote request receiving register	RRTRR	R/W	00000000 _B 00000000 _B
00008B _H				
00008C _H	Receive overrun register	ROVRR	R/W	00000000 _B 00000000 _B
00008D _H				
00008E _H	Reception interrupt enable register	RIER	R/W	00000000 _B 00000000 _B
00008F _H				

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C40 _H	ID register 8	IDR8	R/W	XXXXXXXX _B
007C41 _H				XXXXXXXX _B
007C42 _H				XXXXXXXX _B
007C43 _H				XXXXXXXX _B
007C44 _H	ID register 9	IDR9	R/W	XXXXXXXX _B
007C45 _H				XXXXXXXX _B
007C46 _H				XXXXXXXX _B
007C47 _H				XXXXXXXX _B
007C48 _H	ID register 10	IDR10	R/W	XXXXXXXX _B
007C49 _H				XXXXXXXX _B
007C4A _H				XXXXXXXX _B
007C4B _H				XXXXXXXX _B
007C4C _H	ID register 11	IDR11	R/W	XXXXXXXX _B
007C4D _H				XXXXXXXX _B
007C4E _H				XXXXXXXX _B
007C4F _H				XXXXXXXX _B
007C50 _H	ID register 12	IDR12	R/W	XXXXXXXX _B
007C51 _H				XXXXXXXX _B
007C52 _H				XXXXXXXX _B
007C53 _H				XXXXXXXX _B
007C54 _H	ID register 13	IDR13	R/W	XXXXXXXX _B
007C55 _H				XXXXXXXX _B
007C56 _H				XXXXXXXX _B
007C57 _H				XXXXXXXX _B
007C58 _H	ID register 14	IDR14	R/W	XXXXXXXX _B
007C59 _H				XXXXXXXX _B
007C5A _H				XXXXXXXX _B
007C5B _H				XXXXXXXX _B
007C5C _H	ID register 15	IDR15	R/W	XXXXXXXX _B
007C5D _H				XXXXXXXX _B
007C5E _H				XXXXXXXX _B
007C5F _H				XXXXXXXX _B

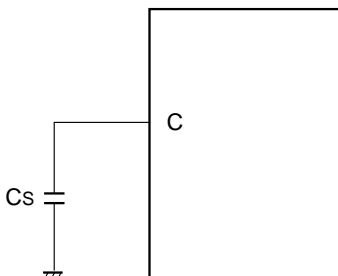
13.2 Recommended Operating Conditions

 $(V_{SS} = AV_{SS} = 0\text{ V})$

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	μF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	-40	—	+125	$^{\circ}\text{C}$	*

* : If used exceeding $T_A = +105^{\circ}\text{C}$, be sure to contact Cypress for reliability limitations.

" C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

13.4 AC Characteristics

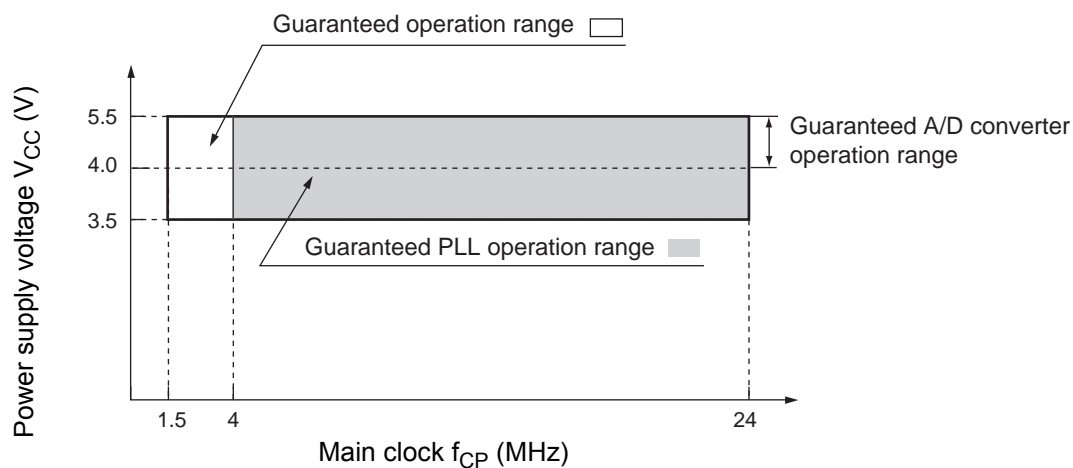
13.4.1 Clock Timing

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

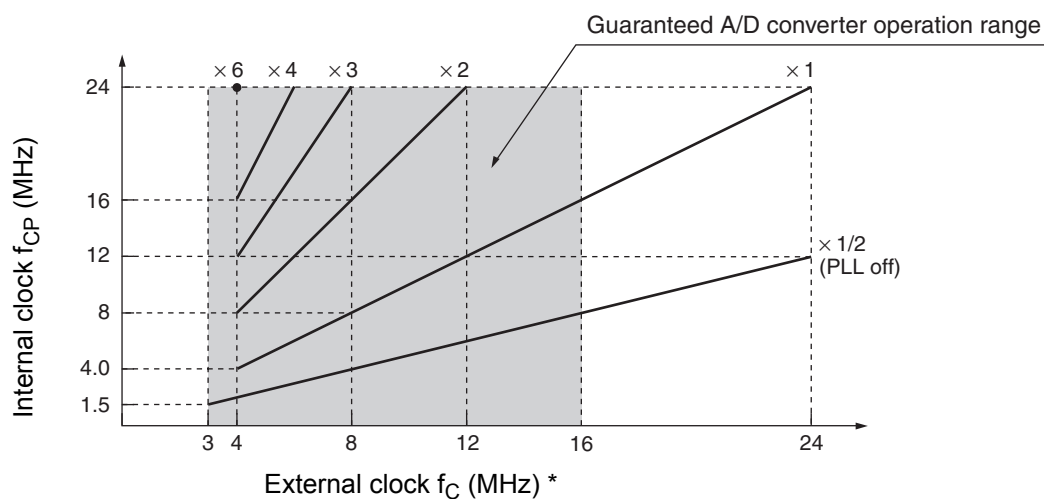
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 (at PLL stop) When using an oscillation circuit
			4	—	16	MHz	1 multiplied PLL When using an oscillation circuit
			4	—	12	MHz	2 multiplied PLL When using an oscillation circuit
			4	—	8	MHz	3 multiplied PLL When using an oscillation circuit
			4	—	6	MHz	4 multiplied PLL When using an oscillation circuit
			—	—	4	MHz	6 multiplied PLL When using an oscillation circuit
		X0	3	—	24	MHz	1/2 (at PLL stop), When using an external clock
			4	—	24	MHz	1 multiplied PLL When using an external clock
			4	—	12	MHz	2 multiplied PLL When using an external clock
			4	—	8	MHz	3 multiplied PLL When using an external clock
			4	—	6	MHz	4 multiplied PLL When using an external clock
			—	—	4	MHz	6 multiplied PLL When using an external clock
		fCL	—	32.768	100	kHz	When using sub clock
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio should be about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock

(Continued)

• PLL guaranteed operation range



Guaranteed operation range of MB90350E series



* : When using crystal oscillator or ceramic oscillator, the maximum clock frequency is 16 MHz.

External clock frequency and internal operation clock frequency

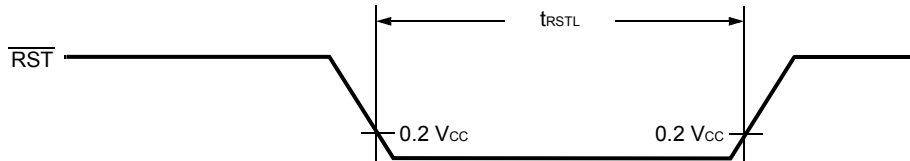
13.4.2 Reset Standby Input

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

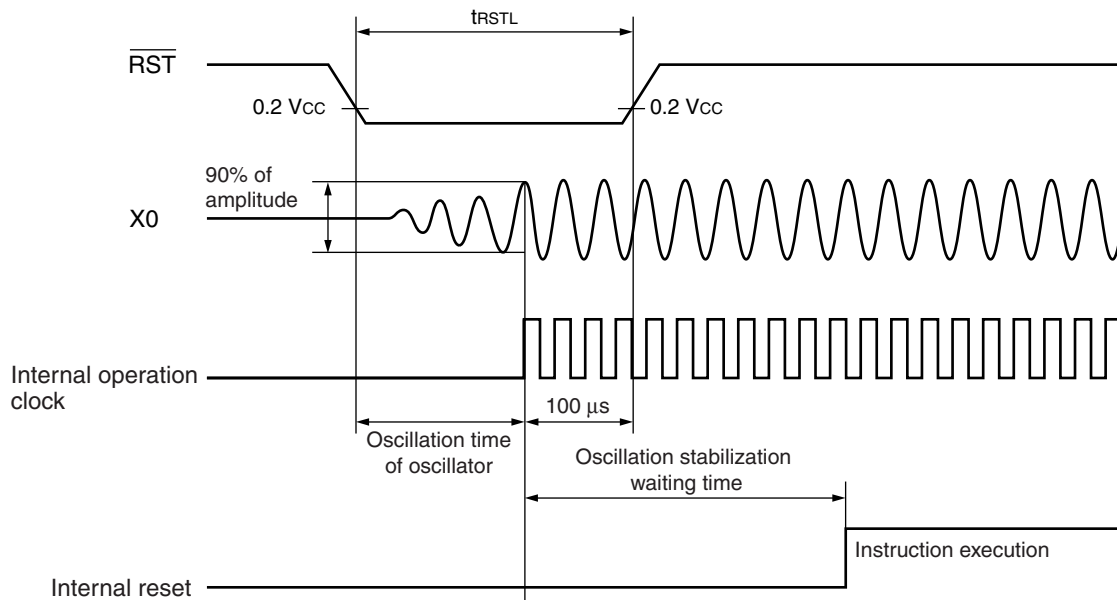
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{\text{RST}}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 μs		μs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	μs	In Main timer mode and PLL timer mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillators, the oscillation time is between hundreds of μs to several ms. With an external clock, the oscillation time is 0 ms.

Under normal operation:



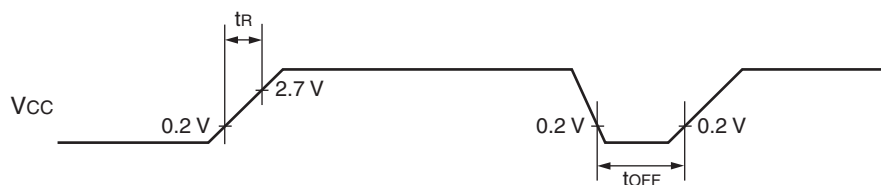
In Stop mode, Sub Clock mode, Sub Sleep mode and, Watch mode:



13.4.3 Power On Reset

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Waiting time until power-on

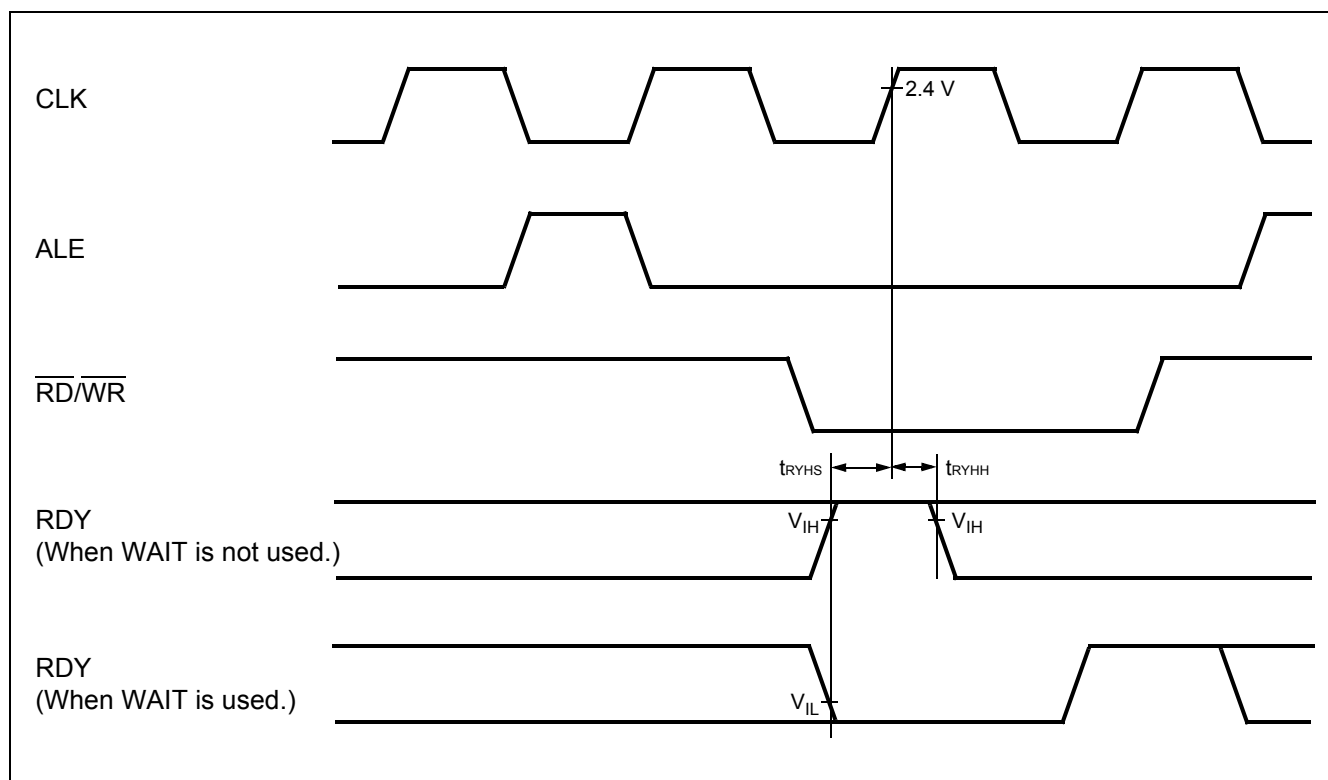


13.4.7 Ready Input Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	45	—	ns	$f_{CP} = 16\text{ MHz}$
				32	—	ns	$f_{CP} = 24\text{ MHz}$
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY set-up time is insufficient, use the auto-ready function.

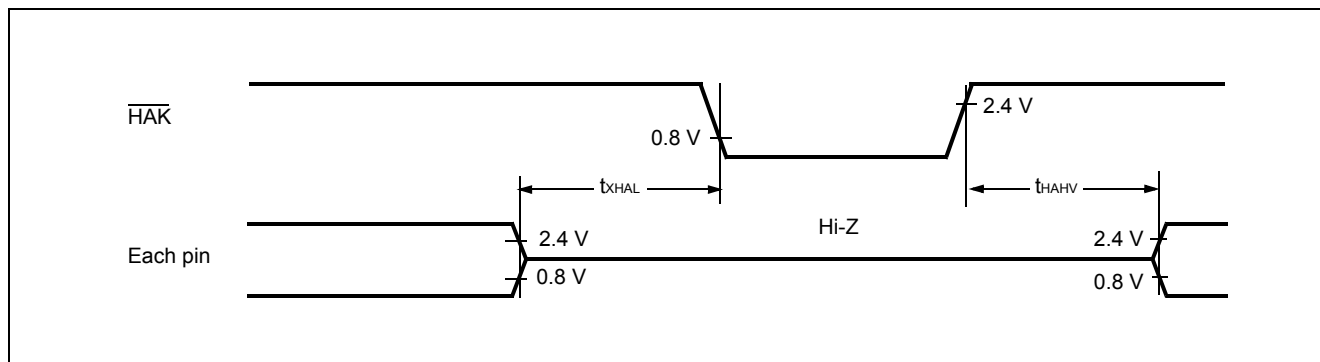


13.4.8 Hold Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Units
				Min	Max	
Pin floating $\rightarrow \overline{\text{HAK}} \downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns
$\overline{\text{HAK}} \uparrow$ time \rightarrow Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$		t_{CP}	$2 t_{CP}$	ns

Note : There is more than 1 machine cycle from when HRQ pin reads in until the $\overline{\text{HAK}}$ is changed.

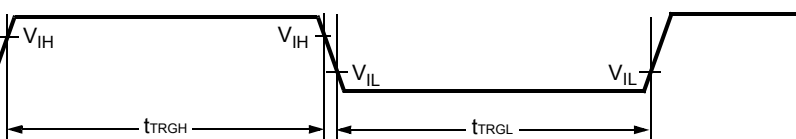


13.4.10 Trigger Input Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	$5 t_{CP}$	—	ns

INT8 to INT15,
INT9R to INT11R,
ADTG

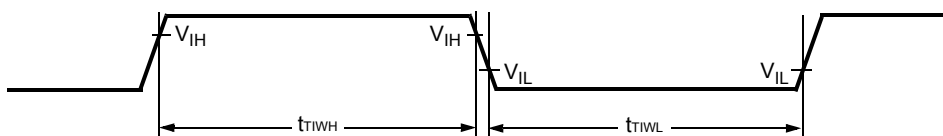


13.4.11 Timer Related Resource Input Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN1, TIN3, IN0, IN1, IN4 to IN7	—	$4 t_{CP}$	—	ns

TIN1, TIN3,
IN0, IN1,
IN4 to IN7



13.4.12 Timer Related Resource Output Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)





Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK \uparrow \rightarrow T_{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Flash memory Data Retention Time	Average $T_A = +85^{\circ}\text{C}$	20	—	—	year	*

* : Corresponding value comes from the technology reliability evaluation result.

(Using Arrhenius equation to translate high temperature measurements test result into normalized value at +85°C)

14. Ordering Information

Part number	Package	Remarks
MB90F351EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm  0.65 mm pitch	Flash memory products (64 Kbytes)
MB90F351ESPMC		
MB90F351TEPMC		
MB90F351TESPMC		
MB90F356EPMC		
MB90F356ESPMC		
MB90F356TEPMC		
MB90F356TESPMC		
MB90F352EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm  0.65 mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ESPMC		
MB90F352TEPMC		
MB90F352TESPMC		
MB90F357EPMC		
MB90F357ESPMC		
MB90F357TEPMC		
MB90F357TESPMC		
MB90351EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm  0.65 mm pitch	MASK ROM products (64 Kbytes)
MB90351ESPMC		
MB90351TEPMC		
MB90351TESPMC		
MB90356EPMC		
MB90356ESPMC		
MB90356TEPMC		
MB90356TESPMC		
MB90352EPMC	64-pin plastic LQFP FPT-64P-M23 12.0 mm  0.65 mm pitch	MASK ROM products (128 Kbytes)
MB90352ESPMC		
MB90352TEPMC		
MB90352TESPMC		
MB90357EPMC		
MB90357ESPMC		
MB90357TEPMC		
MB90357TESPMC		

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