# Infineon Technologies - MB90352ESPMC-GS-201E1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, WDT |
| Number of I/O | 51 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | A/D 15x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90352espmc-gs-201e1 |

- 8/16-bit PPG timer : 8-bit ∞ 10 channels or 16-bit × 6 channels
- 16-bit reload timer : 2 channels (only Evaluation products has 4 channels)
- 16- bit input/output timer
  - 16-bit free-run timer : 2 channels (FRT0 : ICU0/1, FRT1 : ICU4/5/6/7, OCU4/5/6/7)
  - 16- bit input capture: (ICU) : 6 channels
  - 16-bit output compare : (OCU) : 4 channels

### FULL-CAN interface: 1 channel

- Compliant with CAN standard Version2.0 Part A and Part B
- 16 message buffers are built-in
- CAN wake-up function

### LIN-UART: 2 channels

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

### $I^2C$ interface: 1 channel

Up to 400 kbps transfer rate

### DTP/External interrupt: 8 channels, CAN wakeup: 1 channel

Module for activation of extended intelligent I/O service ($EI^2OS$), DMA, and generation of external interrupt by external input.

### Delay interrupt generator module

Generates interrupt request for task switching.

### 8/10-bit A/D converter: 15 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3 µs (at 24 MHz machine clock, including sampling time)

### Address matching detection (Program patch) function

- Address matching detection for 6 address pointers.

### Capable of changing input voltage level for port

- Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)
- TTL level (corresponds to external bus pins only, initial level of these pins is TTL in external bus mode)

### Low voltage/CPU operation detection reset (devices with T-suffix)

- Detects low voltage (4.0 V ± 0.3 V) and resets automatically
- Resets automatically when program is runaway and counter is not cleared within interval time
  (approx. 262 ms : external 4 MHz)

### Dual operation Flash memory (only devices 128 Kbytes Flash memory)

- Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.

### Supported $T_A$ = + 125°C

The maximum operating frequency is 24 MHz* : (at $T_A$ = +125°C) .

### Flash security function

- Protects the content of Flash memory
  (MB90F352x, MB90F357x only)

### External bus interface

- 4 Mbytes external memory space
  MB90F351E(S), MB90F351TE(S), MB90F352E(S), MB90F352TE(S) : External bus Interface can not be used in internal vector mode. It can be used only in external vector mode.

* : If used exceeding $T_A$ = + 105 °C, be sure to contact Cypress for reliability limitations.

*(Continued)*

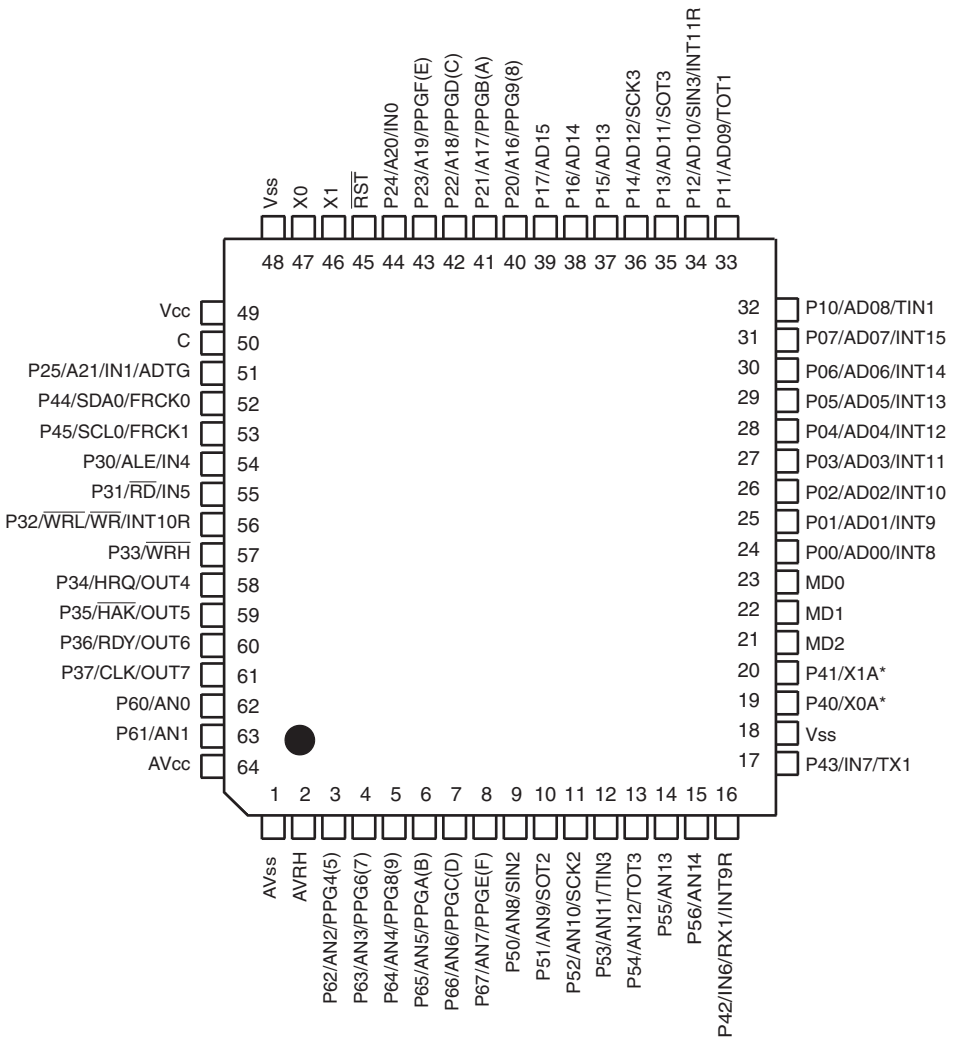
| Parameter \ Part Number | MB90F351E<br>MB90F352E | MB90F351TE<br>MB90F352TE | MB90F351ES<br>MB90F352ES | MB90F351TES<br>MB90F352TES |
|---|---|---|---|---|
| 16-bit Input capture | 6 channels | | | |
| | Retains 16-bit free-run timer value by (rising edge, falling edge or rising & falling edge) , signals an interrupt. | | | |
| 8/16-bit programmable pulse generator | 6 channels (16-bit)/10 channels (8-bit)<br>8-bit reload counters × 12<br>8-bit reload registers for L pulse width × 12<br>8-bit reload registers for H pulse width×12 | | | |
| | Supports 8-bit and 16-bit operation modes.<br>A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter.<br>Operation clock frequency : fsys, fsys/$2^1$, fsys/$2^2$, fsys/$2^3$, fsys/$2^4$ or 128 μs@fosc = 4 MHz<br>(fsys = Machine clock frequency, fosc = Oscillation clock frequency) | | | |
| CAN interface | 1 channel | | | |
| | Compliant with CAN standard Version2.0 Part A and Part B.<br>Automatic re-transmission in case of error<br>Automatic transmission responding to Remote Frame<br>16 prioritized message buffers for data and ID<br>Supports multiple messages.<br>Flexible configuration of acceptance filtering :<br>Full bit compare/Full bit mask/Two partial bit masks<br>Supports up to 1 Mbps. | | | |
| External interrupt | 8 channels | | | |
| | Can be used rising edge, falling edge, starting up by “H”/“L” level input, external interrupt, extended intelligent I/O services (EI$^2$OS) and DMA. | | | |
| D/A converter | — | | | |
| I/O ports | Virtually all external pins can be used as general purpose I/O port.<br>All push-pull outputs<br>Bit-wise settable as input/output or peripheral signal<br>Settable as CMOS schmitt trigger/ automotive inputs<br>TTL input level settable for external bus (only for external bus pin) | | | |
| Flash memory | Supports automatic programming, Embedded Algorithm<br>Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Number of erase cycles : 10000 times<br>Data retention time : 20 years<br>Boot block configuration<br>Erase can be performed on each block.<br>Block protection with external programming voltage<br>Flash Security Feature for protecting the content of the Flash (MB90F352E(S) and MB90F352TE(S) only) | | | |
| Corresponding evaluation name | MB90V340E-102 | | MB90V340E-101 | |

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

## 4. Pin Assignments

■ MB90351E (S) , MB90351TE (S) , MB90F351E (S) , MB90F351TE (S) , MB90352E (S) , MB90352TE (S) , MB90F352E (S) , MB90F352TE (S) , MB90356E (S) , MB90356TE (S) , MB90F356E (S) , MB90F356TE (S) , MB90357E (S) , MB90357TE (S) , MB90F357E (S) , MB90F357TE (S)

(TOP VIEW)




(FPT-64P-M23, FPT-64P-M24)

* : Devices without S-suffix : X0A, X1A
Devices with S-suffix : P40, P41

| Pin No. | Pin name | I/O Circuit type* | Function |
|---|---|---|---|
| 39 | P17 | G | General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | AD15 | | Input/output pin for external bus address data bus bit 15. This function is enabled when external bus is enabled. |
| 40 to 43 | P20 to P23 | G | General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pins are enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1. |
| | A16 to A19 | | Output pins for A16 to A19 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins A16 to A19. |
| | PPG9 (8)<br>PPGB (A)<br>PPGD (C)<br>PPGF (E) | | Output pins for PPGs |
| 44 | P24 | G | General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1. |
| | A20 | | Output pin for A20 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A20. |
| | IN0 | | Data sample input pin for input capture ICU0 |
| 51 | P25 | G | General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1. |
| | A21 | | Output pin for A21 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A21. |
| | IN1 | | Data sample input pin for input capture ICU1 |
| | ADTG | | Trigger input pin for A/D converter |
| 52 | P44 | H | General purpose I/O port |
| | SDA0 | | Serial data I/O pin for $I^2C$ 0 |
| | FRCK0 | | Input pin for the 16-bit Free-run Timer 0 |
| 53 | P45 | H | General purpose I/O port |
| | SCL0 | | Serial clock I/O pin for $I^2C$ 0 |
| | FRCK1 | | Input pin for the 16-bit Free-run Timer 1 |

*(Continued)*

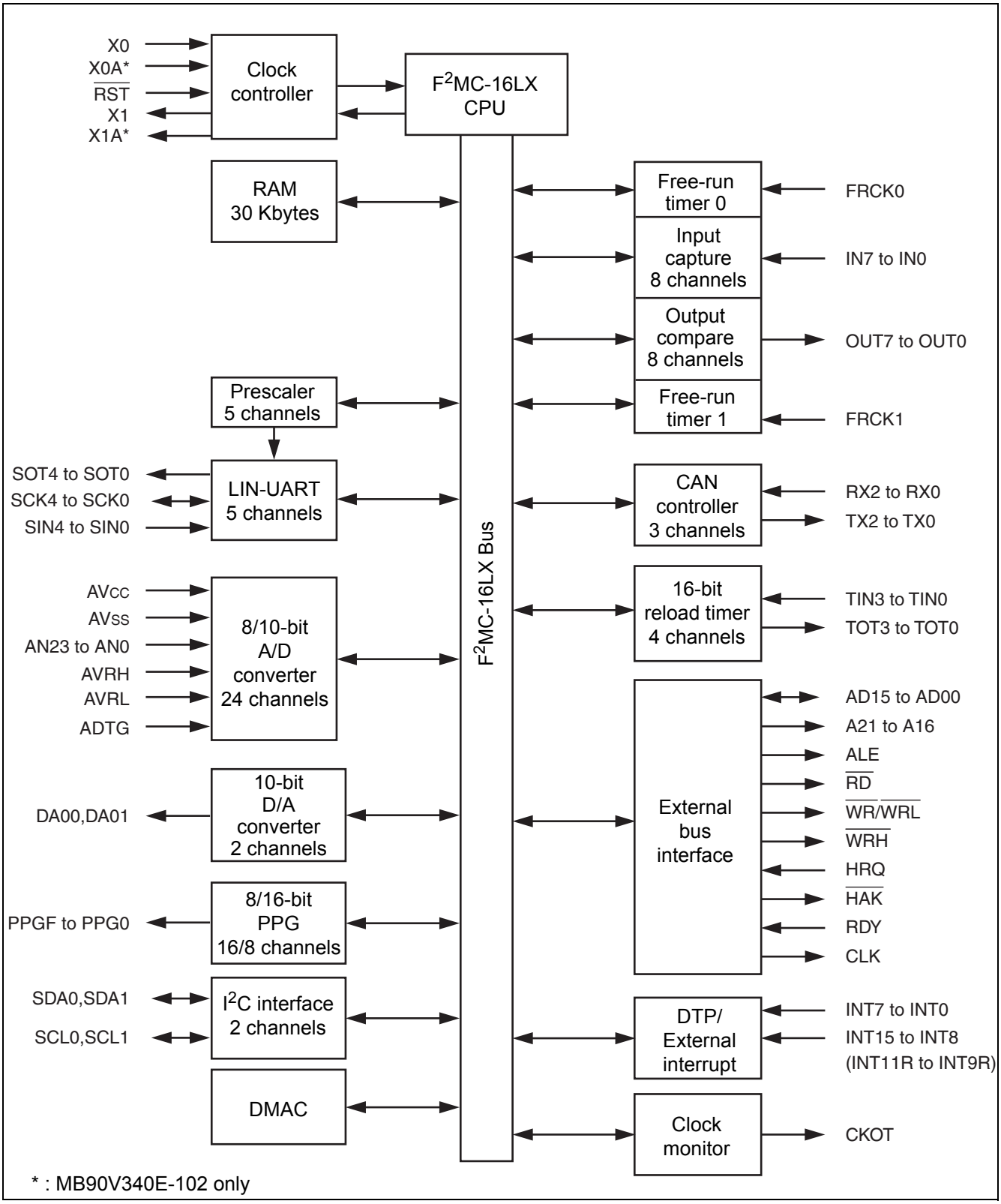
*(Continued)*

| Pin No. | Pin name | I/O Circuit type* | Function |
|---|---|---|---|
| 61 | P37 | G | General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the CLK output disabled. |
| | CLK | | CLK output pin. This function is enabled when both the external bus and CLK output are enabled. |
| | OUT7 | | Wave form output pin for output compare OCU7 |
| 62, 63 | P60, P61 | I | General purpose I/O ports |
| | AN0, AN1 | | Analog input pins for A/D converter |
| 64 | $AV_{CC}$ | K | $V_{CC}$ power input pin for analog circuits |
| 2 | AVRH | L | Reference voltage input for the A/D converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to $AV_{CC}$. |
| 1 | $AV_{SS}$ | K | $V_{SS}$ power input pin for analog circuits |
| 22, 23 | MD1, MD0 | C | Input pins for specifying the operating mode |
| 21 | MD2 | D | Input pin for specifying the operating mode |
| 49 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pin |
| 18, 48 | $V_{SS}$ | — | Power (0 V) input pins |
| 50 | C | K | This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic capacitor. |

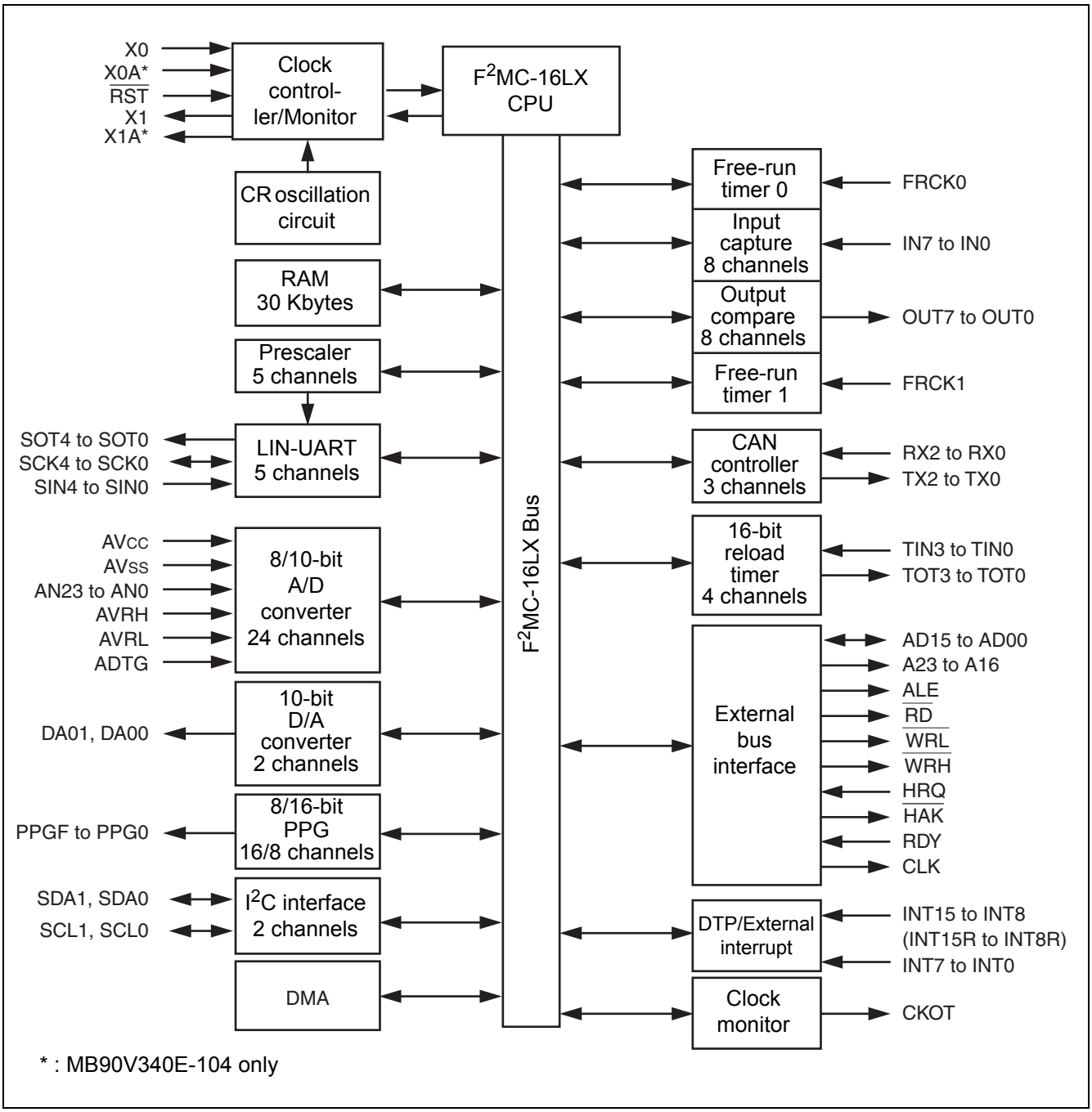
* : For the I/O circuit type, refer to “I/O Circuit Type”.

## 8. Block Diagrams

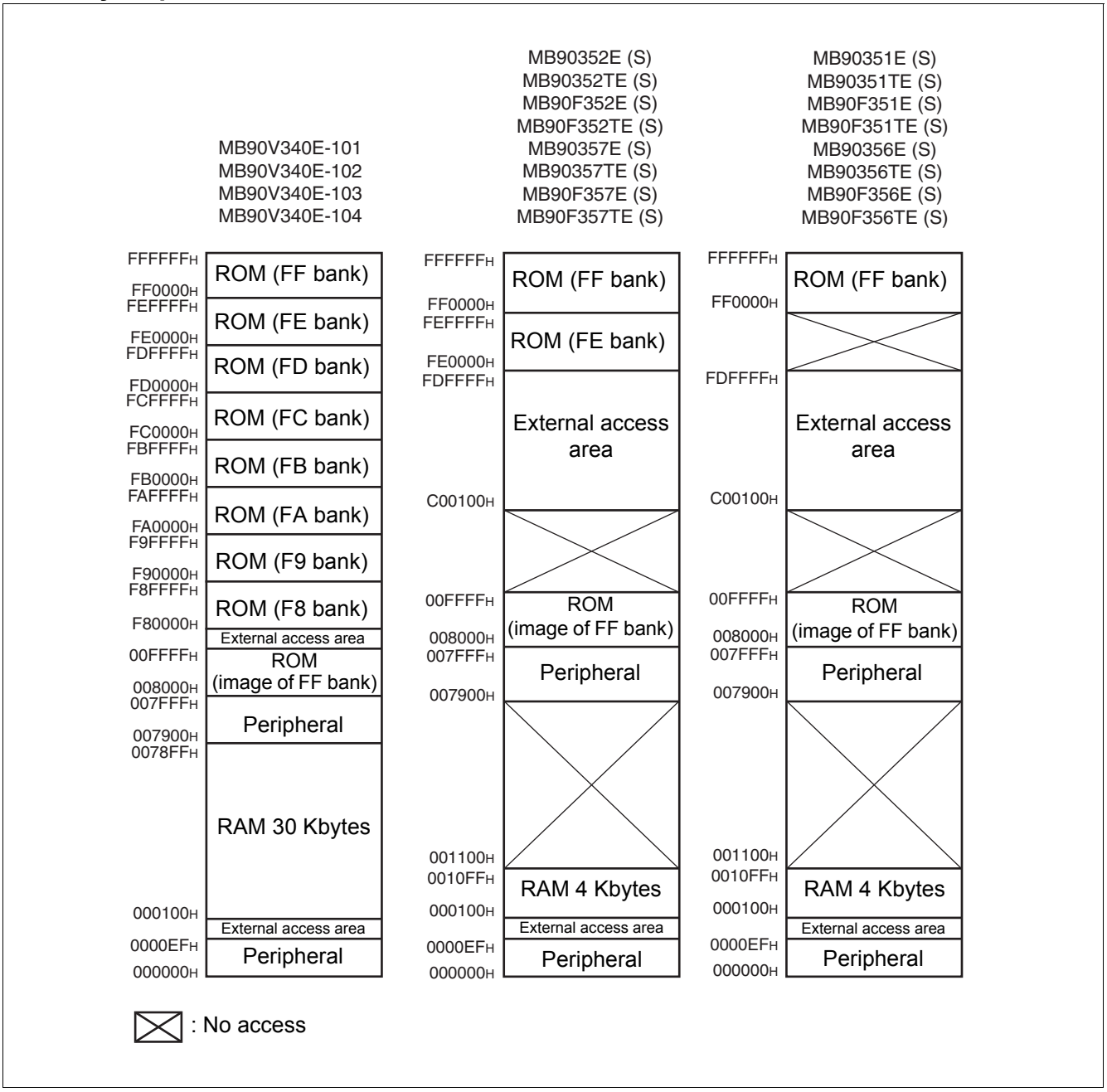
■ MB90V340E-101/102



■ MB90V340E-103/104



## 9. Memory Map




Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access $00C000_H$ practically accesses the value at $FFC000_H$ in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $00009B_H$ | DMA Descriptor Channel Specification Register | DCSR | R/W | DMA | $00000000_B$ |
| $00009C_H$ | DMA Status Register L Register | DSRL | R/W | | $00000000_B$ |
| $00009D_H$ | DMA Status Register H Register | DSRH | R/W | | $00000000_B$ |
| $00009E_H$ | Address Detect Control Register 0 | PACSR0 | R/W | Address Match Detection 0 | $00000000_B$ |
| $00009F_H$ | Delayed Interrupt/Release Register | DIRR | R/W | Delayed Interrupt | $XXXXXXX0_B$ |
| $0000A0_H$ | Low-power Consumption Mode Control Register | LPMCR | W,R/W | Low Power Consumption Control Circuit | $00011000_B$ |
| $0000A1_H$ | Clock Selection Register | CKSCR | R,R/W | Low Power Consumption Control Circuit | $11111100_B$ |
| $0000A2_H$, $0000A3_H$ | Reserved | | | | |
| $0000A4_H$ | DMA Stop Status Register | DSSR | R/W | DMA | $00000000_B$ |
| $0000A5_H$ | Automatic Ready Function Selection Register | ARSR | W | External Memory Access | $0011XX00_B$ |
| $0000A6_H$ | External Address Output Control Register | HACR | W | | $00000000_B$ |
| $0000A7_H$ | Bus Control Signal Selection Register | ECSR | W | | $0000000X_B$ |
| $0000A8_H$ | Watchdog Control Register | WDTC | R,W | Watchdog Timer | $XXXXX111_B$ |
| $0000A9_H$ | Timebase Timer Control Register | TBTC | W,R/W | Timebase timer | $1XX00100_B$ |
| $0000AA_H$ | Watch Timer Control Register | WTC | R,R/W | Watch Timer | $1X001000_B$ |
| $0000AB_H$ | Reserved | | | | |
| $0000AC_H$ | DMA Enable Register L Register | DERL | R/W | DMA | $00000000_B$ |
| $0000AD_H$ | DMA Enable Register H Register | DERH | R/W | | $00000000_B$ |
| $0000AE_H$ | Flash Control Status Register (Flash Devices only. Otherwise reserved) | FMCS | R,R/W | Flash memory | $000X0000_B$ |
| $0000AF_H$ | Reserved | | | | |
| $0000B0_H$ | Interrupt Control Register 00 | ICR00 | W,R/W | Interrupt Control | $00000111_B$ |
| $0000B1_H$ | Interrupt Control Register 01 | ICR01 | W,R/W | | $00000111_B$ |
| $0000B2_H$ | Interrupt Control Register 02 | ICR02 | W,R/W | | $00000111_B$ |
| $0000B3_H$ | Interrupt Control Register 03 | ICR03 | W,R/W | | $00000111_B$ |
| $0000B4_H$ | Interrupt Control Register 04 | ICR04 | W,R/W | | $00000111_B$ |
| $0000B5_H$ | Interrupt Control Register 05 | ICR05 | W,R/W | | $00000111_B$ |
| $0000B6_H$ | Interrupt Control Register 06 | ICR06 | W,R/W | | $00000111_B$ |
| $0000B7_H$ | Interrupt Control Register 07 | ICR07 | W,R/W | | $00000111_B$ |
| $0000B8_H$ | Interrupt Control Register 08 | ICR08 | W,R/W | | $00000111_B$ |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $0000B9_H$ | Interrupt Control Register 09 | ICR09 | W,R/W | Interrupt Control | $00000111_B$ |
| $0000BA_H$ | Interrupt Control Register 10 | ICR10 | W,R/W | | $00000111_B$ |
| $0000BB_H$ | Interrupt Control Register 11 | ICR11 | W,R/W | | $00000111_B$ |
| $0000BC_H$ | Interrupt Control Register 12 | ICR12 | W,R/W | | $00000111_B$ |
| $0000BD_H$ | Interrupt Control Register 13 | ICR13 | W,R/W | | $00000111_B$ |
| $0000BE_H$ | Interrupt Control Register 14 | ICR14 | W,R/W | | $00000111_B$ |
| $0000BF_H$ | Interrupt Control Register 15 | ICR15 | W,R/W | | $00000111_B$ |
| $0000C0_H$ to $0000C9_H$ | Reserved | | | | |
| $0000CA_H$ | External Interrupt Enable Register 1 | ENIR1 | R/W | External Interrupt 1 | $00000000_B$ |
| $0000CB_H$ | External Interrupt Source Register 1 | EIRR1 | R/W | | $XXXXXXXX_B$ |
| $0000CC_H$ | External Interrupt Level Register 1 | ELVR1 | R/W | | $00000000_B$ |
| $0000CD_H$ | External Interrupt Level Register 1 | ELVR1 | R/W | | $00000000_B$ |
| $0000CE_H$ | External Interrupt Source Select Register | EISSR | R/W | | $00000000_B$ |
| $0000CF_H$ | PLL/Sub clock Control register | PSCCR | W | PLL | $XXXX0000_B$ |
| $0000D0_H$ | DMA Buffer Address Pointer L Register | BAPL | R/W | DMA | $XXXXXXXX_B$ |
| $0000D1_H$ | DMA Buffer Address Pointer M Register | BAPM | R/W | | $XXXXXXXX_B$ |
| $0000D2_H$ | DMA Buffer Address Pointer H Register | BAPH | R/W | | $XXXXXXXX_B$ |
| $0000D3_H$ | DMA Control Register | DMACS | R/W | | $XXXXXXXX_B$ |
| $0000D4_H$ | I/O Register Address Pointer L Register | IOAL | R/W | | $XXXXXXXX_B$ |
| $0000D5_H$ | I/O Register Address Pointer H Register | IOAH | R/W | | $XXXXXXXX_B$ |
| $0000D6_H$ | Data Counter L Register | DCTL | R/W | | $XXXXXXXX_B$ |
| $0000D7_H$ | Data Counter H Register | DCTH | R/W | | $XXXXXXXX_B$ |
| $0000D8_H$ | Serial Mode Register 2 | SMR2 | W,R/W | UART2 | $00000000_B$ |
| $0000D9_H$ | Serial Control Register 2 | SCR2 | W,R/W | | $00000000_B$ |
| $0000DA_H$ | Reception/Transmission Data Register 2 | RDR2/TDR2 | R/W | | $00000000_B$ |
| $0000DB_H$ | Serial Status Register 2 | SSR2 | R,R/W | | $00001000_B$ |
| $0000DC_H$ | Extended Communication Control Register 2 | ECCR2 | R,W, R/W | | $000000XX_B$ |
| $0000DD_H$ | Extended Status/Control Register 2 | ESCR2 | R/W | | $00000100_B$ |
| $0000DE_H$ | Baud Rate Generator Register 20 | BGR20 | R/W | | $00000000_B$ |

*(Continued)*

*(Continued)*

| Interrupt cause | EI$^2$OS corresponding | DMA ch number | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|---|
| | | | Number | Address | Number | Address |
| UART 2 RX | Y2 | 14 | #39 | $FFFF60_H$ | ICR14 | $0000BE_H$ |
| UART 2 TX | Y1 | 15 | #40 | $FFFF5C_H$ | | |
| Flash Memory | N | — | #41 | $FFFF58_H$ | ICR15 | $0000BF_H$ |
| Delayed Interrupt | N | — | #42 | $FFFF54_H$ | | |

Y1 : Usable

Y2 : Usable, with EI$^2$OS stop function

N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When the peripheral resources sharing the ICR register use extended intelligent I/O service, only one can use EI$^2$OS at a time.
- When either of the two peripheral resources sharing the ICR register specifies EI$^2$OS, the other one cannot use interrupts.

# 13. Electrical Characteristics

## 13.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$ | $V_{SS}$ − 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ − 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC} = AV_{CC}$*2 |
| | AVRH | $V_{SS}$ − 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC} \geq AVRH$*2 |
| Input voltage*1 | $V_I$ | $V_{SS}$ − 0.3 | $V_{SS}$ + 6.0 | V | *3 |
| Output voltage*1 | $V_O$ | $V_{SS}$ − 0.3 | $V_{SS}$ + 6.0 | V | *3 |
| Maximum Clamp Current | $I_{CLAMP}$ | −4.0 | +4.0 | mA | *5 |
| Total Maximum Clamp Current | $\Sigma\lvert I_{CLAMP}\rvert$ | — | 40 | mA | *5 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | *4 |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | *4 |
| “L” level maximum overall output current | $\Sigma I_{OL}$ | — | 100 | mA | *4 |
| “L” level average overall output current | $\Sigma I_{OLAV}$ | — | 50 | mA | *4 |
| “H” level maximum output current | $I_{OH}$ | — | −15 | mA | *4 |
| “H” level average output current | $I_{OHAV}$ | — | −4 | mA | *4 |
| “H” level maximum overall output current | $\Sigma I_{OH}$ | — | −100 | mA | *4 |
| “H” level average overall output current | $\Sigma I_{OHAV}$ | — | −50 | mA | *4 |
| Power consumption | $P_D$ | — | 454 | mW | |
| Operating temperature | $T_A$ | −40 | +105 | °C | |
| | | −40 | +125 | °C | *6 |
| Storage temperature | $T_{STG}$ | −55 | +150 | °C | |

*(Continued)*

## 13.3 DC Characteristics

($T_A$ = −40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage (At $V_{CC}$ = 5 V ± 10%) | $V_{IHS}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50) |
| | $V_{IHA}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Pin inputs if Automotive input levels are selected |
| | $V_{IHT}$ | — | — | 2.0 | — | $V_{CC}$ + 0.3 | V | Pin inputs if TTL input levels are selected |
| | $V_{IHS}$ | — | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | P12, P15, P50 inputs if CMOS input levels are selected |
| | $V_{IHI}$ | — | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | P44, P45 inputs if CMOS hysteresis input levels are selected |
| | $V_{IHR}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | $\overline{RST}$ input pin (CMOS hysteresis) |
| | $V_{IHM}$ | — | — | $V_{CC}$ − 0.3 | — | $V_{CC}$ + 0.3 | V | MD input pin |
| "L" level input voltage (At $V_{CC}$ = 5 V ± 10%) | $V_{ILS}$ | — | — | $V_{SS}$ − 0.3 | — | 0.2 $V_{CC}$ | V | Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50) |
| | $V_{ILA}$ | — | — | $V_{SS}$ − 0.3 | — | 0.5 $V_{CC}$ | V | Pin inputs if Automotive input levels are selected |
| | $V_{ILT}$ | — | — | $V_{SS}$ − 0.3 | — | 0.8 | V | Pin inputs if TTL input levels are selected |
| | $V_{ILS}$ | — | — | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | P12, P15, P50 inputs if CMOS input levels are selected |
| | $V_{ILI}$ | — | — | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | P44, P45 inputs if CMOS hysteresis input levels are selected |
| | $V_{ILR}$ | — | — | $V_{SS}$ − 0.3 | — | 0.2 $V_{CC}$ | V | $\overline{RST}$ input pin (CMOS hysteresis) |
| | $V_{ILM}$ | — | — | $V_{SS}$ − 0.3 | — | $V_{SS}$ + 0.3 | V | MD input pin |
| Output "H" voltage | $V_{OH}$ | Normal outputs | $V_{CC}$ = 4.5 V, $I_{OH}$ = −4.0 mA | $V_{CC}$ − 0.5 | — | — | V | |
| Output "H" voltage | $V_{OHI}$ | $I^2C$ current outputs | $V_{CC}$ = 4.5 V, $I_{OH}$ = −3.0 mA | $V_{CC}$ − 0.5 | — | — | V | |

*(Continued)*

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Sym-bol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CCL}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub clock operation $T_A$ = +25°C | — | 70 | 140 | µA | MB90351E<br>MB90F351E<br>MB90352E<br>MB90F352E<br>MB90356E<br>MB90F356E<br>MB90357E<br>MB90F357E |
| | | | $V_{CC}$ = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub clock operation $T_A$ = +25°C | — | 100 | 200 | µA | MB90356E<br>MB90F356E<br>MB90357E<br>MB90F357E |
| | | | $V_{CC}$ = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation $T_A$ = +25°C | — | 100 | 200 | µA | MB90356ES<br>MB90F356ES<br>MB90357ES<br>MB90F357ES |
| | | | $V_{CC}$ = 5.0 V, Internal frequency: 8 kHz, During stopping clock supervisor, At sub clock operation $T_A$ = +25°C | — | 120 | 240 | µA | MB90351TE<br>MB90F351TE<br>MB90352TE<br>MB90F352TE<br>MB90356TE<br>MB90F356TE<br>MB90357TE<br>MB90F357TE |
| | | | $V_{CC}$ = 5.0 V, Internal frequency: 8 kHz, During operating clock supervisor, At sub clock operation $T_A$ = +25°C | — | 150 | 300 | µA | MB90356TE<br>MB90F356TE<br>MB90357TE<br>MB90F357TE |
| | | | $V_{CC}$ = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation $T_A$ = +25°C | — | 150 | 300 | µA | MB90356TES<br>MB90F356TES<br>MB90357TES<br>MB90F357TES |

*(Continued)*

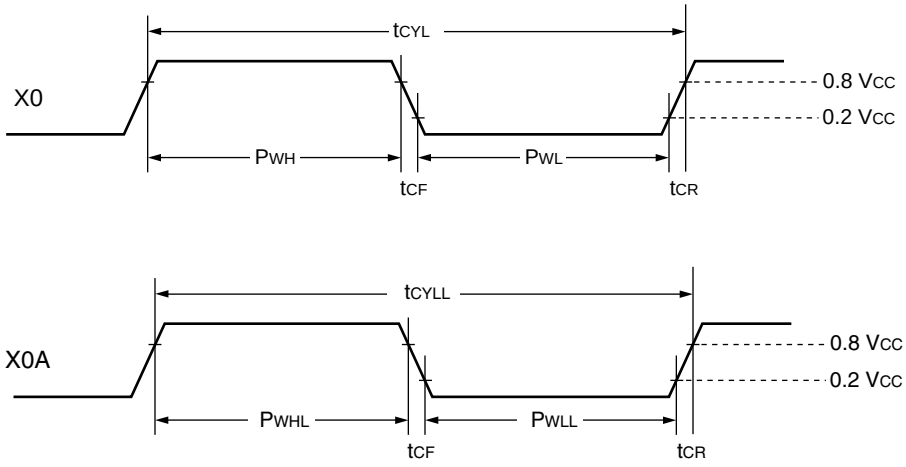
*(Continued)*

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Internal operating clock frequency (machine clock) | $f_{CP}$ | — | 1.5 | — | 24 | MHz | When using main clock |
| | $f_{CPL}$ | — | — | 8.192 | 50 | kHz | When using sub clock |
| Internal operating clock cycle time (machine clock) | $t_{CP}$ | — | 41.67 | — | 666 | ns | When using main clock |
| | $t_{CPL}$ | — | 20 | 122.1 | — | µs | When using sub clock |

*: The limitation is in the range of the clock frequency when PLL is used. Use within the range in graph of "· PLL guaranteed operation range External clock frequency and internal operation clock frequency".

- Clock Timing



*13.4.9 LIN-UART2/3*

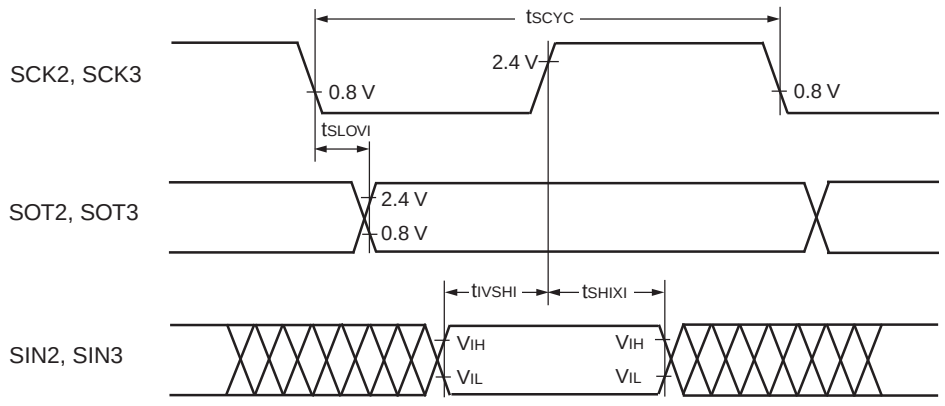
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

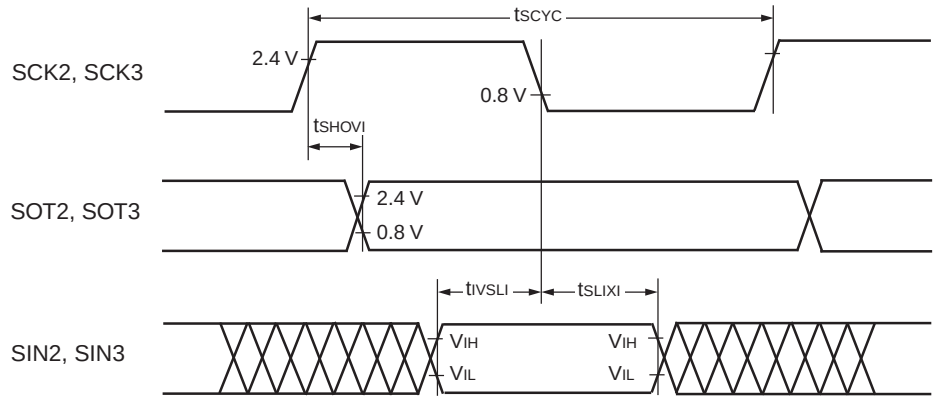
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK2, SCK3 | Internal shift clock mode output pins are CL = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK2, SCK3 SOT2, SOT3 | | –50 | +50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK2, SCK3 SIN2, SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK2, SCK3 SIN2, SIN3 | | 0 | — | ns |
| Serial clock “L” pulse width | $t_{SHSL}$ | SCK2, SCK3 | External shift clock mode output pins are CL = 80 pF + 1 TTL. | 3 $t_{CP}$ - $t_R$ | — | ns |
| Serial clock “H” pulse width | $t_{SLSH}$ | SCK2, SCK3 | | $t_{CP}$ + 10 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK2, SCK3 SOT2, SOT3 | | — | 2 $t_{CP}$ + 60 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCK2, SCK3 SIN2, SIN3 | | 30 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | SCK2, SCK3 SIN2, SIN3 | | $t_{CP}$ + 30 | — | ns |
| SCK fall time | $t_F$ | SCK2, SCK3 | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK2, SCK3 | | — | 10 | ns |

Notes :
- AC characteristic in CLK synchronized mode.
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

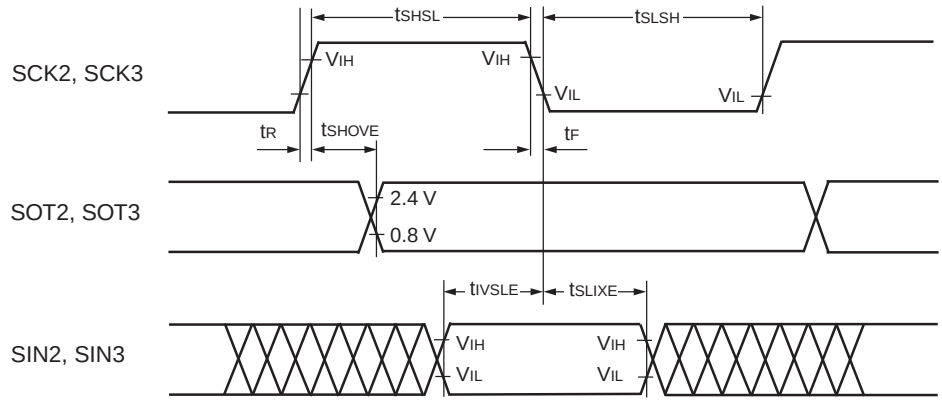
″ Internal Shift Clock Mode



• Internal Shift Clock Mode




• External Shift Clock Mode

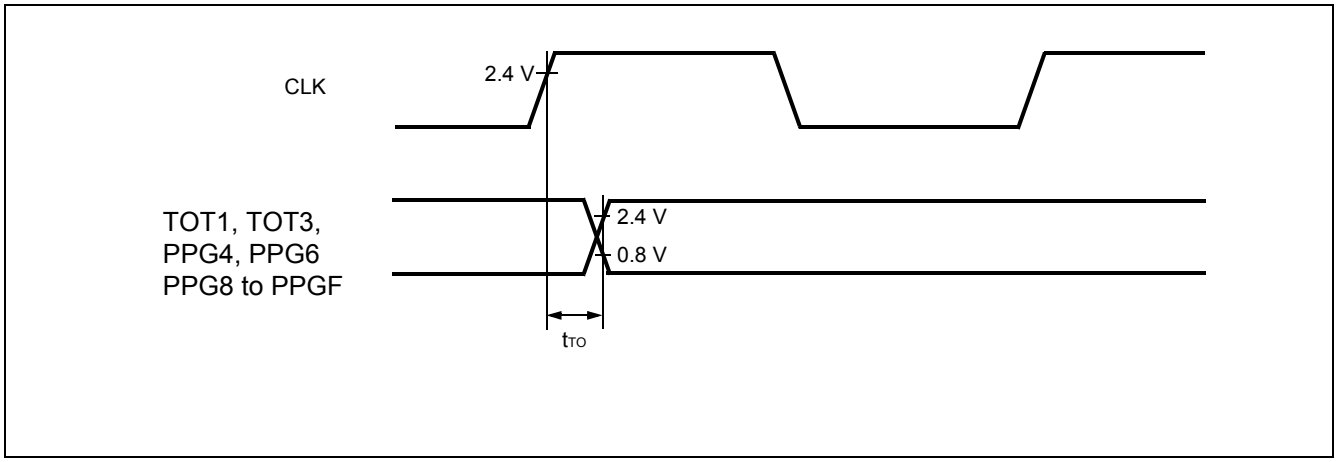



■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK2, SCK3 | Internal clock operation output pins are CL = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK2, SCK3<br>SOT2, SOT3 | | –50 | +50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK2, SCK3<br>SIN2, SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK2, SCK3<br>SIN2, SIN3 | | 0 | — | ns |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK2, SCK3<br>SOT2, SOT3 | | 3 $t_{CP}$ – 70 | — | ns |

Notes : • $C_L$ is load capacity value of pins when testing.
• $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.




### 13.4.13 $I^2C$ Timing

($T_A$ = −40°C to +125°C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Condition | Standard-mode | | Fast-mode*4 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| Hold time for (repeated) START condition SDA ↓ → SCL ↓ | $t_{HDSTA}$ | | 4.0 | — | 0.6 | — | µs |
| "L" width of the SCL clock | $t_{LOW}$ | | 4.7 | — | 1.3 | — | µs |
| "H" width of the SCL clock | $t_{HIGH}$ | | 4.0 | — | 0.6 | — | µs |
| Set-up time for a repeated START condition SCL ↑ → SDA ↓ | $t_{SUSTA}$ | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data set-up time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | | 250*5 | — | 100*5 | — | ns |
| Set-up time for STOP condition SCL ↑ → SDA ↑ | $t_{SUSTO}$ | | 4.0 | — | 0.6 | — | µs |
| Bus free time between STOP condition and START condition | $t_{BUS}$ | | 4.7 | — | 1.3 | — | µs |

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

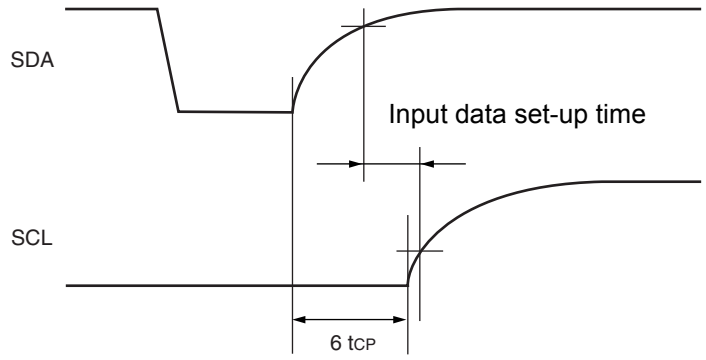
*2 : The maximum $t_{HDDAT}$ has to meet at least that the device does not exceed the "L" width ($t_{LOW}$) of the SCL signal.

*3 : A Fast-mode $I^2C$ -bus device can be used in a Standard-mode $I^2C$-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

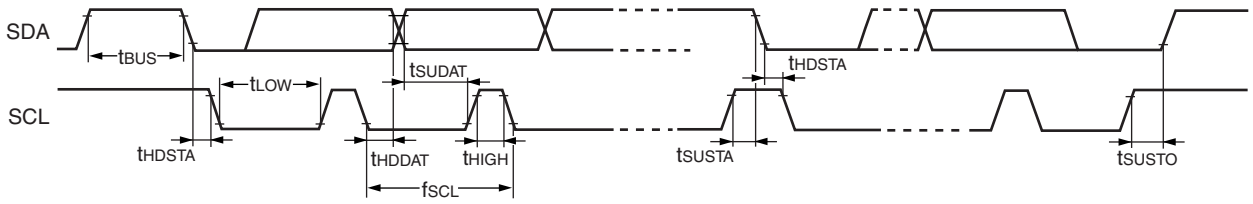
*5 : Refer to "• Note of SDA, SCL set-up time".

• Note of SDA, SCL set-up time




Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition

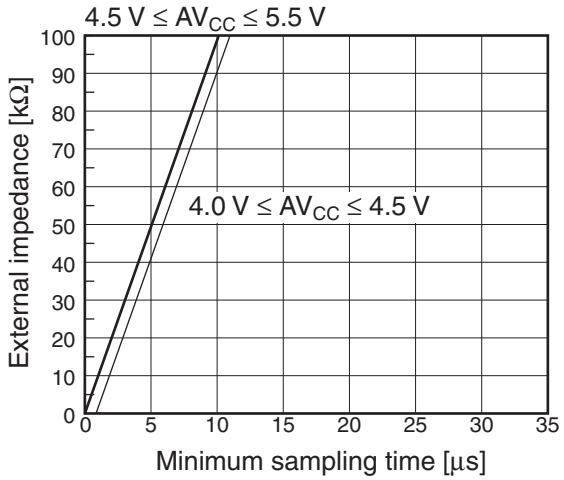


■ MASK ROM device

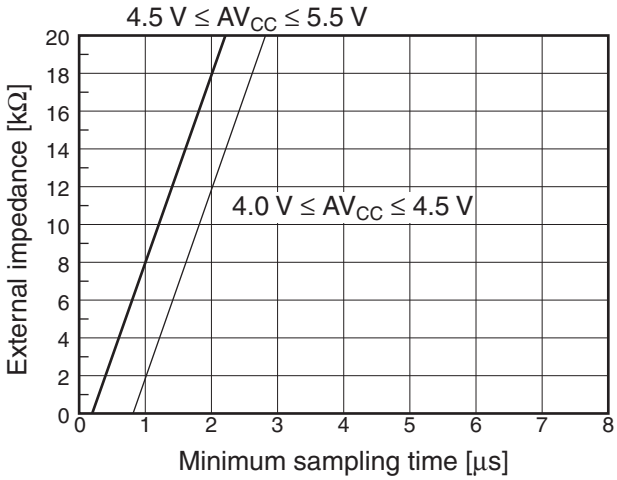
· Relation between External impedance and minimum sampling time

( MB90351E(S),MB90351TE(S),MB90352E(S),MB90352TE(S),MB90356E(S), MB90356TE(S),MB90357E(S),MB90357TE(S),MB90V340E-101/102/103/104)

[External impedance = 0 kΩ to 100 kΩ]




[External impedance = 0 kΩ to 20kΩ]




■ About the error

Values of relative errors grow larger, as |AVRH − $AV_{SS}$| becomes smaller.

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Flash memory Data Retention Time | Average $T_A$ = +85°C | 20 | — | — | year | * |

* : Corresponding value comes from the technology reliability evaluation result.
(Using Arrhenius equation to translate high temperature measurements test result into normalized value at +85°C)

## 14. Ordering Information

| Part number | Package | Remarks |
|---|---|---|
| MB90F351EPMC | 64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch | Flash memory products (64 Kbytes) |
| MB90F351ESPMC | | |
| MB90F351TEPMC | | |
| MB90F351TESPMC | | |
| MB90F356EPMC | | |
| MB90F356ESPMC | | |
| MB90F356TEPMC | | |
| MB90F356TESPMC | | |
| MB90F352EPMC | 64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch | Dual operation Flash memory products (128 Kbytes) |
| MB90F352ESPMC | | |
| MB90F352TEPMC | | |
| MB90F352TESPMC | | |
| MB90F357EPMC | | |
| MB90F357ESPMC | | |
| MB90F357TEPMC | | |
| MB90F357TESPMC | | |
| MB90351EPMC | 64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch | MASK ROM products (64 Kbytes) |
| MB90351ESPMC | | |
| MB90351TEPMC | | |
| MB90351TESPMC | | |
| MB90356EPMC | | |
| MB90356ESPMC | | |
| MB90356TEPMC | | |
| MB90356TESPMC | | |
| MB90352EPMC | 64-pin plastic LQFP FPT-64P-M23 12.0 mm □, 0.65 mm pitch | MASK ROM products (128 Kbytes) |
| MB90352ESPMC | | |
| MB90352TEPMC | | |
| MB90352TESPMC | | |
| MB90357EPMC | | |
| MB90357ESPMC | | |
| MB90357TEPMC | | |
| MB90357TESPMC | | |

*(Continued)*