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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90352espmc-gs-229e1

- 8/16-bit PPG timer : 8-bit ∞ 10 channels or 16-bit $\times$ 6 channels
- 16-bit reload timer : 2 channels (only Evaluation products has 4 channels)
- 16-bit input/output timer
 - 16-bit free-run timer : 2 channels (FRT0 : ICU0/1, FRT1 : ICU4/5/6/7, OCU4/5/6/7)
 - 16-bit input capture: (ICU) : 6 channels
 - 16-bit output compare : (OCU) : 4 channels

FULL-CAN interface: 1 channel

- Compliant with CAN standard Version2.0 Part A and Part B
- 16 message buffers are built-in
- CAN wake-up function

LIN-UART: 2 channels

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

I²C interface: 1 channel

Up to 400 kbps transfer rate

DTP/External interrupt: 8 channels, CAN wakeup: 1 channel

Module for activation of extended intelligent I/O service (EI²OS), DMA, and generation of external interrupt by external input.

Delay interrupt generator module

Generates interrupt request for task switching.

8/10-bit A/D converter: 15 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3 μ s (at 24 MHz machine clock, including sampling time)

Address matching detection (Program patch) function

- Address matching detection for 6 address pointers.

Capable of changing input voltage level for port

- Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)
- TTL level (corresponds to external bus pins only, initial level of these pins is TTL in external bus mode)

Low voltage/CPU operation detection reset (devices with T-suffix)

- Detects low voltage (4.0 V $\pm$ 0.3 V) and resets automatically
- Resets automatically when program is runaway and counter is not cleared within interval time (approx. 262 ms : external 4 MHz)

Dual operation Flash memory (only devices 128 Kbytes Flash memory)

- Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.

Supported T_A = + 125°C

The maximum operating frequency is 24 MHz* : (at T_A = +125°C) .

Flash security function

- Protects the content of Flash memory (MB90F352x, MB90F357x only)

External bus interface

- 4 Mbytes external memory space
MB90F351E(S), MB90F351TE(S), MB90F352E(S), MB90F352TE(S) : External bus Interface can not be used in internal vector mode. It can be used only in external vector mode.

* : If used exceeding T_A = + 105 °C, be sure to contact Cypress for reliability limitations.

1. Product Lineup1 (Without Clock supervisor function)

■ Flash memory products

Flash memory products Part Number	MB90F351E MB90F352E	MB90F351TE MB90F352TE	MB90F351ES MB90F352ES	MB90F351TES MB90F352TES
Parameter				
Type	Flash memory products			
CPU	F ² MC-16LX CPU			
System clock	PLL clock multiplication circuit (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	64 Kbytes Flash memory : MB90F351E(S), MB90F351TE(S) 128 Kbytes Dual operation Flash memory (Erase/write and read can be operated at the same time) : MB90F352E(S), MB90F352TE(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No	
Clock supervisor	No			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus			
Operating temperature	−40°C to +125°C			
Package	LQFP-64			
LIN-UART	2 channels			
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I ² C (400 kbps)	1 channel			
A/D converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit reload timer (2 channels)	Operation clock frequency : fsys/2 ¹ , fsys/2 ³ , fsys/2 ⁵ (fsys = Machine clock frequency) Supports External Event Count function.			
16-bit Free-run timer (2 channels)	Free-run Timer 0 (clock input FRCK0) corresponds to ICU0/1. Free-run Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when it matches Output Compare (ch.0, ch.4) . Operation clock frequency : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ , fsys/2 ⁵ , fsys/2 ⁶ , fsys/2 ⁷ (fsys = Machine clock frequency)			
16-bit output compare	4 channels			
	Signals an interrupt when 16-bit free-run Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			

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3. Packages and Product Correspondence

Package	MB90V340E-101 MB90V340E-102 MB90V340E-103 MB90V340E-104	MB90351E (S) , MB90351TE (S) MB90F351E (S) , MB90F351TE (S) MB90352E (S) , MB90352TE (S) MB90F352E (S) , MB90F352TE (S) MB90356E (S) , MB90356TE (S) MB90F356E (S) , MB90F356TE (S) MB90357E (S) , MB90357TE (S) MB90F357E (S) , MB90F357TE (S)
PGA-299C-A01	○	×
FPT-64P-M23 (12.0 mm □ , 0.65 mm pitch)	×	○
FPT-64P-M24 (10.0 mm □ , 0.50 mm pitch)	×	○

○ : Yes, × : No

Note : Refer to "[Package Dimensions](#)" for detail of each package.

5. Pin Description

Pin No.	Pin name	I/O Circuit type*	Function
46	X1	A	Oscillation output pin
47	X0		Oscillation input pin
45	RST	E	Reset input pin
3 to 8	P62 to P67	I	General purpose I/O ports
	AN2 to AN7		Analog input pins for A/D converter
	PPG4 (5), 6 (7), 8 (9), A (B), C (D), E (F)		Output pins for PPGs
9	P50	O	General purpose I/O port
	AN8		Analog input pin for A/D converter
	SIN2		Serial data input pin for UART2
10	P51	I	General purpose I/O port
	AN9		Analog input pin for A/D converter
	SOT2		Serial data output pin for UART2
11	P52	I	General purpose I/O port
	AN10		Analog input pin for A/D converter
	SCK2		Serial clock I/O pin for UART2
12	P53	I	General purpose I/O port
	AN11		Analog input pin for A/D converter
	TIN3		Event input pin for reload timer3
13	P54	I	General purpose I/O port
	AN12		Analog input pin for A/D converter
	TOT3		Output pin for reload timer3
14, 15	P55, P56	I	General purpose I/O ports
	AN13, AN14		Analog input pins for A/D converter
16	P42	F	General purpose I/O port
	IN6		Data sample input pin for input capture ICU6
	RX1		RX input pin for CAN1
	INT9R		External interrupt request input pin for INT9
17	P43	F	General purpose I/O port
	IN7		Data sample input pin for input capture ICU7
	TX1		TX output pin for CAN1
19, 20	P40, P41	F	General purpose I/O ports (devices with S-suffix and MB90V340E-101/103)
	X0A, X1A	B	X0A : Oscillation input pin for sub clock X1A : Oscillation output pin for sub clock (devices without S-suffix and MB90V340E-102/104)

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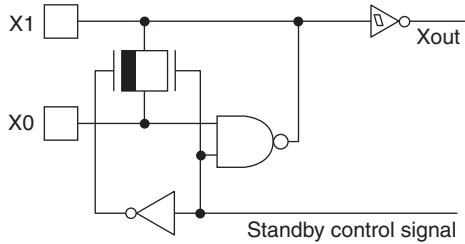
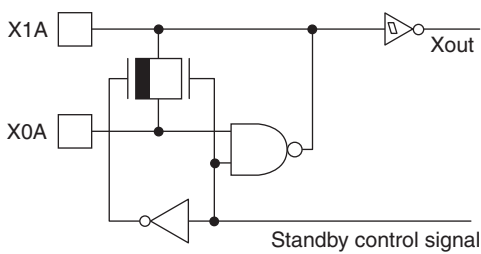
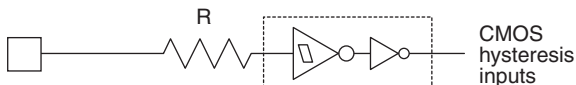
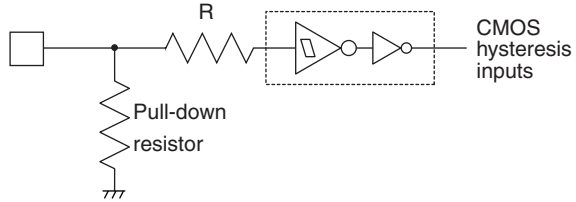
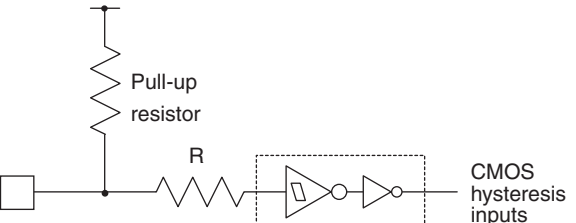
Pin No.	Pin name	I/O Circuit type*	Function
24 to 31	P00 to P07	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD00 to AD07		Input/output pins of external address data bus lower 8 bits. This function is enabled when the external bus is enabled.
	INT8 to INT15		External interrupt request input pins for INT8 to INT15
32	P10	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD08		Input/output pin for external bus address data bus bit 8. This function is enabled when external bus is enabled.
	TIN1		Event input pin for reload timer1
33	P11	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD09		Input/output pin for external bus address data bus bit 9. This function is enabled when external bus is enabled.
	TOT1		Output pin for reload timer1
34	P12	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD10		Input/output pin for external bus address data bus bit 10. This function is enabled when external bus is enabled.
	SIN3		Serial data input pin for UART3
	INT11R		External interrupt request input pin for INT11
35	P13	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD11		Input/output pin for external bus address data bus bit 11. This function is enabled when external bus is enabled.
	SOT3		Serial data output pin for UART3
36	P14	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD12		Input/output pin for external bus address data bus bit 12. This function is enabled when external bus is enabled.
	SCK3		Clock input/output pin for UART3
37	P15	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD13		Input/output pin for external bus address data bus bit 13. This function is enabled when external bus is enabled.
38	P16	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD14		Input/output pin for external bus address data bus bit 14. This function is enabled when external bus is enabled.

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Pin No.	Pin name	I/O Circuit type*	Function
54	P30	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when external bus is enabled.
	IN4		Data sample input pin for input capture ICU4
55	P31	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	$\overline{\text{RD}}$		Read strobe output pin for data bus. This function is enabled when external bus is enabled.
	IN5		Data sample input pin for input capture ICU5
56	P32	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{\text{WR/WRL}}$ pin output disabled.
	$\overline{\text{WR/WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR/WRL}}$ pin output are enabled. WRL is used to write-strobe 8 lower bits of the data bus in 16-bit access. WR is used to write-strobe 8 bits of the data bus in 8-bit access.
	INT10R		External interrupt request input pin for INT10
57	P33	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode, in external bus 8-bit mode or with the WRH pin output disabled.
	$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.
58	P34	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT4		Wave form output pin for output compare OCU4
59	P35	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT5		Wave form output pin for output compare OCU5
60	P36	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
	OUT6		Wave form output pin for output compare OCU6

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6. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 M Ω
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 M Ω
C		■ MASK ROM device CMOS hysteresis input pin ■ Flash memory device CMOS input pin
D		■ MASK ROM device CMOS hysteresis input pin Pull-down resistor value: approx. 50 k Ω ■ Flash memory device CMOS input pin No Pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 k Ω

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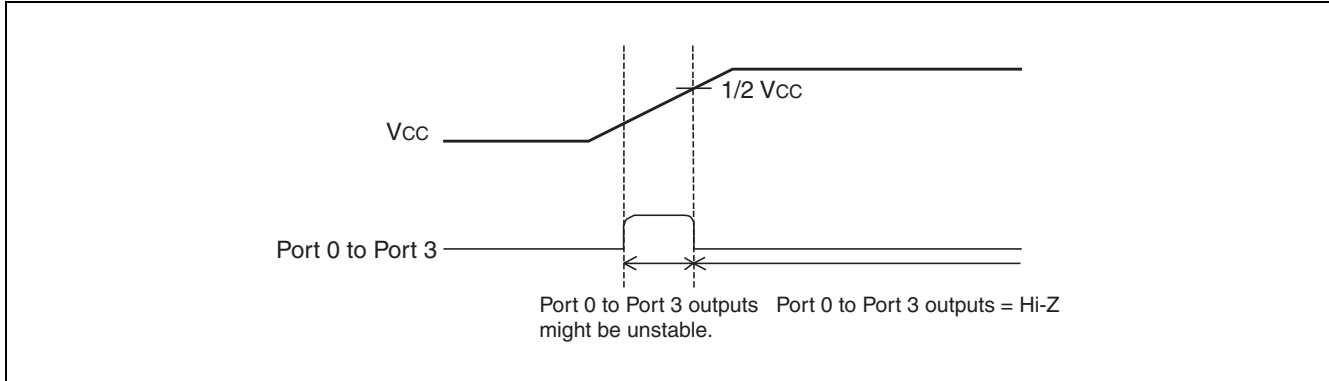
13. Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

14. Port 0 to port 3 output during power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable regardless of reset inputs.



15. Setting using CAN function

To use CAN function, please set "1" to DIRECT bit of CAN direct mode register (CDMR).

16. Flash security function

The security byte is located in the area of the Flash memory. If protection code 01_H is written in the security byte, the Flash memory is in the protected state by security.

Therefore please do not write 01_H in this address if you do not use the security function.

Please refer to following table for the address of the security byte.

Product name	Flash memory size	Address for security bit
MB90F352E(S) MB90F352TE(S) MB90F357E(S) MB90F357TE(S)	Embedded 1 Mbit Flash memory	FE0001 _H

17. Operation with $T_A = +105^\circ\text{C}$ or more

If used exceeding $T_A = +105^\circ\text{C}$, please contact Cypress sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.

The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

(1) Low voltage detection reset circuit

Detection voltage
4.0 V $\pm$ 0.3 V

When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to "1" and an internal reset signal is output.

Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.

Address	Register	Abbreviation	Access	Resource name	Initial value
00009B _H	DMA Descriptor Channel Specification Register	DCSR	R/W	DMA	00000000 _B
00009C _H	DMA Status Register L Register	DSRL	R/W		00000000 _B
00009D _H	DMA Status Register H Register	DSRH	R/W		00000000 _B
00009E _H	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 _B
00009F _H	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXX0 _B
0000A0 _H	Low-power Consumption Mode Control Register	LPMCR	W,R/W	Low Power Consumption Control Circuit	00011000 _B
0000A1 _H	Clock Selection Register	CKSCR	R,R/W	Low Power Consumption Control Circuit	11111100 _B
0000A2 _H , 0000A3 _H	Reserved				
0000A4 _H	DMA Stop Status Register	DSSR	R/W	DMA	00000000 _B
0000A5 _H	Automatic Ready Function Selection Register	ARSR	W	External Memory Access	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W		00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
0000A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXX111 _B
0000A9 _H	Timebase Timer Control Register	TBTC	W,R/W	Timebase timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H	Reserved				
0000AC _H	DMA Enable Register L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable Register H Register	DERH	R/W		00000000 _B
0000AE _H	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B

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Address	Register	Abbreviation	Access	Resource name	Initial value
0000DF _H	Baud Rate Generator Register 21	BGR21	R/W	UART2	00000000 _B
0000E0 _H to 0000EF _H	Reserved				
0000F0 _H to 0000FF _H	External area				
007900 _H to 007907 _H	Reserved				
007908 _H	Reload Register L4	PRL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
007909 _H	Reload Register H4	PRLH4	R/W		XXXXXXXX _B
00790A _H	Reload Register L5	PRL5	R/W		XXXXXXXX _B
00790B _H	Reload Register H5	PRLH5	R/W		XXXXXXXX _B
00790C _H	Reload Register L6	PRL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
00790D _H	Reload Register H6	PRLH6	R/W		XXXXXXXX _B
00790E _H	Reload Register L7	PRL7	R/W		XXXXXXXX _B
00790F _H	Reload Register H7	PRLH7	R/W		XXXXXXXX _B
007910 _H	Reload Register L8	PRL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX _B
007911 _H	Reload Register H8	PRLH8	R/W		XXXXXXXX _B
007912 _H	Reload Register L9	PRL9	R/W		XXXXXXXX _B
007913 _H	Reload Register H9	PRLH9	R/W		XXXXXXXX _B
007914 _H	Reload Register LA	PRLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX _B
007915 _H	Reload Register HA	PRLHA	R/W		XXXXXXXX _B
007916 _H	Reload Register LB	PRLB	R/W		XXXXXXXX _B
007917 _H	Reload Register HB	PRLHB	R/W		XXXXXXXX _B
007918 _H	Reload Register LC	PRLC	R/W	16-bit Programmable Pulse Generator C/D	XXXXXXXX _B
007919 _H	Reload Register HC	PRLHC	R/W		XXXXXXXX _B
00791A _H	Reload Register LD	PRLD	R/W		XXXXXXXX _B
00791B _H	Reload Register HD	PRLHD	R/W		XXXXXXXX _B
00791C _H	Reload Register LE	PRLLE	R/W	16-bit Programmable Pulse Generator E/F	XXXXXXXX _B
00791D _H	Reload Register HE	PRLHE	R/W		XXXXXXXX _B
00791E _H	Reload Register LF	PRLLE	R/W		XXXXXXXX _B
00791F _H	Reload Register HF	PRLHF	R/W		XXXXXXXX _B
007920 _H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
007921 _H	Input Capture Register 0	IPCP0	R		XXXXXXXX _B
007922 _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
007923 _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B

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List of Control Registers

Address	Register	Abbreviation	Access	Initial Value
CAN1				
000080 _H	Message buffer enable register	BVALR	R/W	00000000 _B 00000000 _B
000081 _H				
000082 _H	Transmit request register	TREQR	R/W	00000000 _B 00000000 _B
000083 _H				
000084 _H	Transmit cancel register	TCANR	W	00000000 _B 00000000 _B
000085 _H				
000086 _H	Transmission complete register	TCR	R/W	00000000 _B 00000000 _B
000087 _H				
000088 _H	Receive complete register	RCR	R/W	00000000 _B 00000000 _B
000089 _H				
00008A _H	Remote request receiving register	RRTRR	R/W	00000000 _B 00000000 _B
00008B _H				
00008C _H	Receive overrun register	ROVRR	R/W	00000000 _B 00000000 _B
00008D _H				
00008E _H	Reception interrupt enable register	RIER	R/W	00000000 _B 00000000 _B
00008F _H				

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Address	Register	Abbreviation	Access	Initial Value
CAN1				
007D00 _H	Control status register	CSR	R/W, W R/W, R	0XXXX0X1 _B
007D01 _H				00XXXX00 _B
007D02 _H	Last event indicator register	LEIR	R/W	000X0000 _B
007D03 _H				XXXXXXXX _B
007D04 _H	Receive/transmit error counter	RTEC	R	00000000 _B
007D05 _H				00000000 _B
007D06 _H	Bit timing register	BTR	R/W	11111111 _B
007D07 _H				X1111111 _B
007D08 _H	IDE register	IDER	R/W	XXXXXXXX _B
007D09 _H				XXXXXXXX _B
007D0A _H	Transmit RTR register	TRTRR	R/W	00000000 _B
007D0B _H				00000000 _B
007D0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX _B
007D0D _H				XXXXXXXX _B
007D0E _H	Transmit interrupt enable register	TIER	R/W	00000000 _B
007D0F _H				00000000 _B
007D10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX _B
007D11 _H				XXXXXXXX _B
007D12 _H				XXXXXXXX _B
007D13 _H				XXXXXXXX _B
007D14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX _B
007D15 _H				XXXXXXXX _B
007D16 _H				XXXXXXXX _B
007D17 _H				XXXXXXXX _B
007D18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX _B
007D19 _H				XXXXXXXX _B
007D1A _H				XXXXXXXX _B
007D1B _H				XXXXXXXX _B

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C80 _H to 007C87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
007C88 _H to 007C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
007C90 _H to 007C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
007C98 _H to 007C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
007CA0 _H to 007CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
007CA8 _H to 007CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
007CB0 _H to 007CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
007CB8 _H to 007CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
007CC0 _H to 007CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
007CC8 _H to 007CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
007CD0 _H to 007CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
007CD8 _H to 007CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
007CE0 _H to 007CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
007CE8 _H to 007CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B

(Continued)

(Continued)

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Sym- bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCT}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During stopping clock supervisor, At watch mode $T_A = +25^{\circ}\text{C}$	—	10	35	μA	MB90351E MB90F351E MB90352E MB90F352E MB90356E MB90F356E MB90357E MB90F357E
			$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During operating clock supervisor, At watch mode $T_A = +25^{\circ}\text{C}$	—	25	150	μA	MB90356E MB90F356E MB90357E MB90F357E
			$V_{CC} = 5.0\text{ V}$, Internal CR oscillation/ 4 division, At watch mode $T_A = +25^{\circ}\text{C}$	—	25	150	μA	MB90356ES MB90F356ES MB90357ES MB90F357ES
			$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During stopping clock supervisor, At watch mode $T_A = +25^{\circ}\text{C}$	—	60	140	μA	MB90351TE MB90F351TE MB90352TE MB90F352TE MB90356TE MB90F356TE MB90357TE MB90F357TE
			$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During operating clock supervisor, At watch mode $T_A = +25^{\circ}\text{C}$	—	80	250	μA	MB90356TE MB90F356TE MB90357TE MB90F357TE
			$V_{CC} = 5.0\text{ V}$, Internal CR oscillation/ 4 division, At watch mode $T_A = +25^{\circ}\text{C}$	—	80	250	μA	MB90356TES MB90F356TES MB90357TES MB90F357TES
	I_{CCH}		$V_{CC} = 5.0\text{ V}$, At stop mode, $T_A = +25^{\circ}\text{C}$	—	7	25	μA	Devices without "T"-suffix
				—	60	130	μA	Devices with "T"-suffix
Input capacity	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, V_{CC} , V_{SS}	—	—	5	15	pF	

13.4 AC Characteristics

13.4.1 Clock Timing

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 (at PLL stop) When using an oscillation circuit
			4	—	16	MHz	1 multiplied PLL When using an oscillation circuit
			4	—	12	MHz	2 multiplied PLL When using an oscillation circuit
			4	—	8	MHz	3 multiplied PLL When using an oscillation circuit
			4	—	6	MHz	4 multiplied PLL When using an oscillation circuit
			—	—	4	MHz	6 multiplied PLL When using an oscillation circuit
		X0	3	—	24	MHz	1/2 (at PLL stop), When using an external clock
			4	—	24	MHz	1 multiplied PLL When using an external clock
			4	—	12	MHz	2 multiplied PLL When using an external clock
			4	—	8	MHz	3 multiplied PLL When using an external clock
			4	—	6	MHz	4 multiplied PLL When using an external clock
			—	—	4	MHz	6 multiplied PLL When using an external clock
	f_{CL}	X0A, X1A	—	32.768	100	kHz	When using sub clock
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio should be about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock

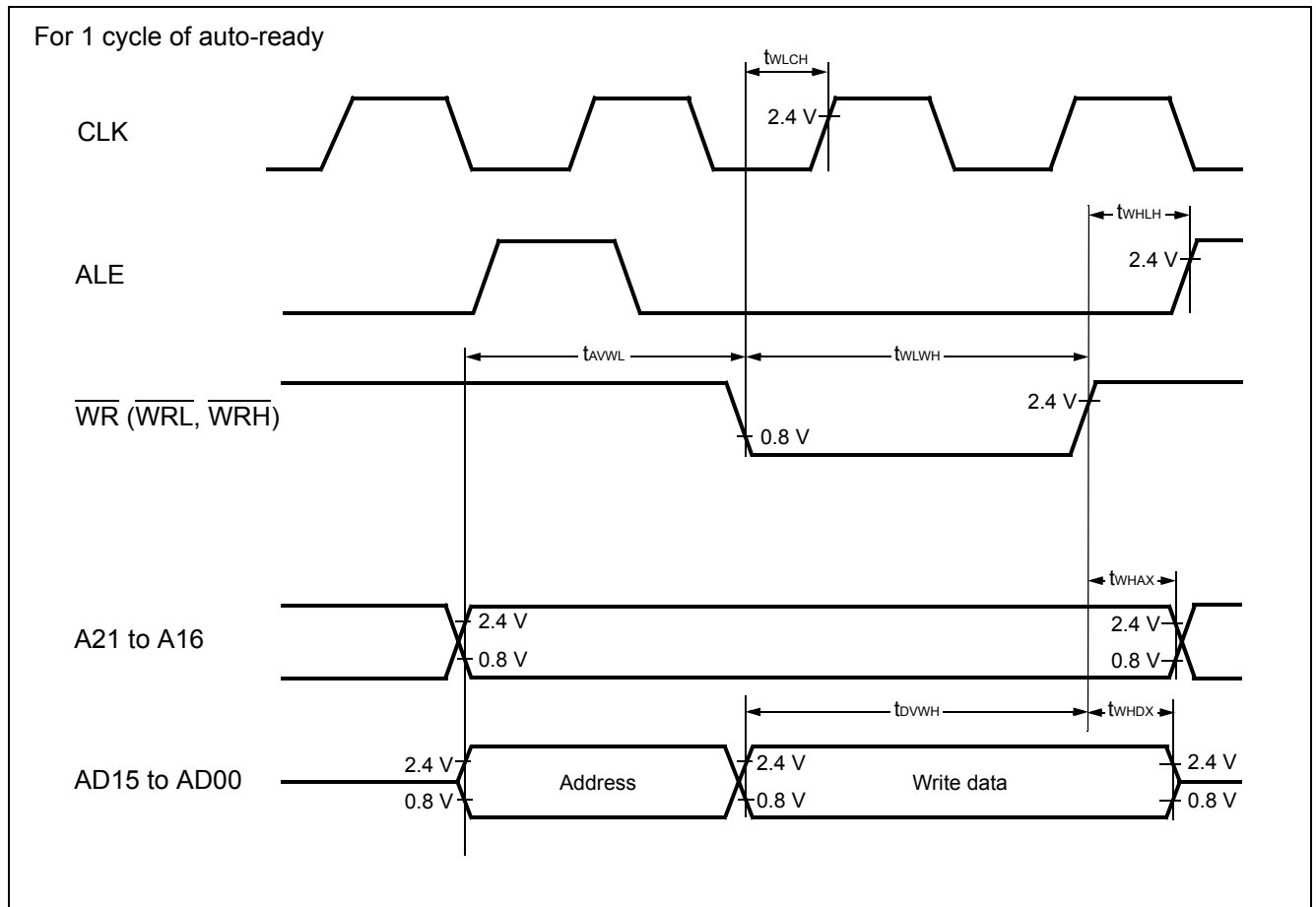
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13.4.6 Bus Timing (Write)

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address $\rightarrow \overline{\text{WR}} \downarrow$ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{\text{WR}}$	—	$t_{CP}-15$	—	ns
$\overline{\text{WR}}$ pulse width	t_{WLWH}	$\overline{\text{WR}}$		$(n^{*}+3/2)t_{CP} - 20$	—	ns
Valid data output $\rightarrow \overline{\text{WR}} \uparrow$ time	t_{DVWH}	AD15 to AD00, $\overline{\text{WR}}$		$(n^{*}+3/2)t_{CP} - 20$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{\text{WR}}$		15	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Address valid time	t_{WHAX}	A21 to A16, $\overline{\text{WR}}$		$t_{CP}/2 - 10$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow \text{ALE} \uparrow$ time	t_{WHLH}	$\overline{\text{WR}}$, ALE		$t_{CP}/2 - 15$	—	ns
$\overline{\text{WR}} \downarrow \rightarrow \text{CLK} \uparrow$ time	t_{WLCH}	$\overline{\text{WR}}$, CLK		$t_{CP}/2 - 15$	—	ns

* : Number of ready cycles

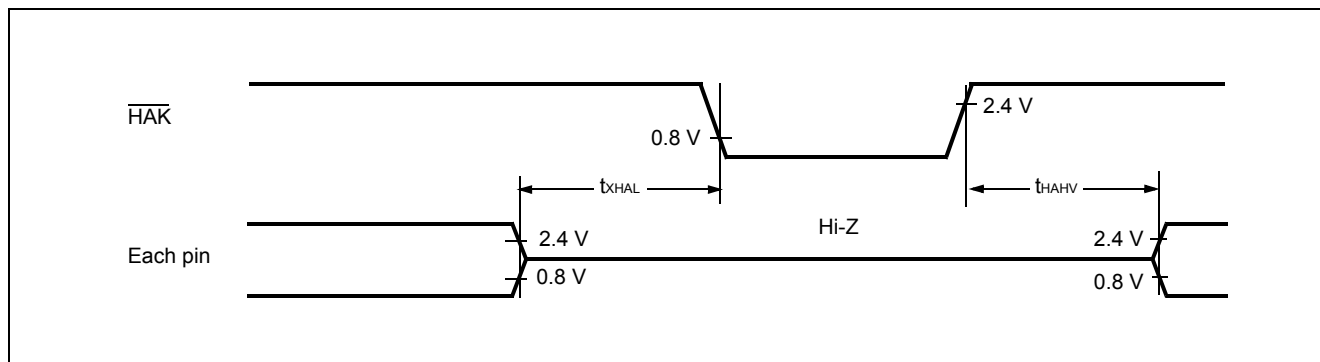


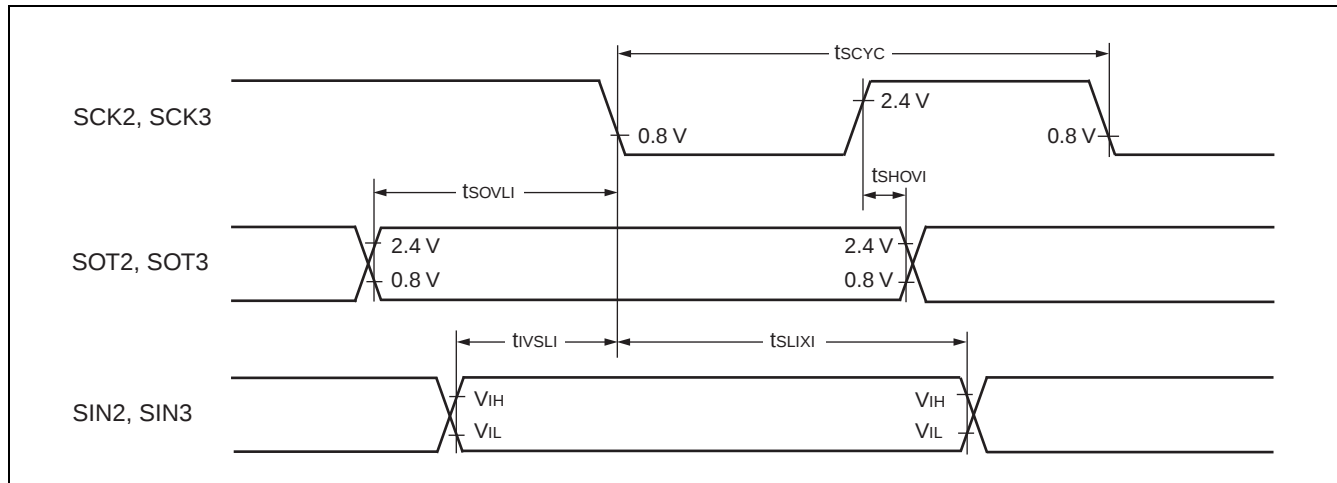
13.4.8 Hold Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Units
				Min	Max	
Pin floating $\rightarrow \overline{\text{HAK}} \downarrow$ time	$t_{X\text{HAL}}$	$\overline{\text{HAK}}$	—	30	t_{CP}	ns
$\overline{\text{HAK}} \uparrow$ time $\rightarrow$ Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$		t_{CP}	$2 t_{CP}$	ns

Note : There is more than 1 machine cycle from when HRQ pin reads in until the $\overline{\text{HAK}}$ is changed.



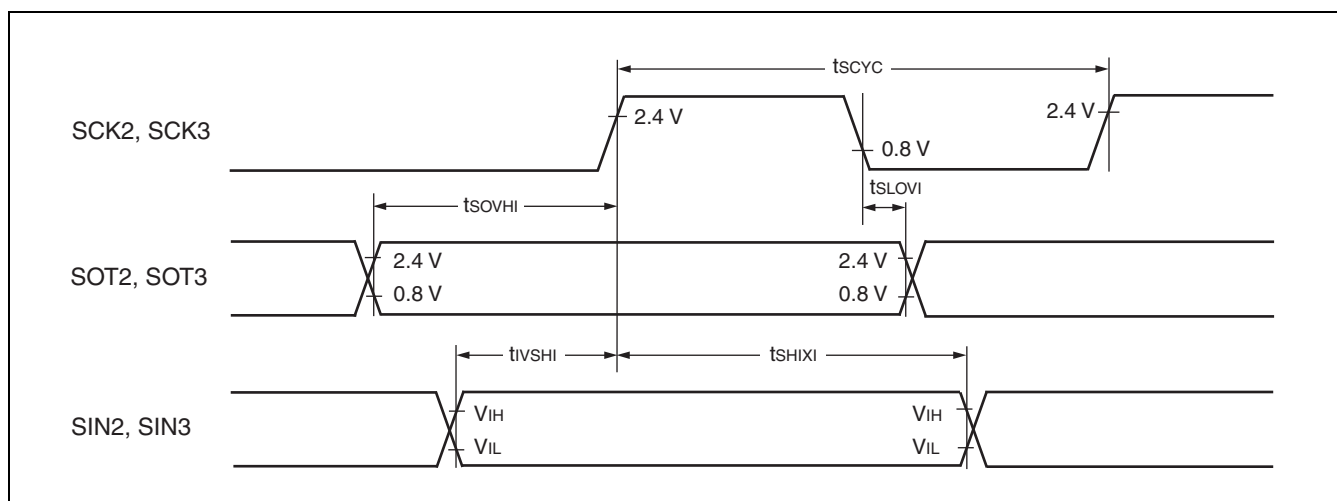


■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal clock operation output pins are $CL = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK2, SCK3 SOT2, SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCK2, SCK3 SIN2, SIN3		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK2, SCK3 SIN2, SIN3		0	—	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	t_{SOVHI}	SCK2, SCK3 SOT2, SOT3		$3 t_{CP} - 70$	—	ns

Notes : • C_L is load capacity value of pins when testing.
• t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

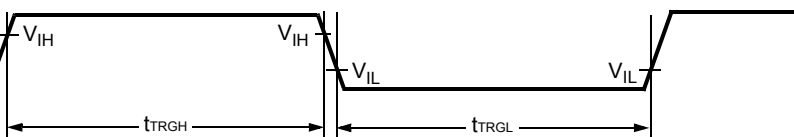


13.4.10 Trigger Input Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	$5 t_{CP}$	—	ns

INT8 to INT15,
INT9R to INT11R,
ADTG

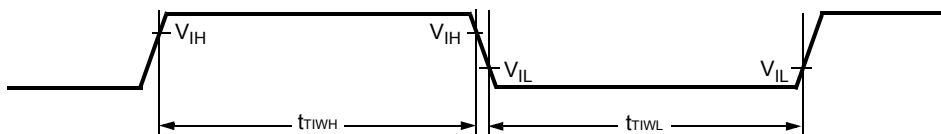


13.4.11 Timer Related Resource Input Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN1, TIN3, IN0, IN1, IN4 to IN7	—	$4 t_{CP}$	—	ns

TIN1, TIN3,
IN0, IN1,
IN4 to IN7

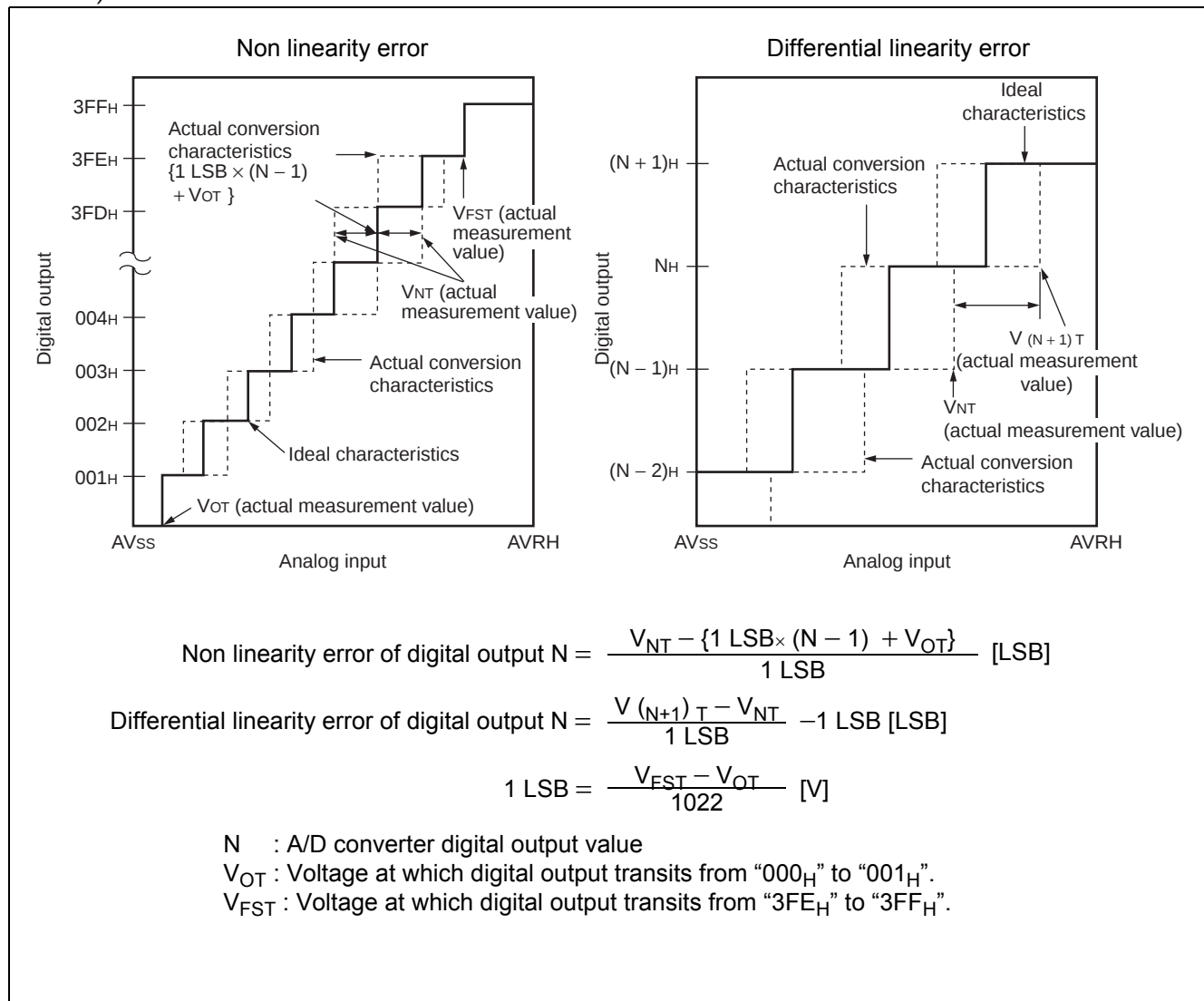


13.4.12 Timer Related Resource Output Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK $\uparrow$ $\rightarrow$ T_{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns

(Continued)



13.7 Flash Memory Program/Erase Characteristics

■ Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T _A = +25°C V _{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3600	μs	Except for the overhead time of the system level
Program/Erase cycle	—	10000	—	—	cycle	